Типы корпусов радиоэлектронных компонентов

Организации занимающиеся стандартизацией в САПР

Стандарт IPC 7351

Определяет размеры контактных площадок для стандартных типов корпусов чип-резисторов, чип-кондекнсаторов, диодов, транзисторов, индуктивностей и микросхем.

Действует взамен IPC-SM-782A

PCB MATRIX
NEW DIMENSIONS FOR EDA

www.pcblibraries.com

PCBSTANDARDS

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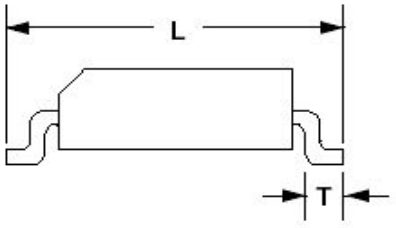
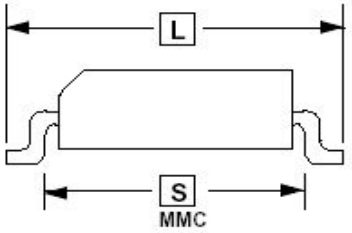
Точность размеров элементов и размеры площадок

A



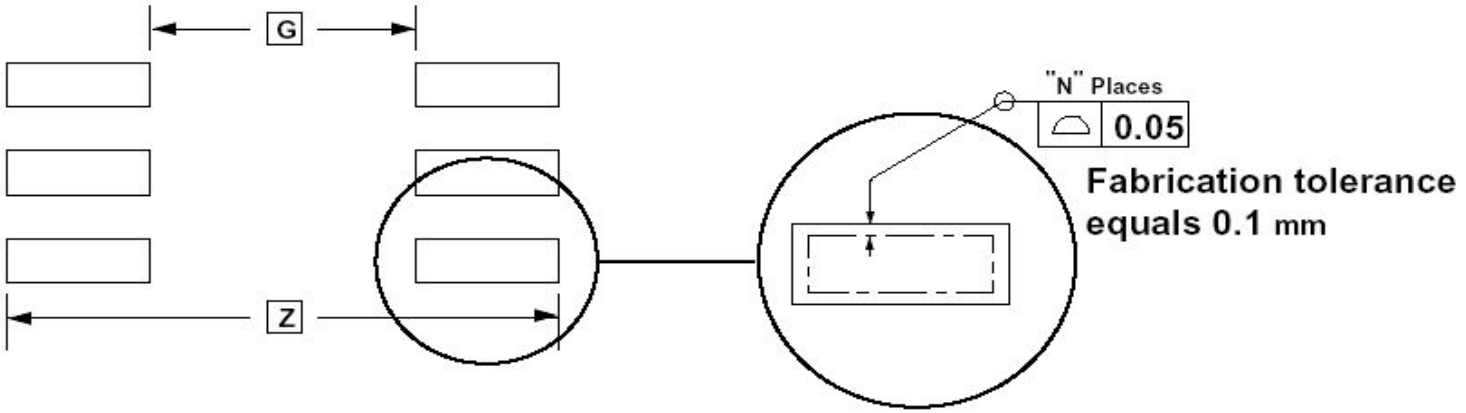
$$G_{MAX} = L_{MIN} - 2 * T_{MAX}$$

B

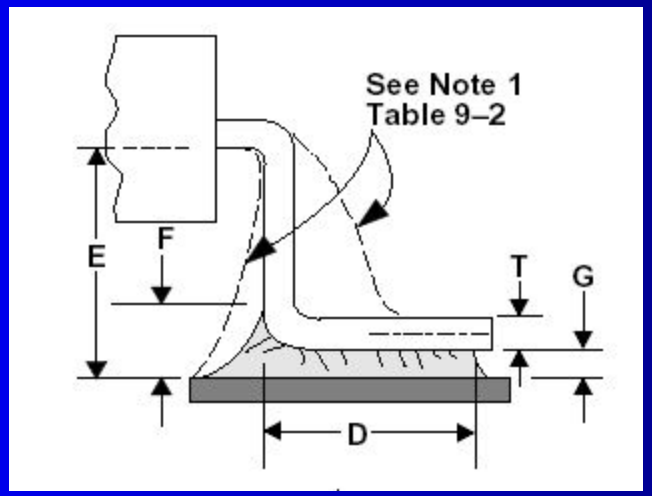


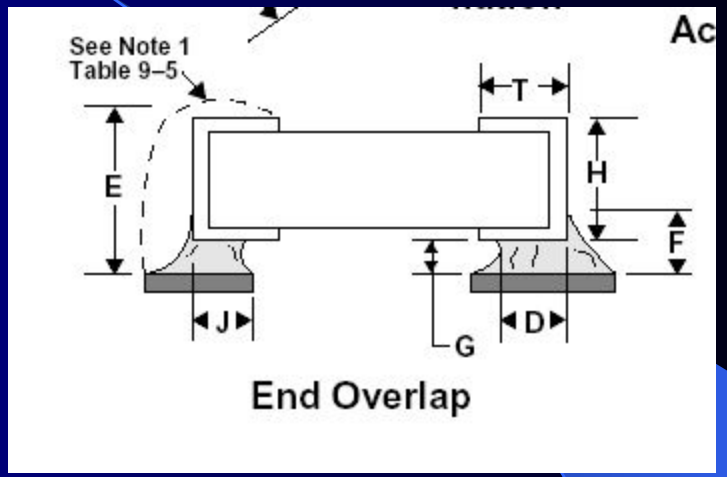
$$Z_{MIN} = L_{MAX} + 2 * X$$

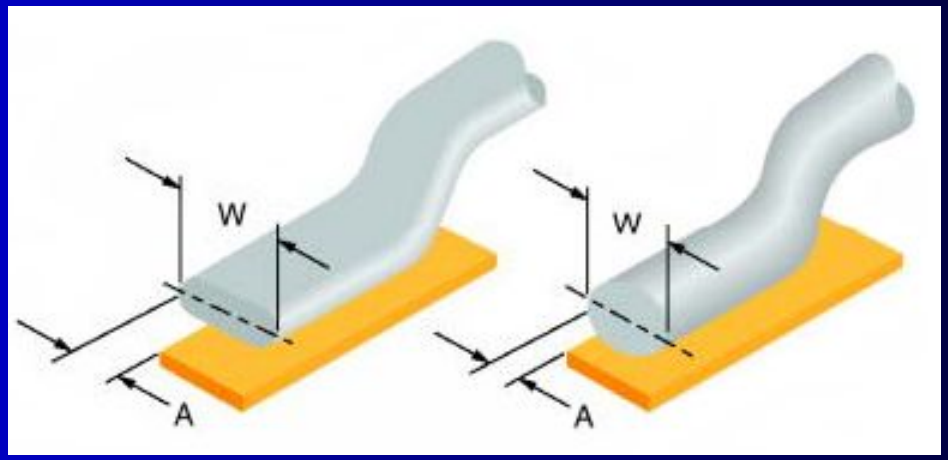
C



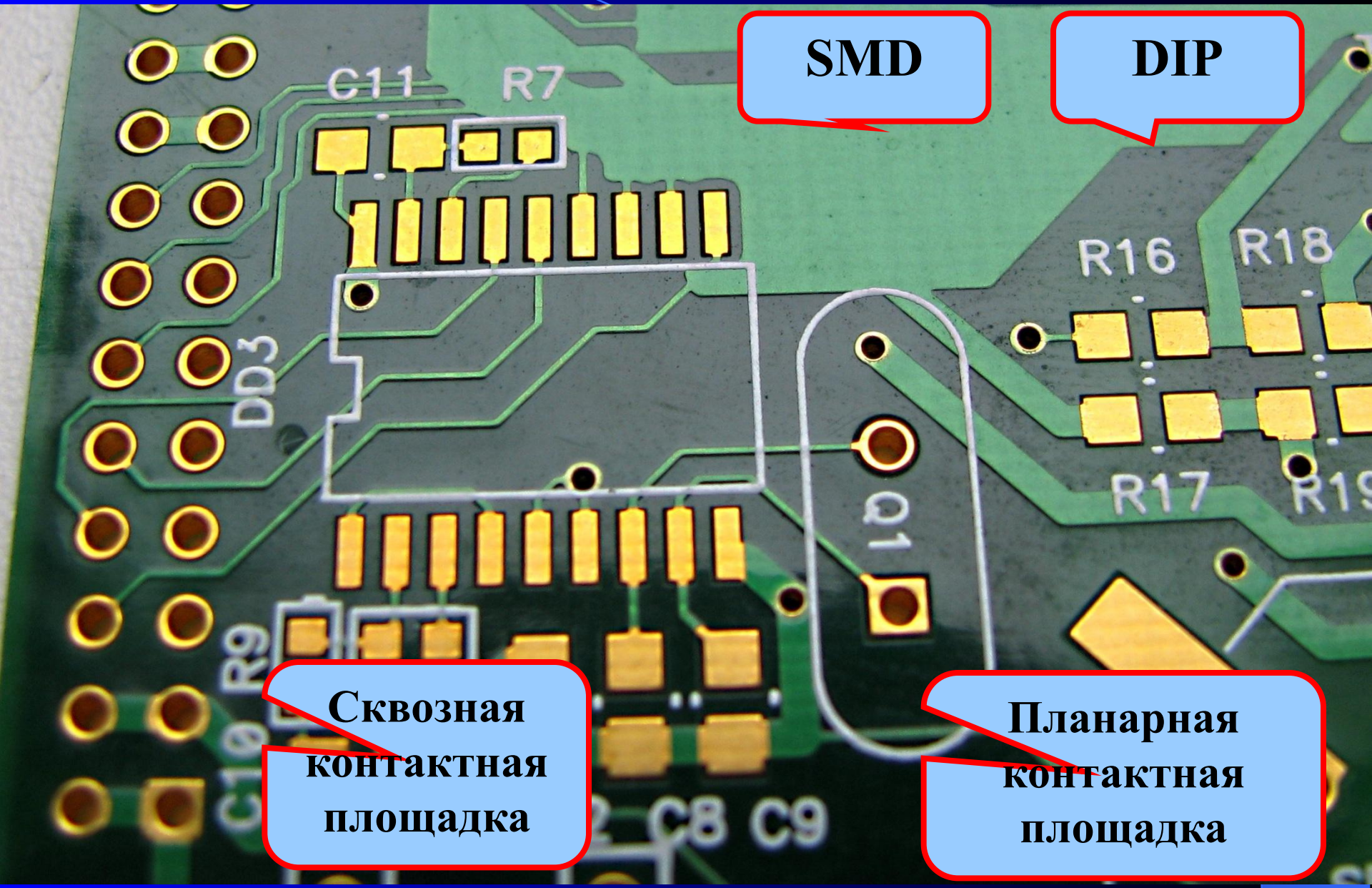
Форма вывода под пайку



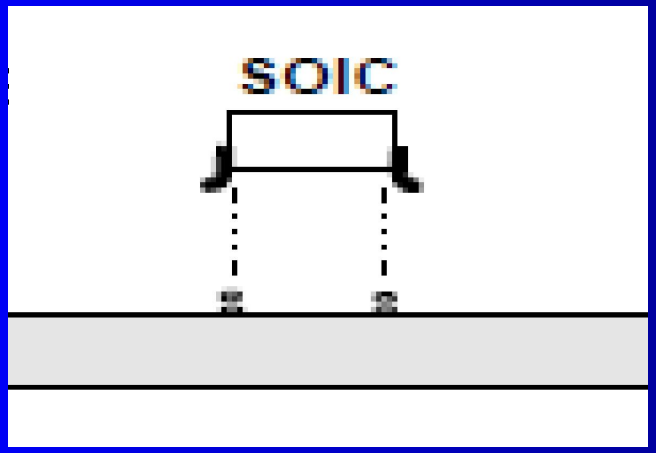




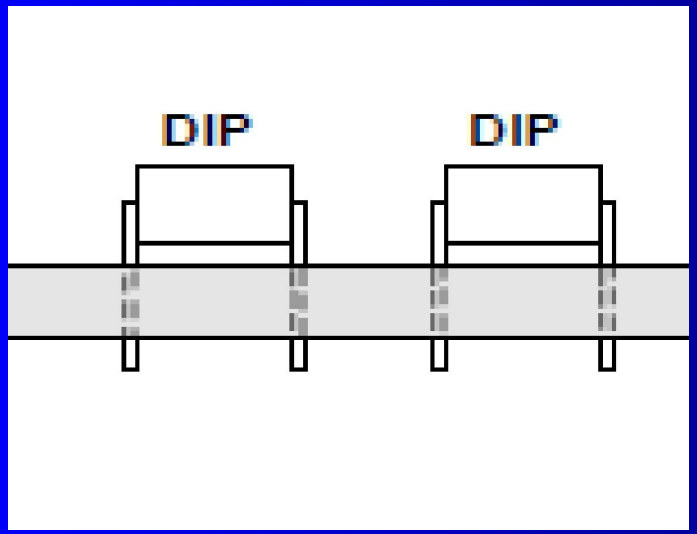
Контактные площадки



Типы посадочных мест



- **ПЛАНАРНЫЕ – без переходов на другую сторону платы (SMD – Surface Mounted Device)**



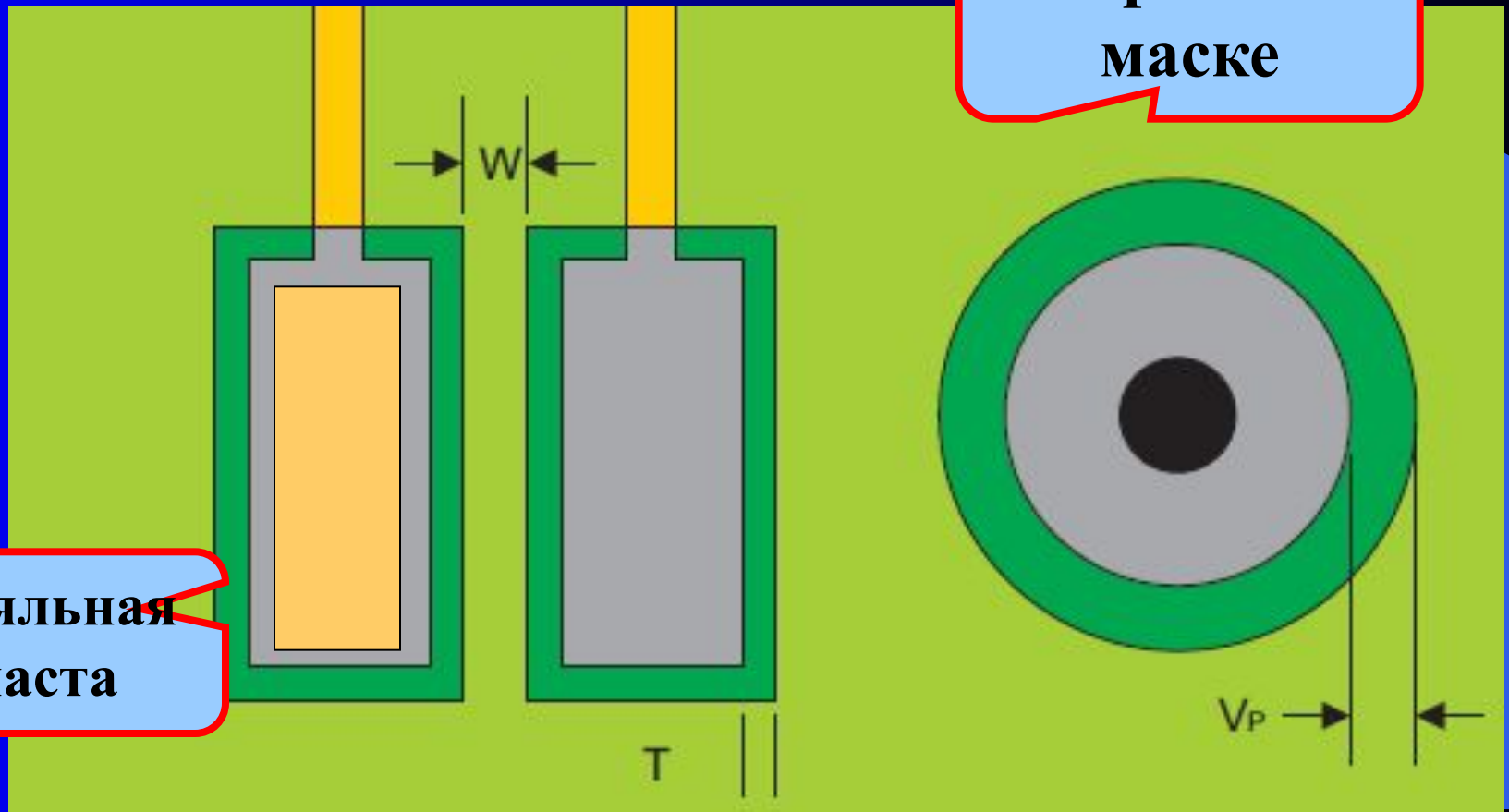
- **СКВОЗНЫЕ – с переходами на другую сторону платы (TH – Through Hole Mounted, DIP)**

Вскрытие маски

- **T = 0,05 – 0,1 мм**
- **W = 0,15 мм (Min)**
- **Vp = 0,1 мм**

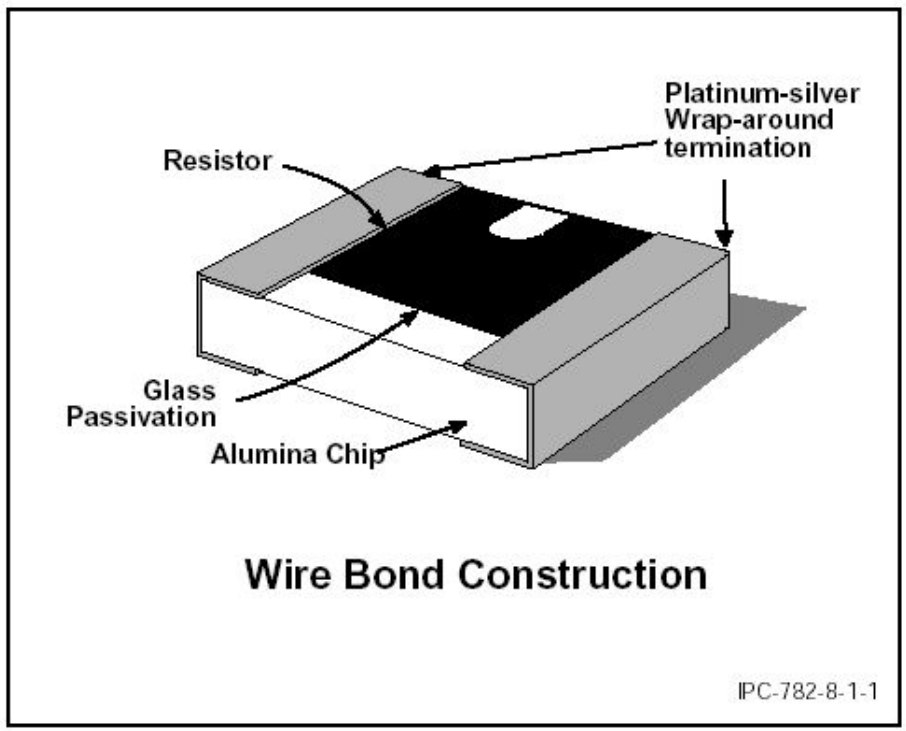
Контактная площадка

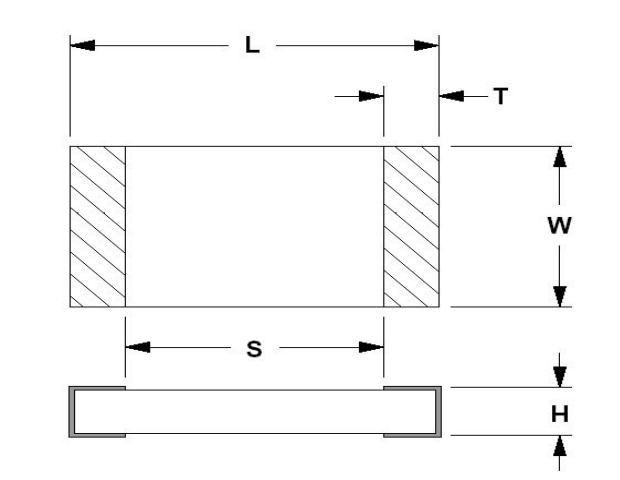
Вскрытие в маске



Паяльная паста

Чип резисторы



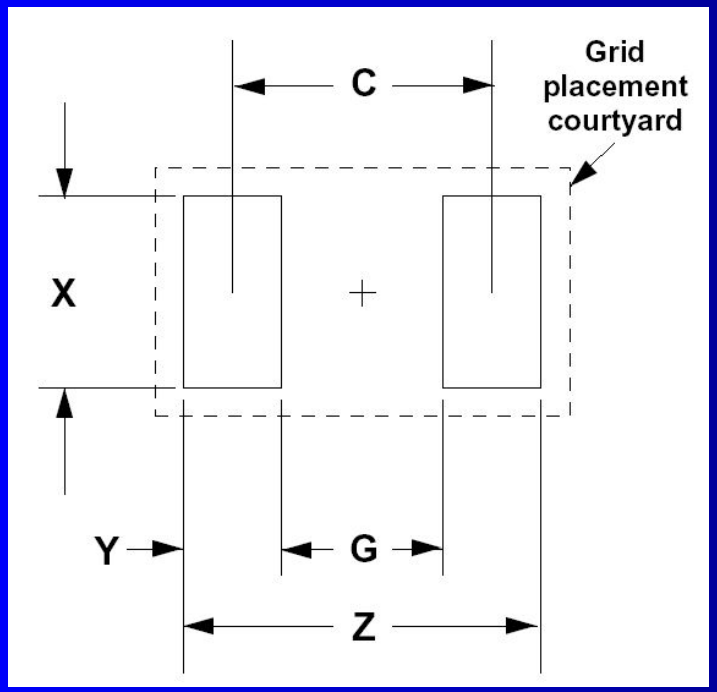


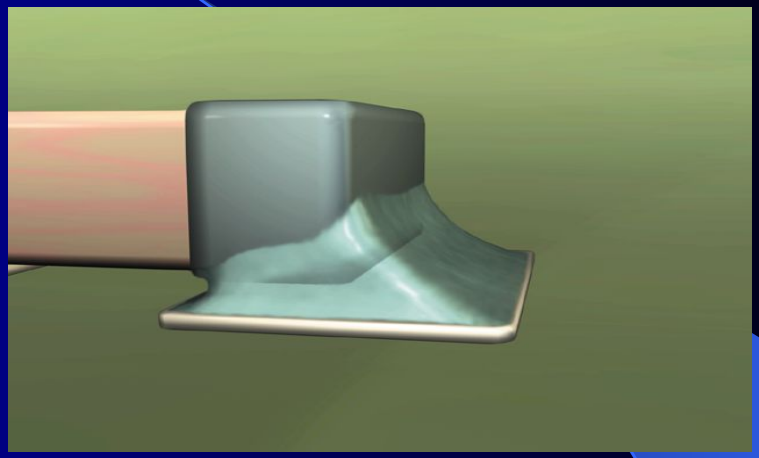
0402 □ 0,04” x 0,02”

1” = 25, 4 mm

mm [in] Component Identifier	L		S		W		T		H
	min	max	min	max	min	max	min	max	max
1005 [0402]	1.00	1.10	0.40	0.70	0.48	0.60	0.10	0.30	0.40
1608 [0603]	1.50	1.70	0.70	1.11	0.70	0.95	0.15	0.40	0.60
2012 [0805]	1.85	2.15	0.55	1.32	1.10	1.40	0.15	0.65	0.65
3216 [1206]	3.05	3.35	1.55	2.32	1.45	1.75	0.25	0.75	0.71
3225 [1210]	3.05	3.35	1.55	2.32	2.34	2.64	0.25	0.75	0.71
5025 [2010]	4.85	5.15	3.15	3.92	2.35	2.65	0.35	0.85	0.71
6332 [2512]	6.15	6.45	4.45	5.22	3.05	3.35	0.35	0.85	0.71

Посадочные места

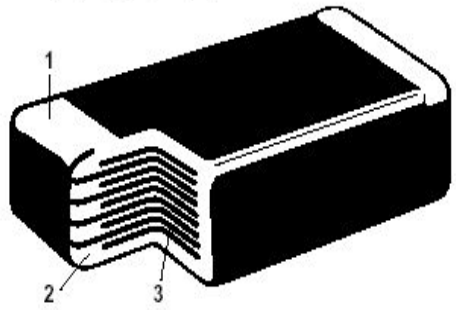


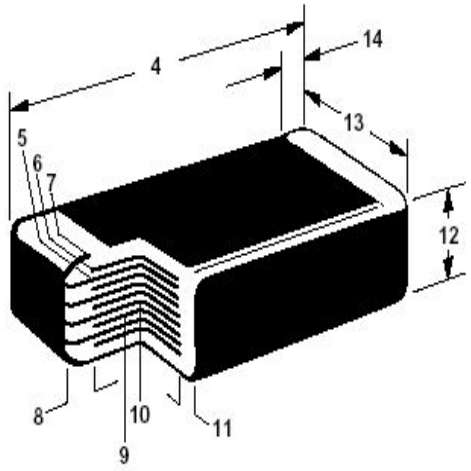


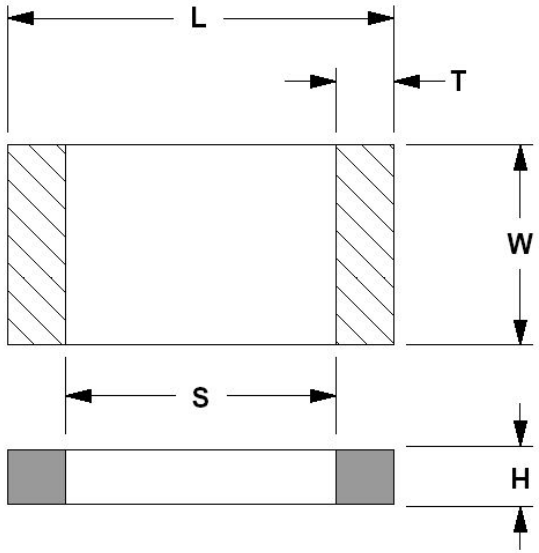
Component Identifier (mm) [in.]	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	Placement Grid (No. of Grid Elements)
1005 [0402]	2.20	0.40	0.70	0.90	1.30	2x6
1608 [0603]	2.80	0.60	1.00	1.10	1.70	4x6
2012 [0805]*	3.20	0.60	1.50	1.30	1.90	4x8
3216 [1206]*	4.40	1.20	1.80	1.60	2.80	4x10
3225 [1210]*	4.40	1.20	2.70	1.60	2.80	6x10
5025 [2010]*	6.20	2.60	2.70	1.80	4.40	6x14
6332 [2512]*	7.40	3.80	3.20	1.80	5.60	8x16

Чип-Конденсаторы

1. Termination
2. Dielectric
3. Electrode
4. Chip length
5. "A" electrode print
6. Electrode print
7. Cap (Topping layer)
8. End margin
9. Base layer
10. Shim (Active dielectric layer)
11. Side margin
12. Chip thickness
13. Chip width
14. Termination width

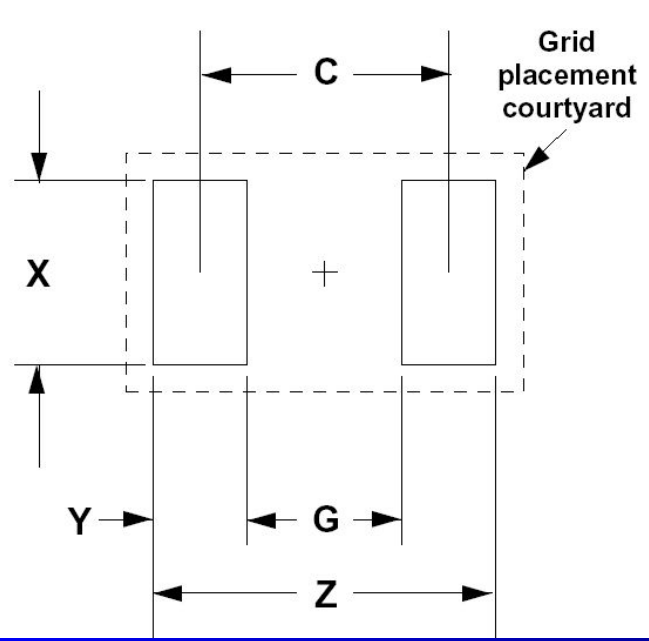


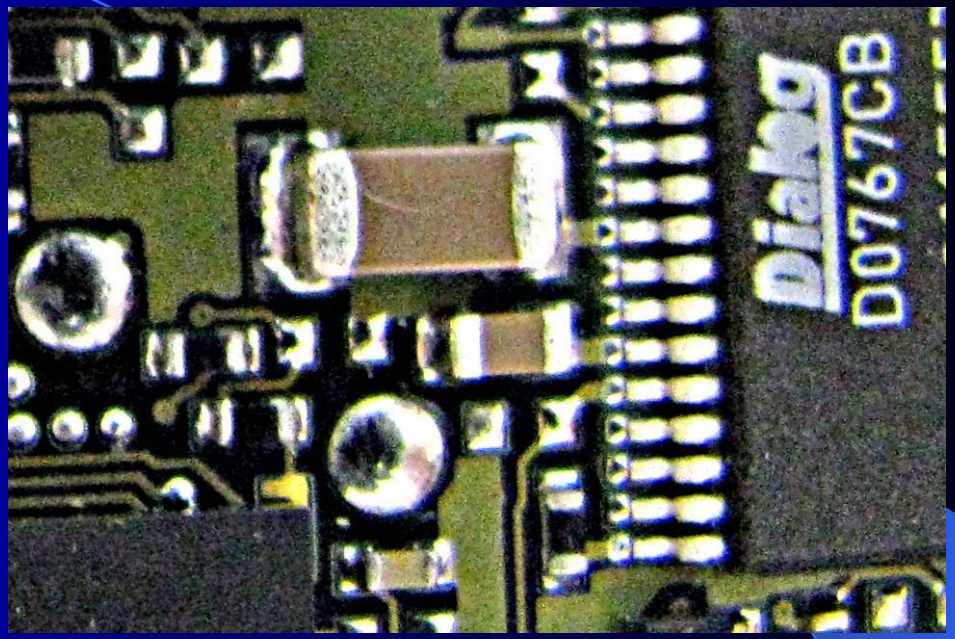




Component Identifier (mm) [in]	L		S		W		T		H
	min	max	min	max	min	max	min	max	max
1005 [0402]	0.90	1.10	0.30	0.65	0.40	0.60	0.10	0.30	0.60
1310 [0504]	1.02	1.32	0.26	0.72	0.77	1.27	0.13	0.38	1.02
1608 [0603]	1.45	1.75	0.45	0.97	0.65	0.95	0.20	0.50	0.85
2012 [0805]	1.80	2.20	0.30	1.11	1.05	1.45	0.25	0.75	1.10
3216 [1206]	3.00	3.40	1.50	2.31	1.40	1.80	0.25	0.75	1.35
3225 [1210]	3.00	3.40	1.50	2.31	2.30	2.70	0.25	0.75	1.35
4532 [1812]	4.20	4.80	2.30	3.46	3.00	3.40	0.25	0.95	1.35
4564 [1825]	4.20	4.80	2.30	3.46	6.00	6.80	0.25	0.95	1.10

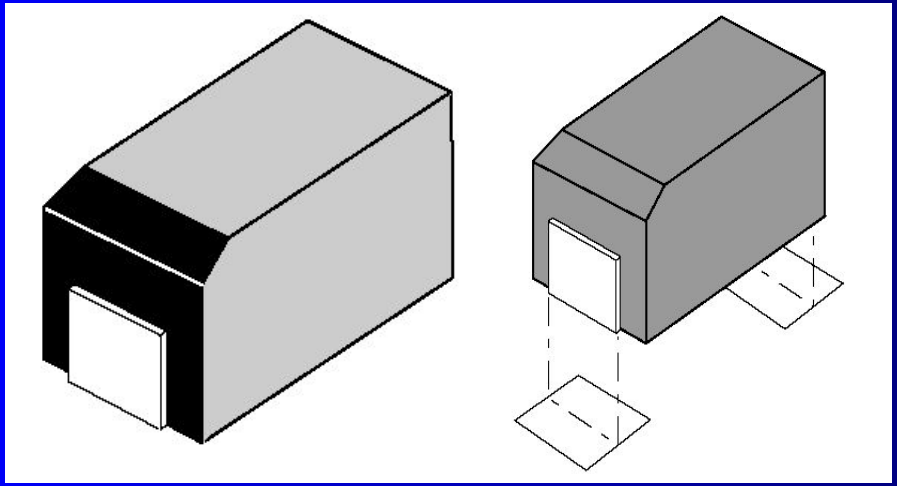
Посадочные места

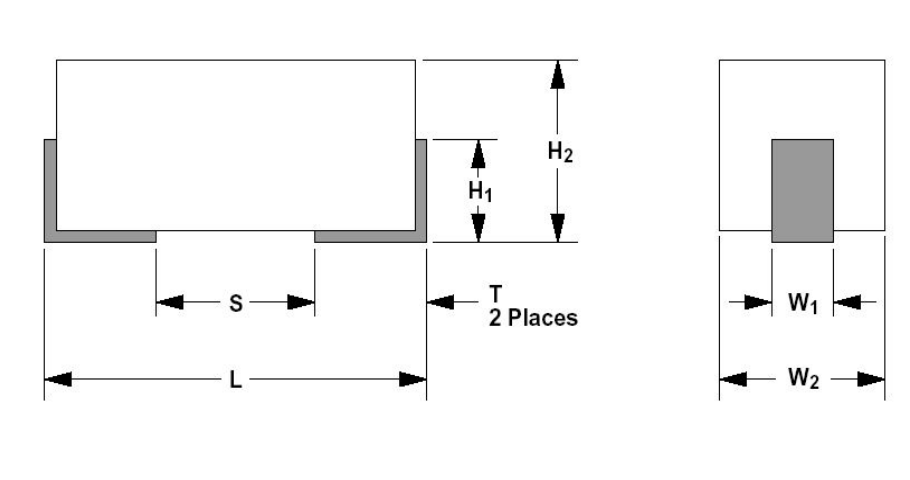




Component Identifier (mm) [in]	Z (mm)	G (mm)	X (mm)	Y ref	C ref	Placement Grid (No. of Grid elements)
1005 [0402]	2.20	0.40	0.70	0.90	1.30	2x6
1310 [0504]	2.40	0.40	1.30	1.00	1.40	4x6
1608 [0603]	2.80	0.60	1.00	1.10	1.70	4x6
2012 [0805]	3.20	0.60	1.50	1.30	1.90	4x8
3216 [1206]	4.40	1.20	1.80	1.60	2.80	4x10
3225 [1210]	4.40	1.20	2.70	1.60	2.80	6x10
4532 [1812]	5.80	2.00	3.40	1.90	3.90	8x12
4564 [1825]	5.80	2.00	6.80	1.90	3.90	14x12

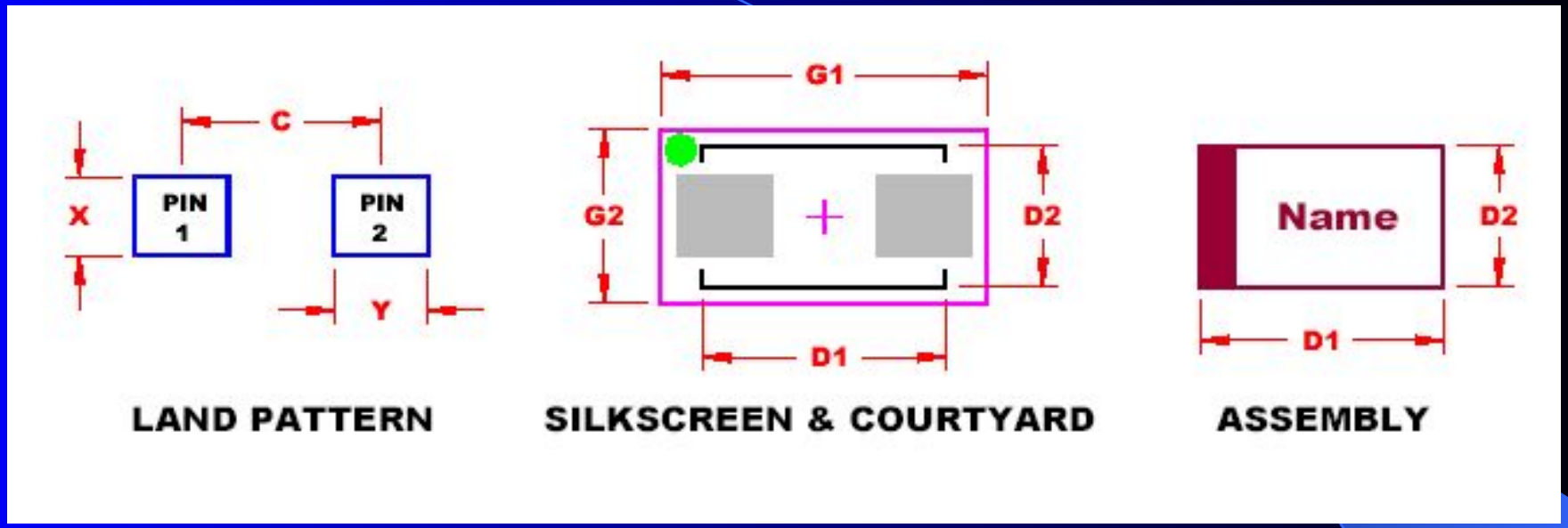
Танталовые конденсаторы





Component Identifier (mm)	L (mm)		S (mm)		W1 (mm)		W2 (mm)		T (mm)		H1 (mm)	H2 (mm)
	min	max	min	max	min	max	min	max	min	max	min	max
A 3216	3.00	3.40	0.80	1.74	1.17	1.21	1.40	1.80	0.50	1.10	0.70	1.80
B 3528	3.30	3.70	1.10	2.04	2.19	2.21	2.60	3.00	0.50	1.10	0.70	2.10
C 6032	5.70	6.30	2.50	3.54	2.19	2.21	2.90	3.50	1.00	1.60	1.00	2.80
D 7343	7.00	7.60	3.80	4.84	2.39	2.41	4.00	4.60	1.00	1.60	1.00	3.10

Посадочные места

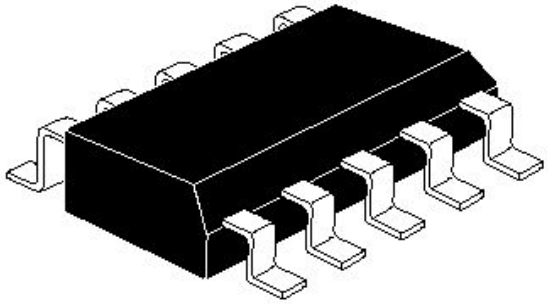


	NUE Capacitors, Tantalum Standard Range	Component						Land Pattern			Silkscreen & Assembly		Courtyard	
	Land Pattern Name	L (nom)	W2 (nom)	W1 (nom)	T (max)	H1 (max)	H2 (max)	C	X	Y	D1	D2	G1	G2
1	**CAPT2012N** (Z CASE)	2.00	1.25	0.90	0.70	0.50	1.20	1.70	1.10	1.30	2.00	1.30	3.50	1.80
2	**CAPT3216N** (A CASE)	3.20	1.60	1.20	1.10	0.70	1.80	2.50	1.40	1.70	3.20	1.60	4.70	2.10
3	**CAPT3528N** (B CASE)	3.50	2.80	2.20	1.10	0.70	2.10	2.80	2.40	1.70	3.50	2.80	5.00	3.30
4	**CAPT4726N** (M CASE)	4.70	2.60	1.40	1.10	0.80	2.30	4.00	1.60	1.70	4.70	2.60	6.20	3.10
5	**CAPT5846N** (N CASE)	5.80	4.60	2.40	1.60	1.00	3.40	4.60	2.60	2.20	5.80	4.60	7.30	5.10
6	**CAPT6032N** (C CASE)	6.00	3.20	2.20	1.60	1.00	2.80	4.80	2.40	2.20	6.00	3.20	7.50	3.70
7	**CAPT7343N** (D CASE)	7.30	4.30	2.40	1.60	1.00	3.10	6.10	2.60	2.20	7.30	4.30	8.80	4.80
8	**CAPT7343HN** (D2 CASE)	7.30	4.30	2.40	1.60	1.00	4.30	6.10	2.60	2.20	7.30	4.30	8.80	4.80
9	**CAPT7358N** (E CASE)	7.30	5.80	3.50	1.60	1.00	3.70	6.10	3.70	2.20	7.30	5.80	8.80	6.30

Корпуса микросхем

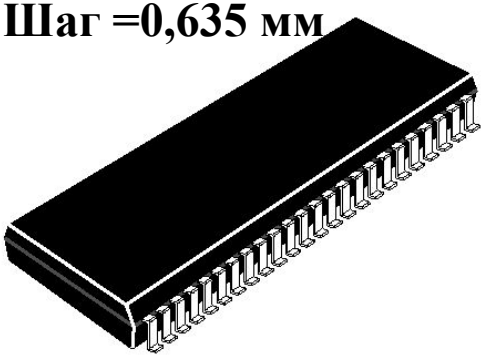
SOIC

Шаг =1,27 мм

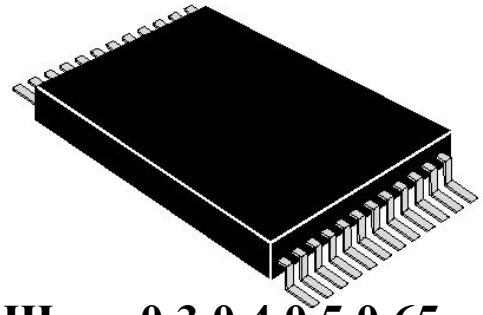


SSOIC

Шаг =0,635 мм

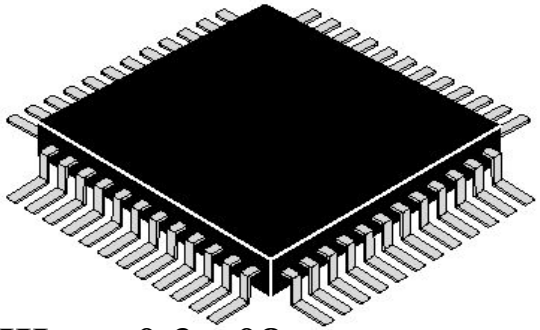


TSOP



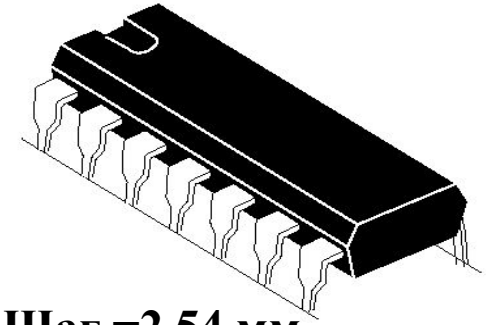
Шаг =0,3 0,4 0,5 0,65

SQFP/QFP



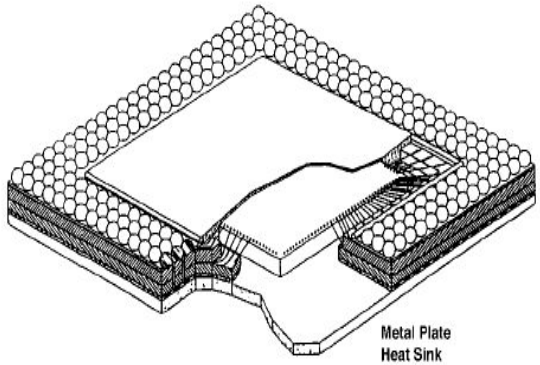
Шаг =0,3 - 08 мм

DIP



Шаг =2,54 мм

BGA

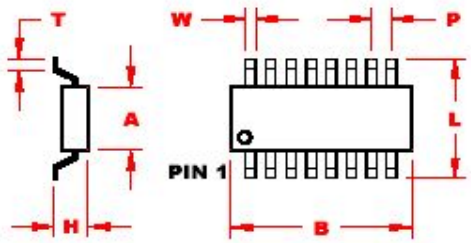


Шаг =0,5 –1,27

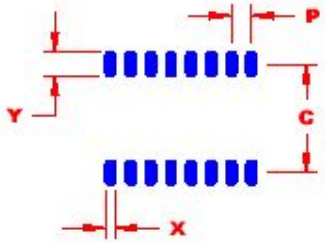
Названия корпусов

- **SOIC – Small Outline Integral Circuit**
- **SSOP – Shrink Small Outline Package**
- **TSOP – Thin Small Outline Package**
- **QFP – Quad Flat Pack ICs**
- **PLCC – Plastic Leaded Chip Carriers**
- **QFN – Quad Flat No-Lead ICs**
- **DIP – Dual in Line Package**
- **BGA – Ball Grid Arrays**

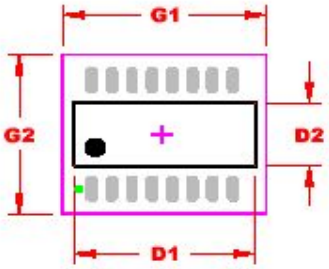
Микросхемы SOIC



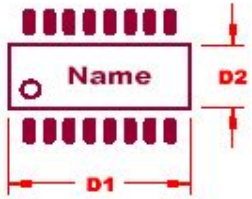
COMPONENT



LAND PATTERN



SILKSCREEN & COURTYARD

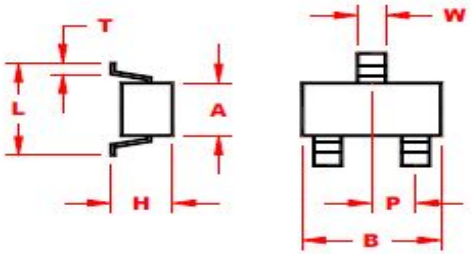


ASSEMBLY

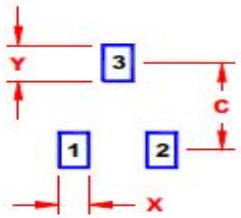
Units are in **mm** [mils]

	NUE 1.27mm [50mil] Pitch SOIC	COMPONENT						LAND PATTERN			COURTYARD		SILKSCREEN ASSEMBLY	
	Land Pattern Name	A nom	B nom	L nom	T max	W max	H max	C	X	Y	G1	G2	D1	D2
1	SO8	3.90 [154]	4.90 [193]	6.00 [236]	1.27 [50]	0.51 [20]	1.75 [69]	4.90 [193]	0.60 [24]	2.10 [83]	5.40 [213]	7.50 [295]	4.90 [193]	2.00 [79]
2	SO8RP	5.60 [220]	5.00 [197]	8.00 [315]	0.70 [28]	0.51 [20]	1.90 [75]	7.50 [295]	0.60 [24]	1.60 [63]	5.50 [217]	9.60 [378]	5.00 [197]	5.10 [201]
3	SO8W	7.50 [295]	5.25 [207]	10.30 [406]	1.04 [41]	0.51 [20]	2.65 [104]	9.40 [370]	0.60 [24]	1.90 [75]	5.80 [228]	11.80 [465]	5.30 [209]	6.70 [264]
4	SO14	3.90 [154]	8.65 [341]	6.00 [236]	1.27 [50]	0.51 [20]	1.75 [69]	4.90 [193]	0.60 [24]	2.10 [83]	9.20 [362]	7.50 [295]	8.70 [343]	2.00 [79]
5	SO14RP	5.60 [220]	10.00 [394]	7.60 [299]	0.70 [28]	0.51 [20]	2.03 [80]	7.10 [280]	0.60 [24]	1.60 [63]	10.50 [413]	9.20 [362]	10.00 [394]	4.70 [185]
6	SO14W	7.50 [295]	9.00 [354]	10.30 [406]	1.04 [41]	0.51 [20]	2.65 [104]	9.40 [370]	0.60 [24]	1.90 [75]	9.50 [374]	11.80 [465]	9.00 [354]	6.70 [264]
7	SO16	3.90 [154]	9.90 [390]	6.00 [236]	1.27 [50]	0.51 [20]	1.75 [69]	4.90 [193]	0.60 [24]	2.10 [83]	10.40 [409]	7.50 [295]	9.90 [390]	2.00 [79]
8	SO16RP	5.60 [220]	11.20 [441]	7.60 [299]	0.70 [28]	0.51 [20]	2.03 [80]	7.10 [280]	0.60 [24]	1.60 [63]	11.70 [461]	9.20 [362]	11.20 [441]	4.70 [185]

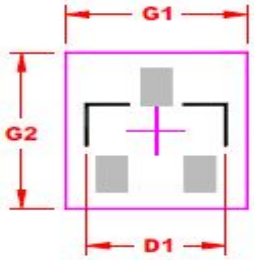
SOT-23, SOT-23-6



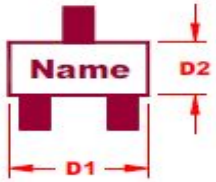
COMPONENT



LAND PATTERN

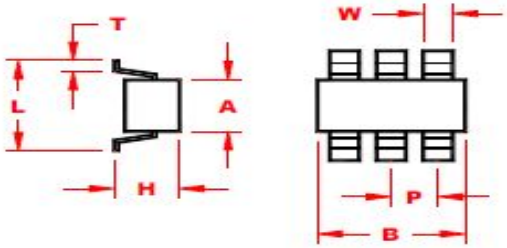


SILKSCREEN & COURTYARD

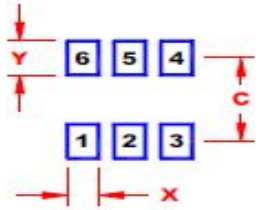


ASSEMBLY

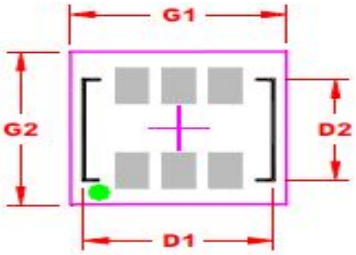
NUE SOT-23		Component							Land Pattern			Silkscreen & Assembly		Courtyard	
	Land Pattern Name	P	A (nom)	B (nom)	L (nom)	T (max)	W (max)	H (max)	C	X	Y	D1	D2	G1	G2
1	SOT-23N	0.95	1.30	2.90	2.45	0.60	0.50	1.10	2.10	0.60	1.50	2.90	1.30	3.40	4.10



COMPONENT



LAND PATTERN

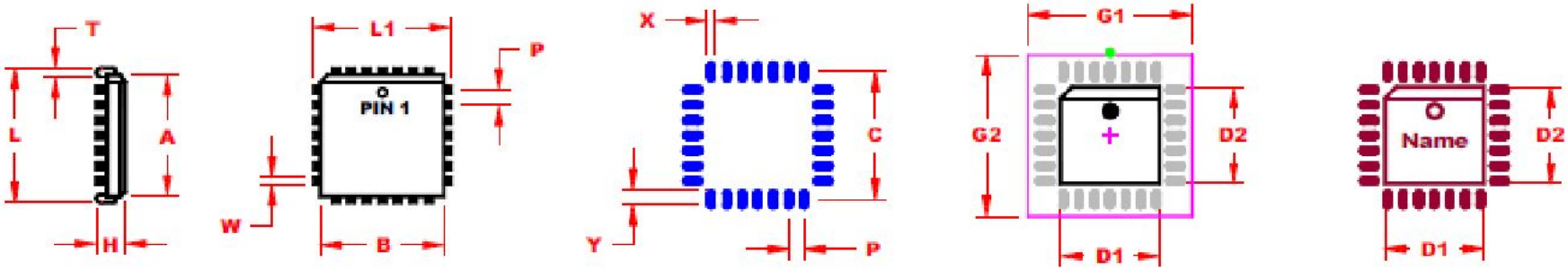


SILKSCREEN & COURTYARD

ASSEMBLY

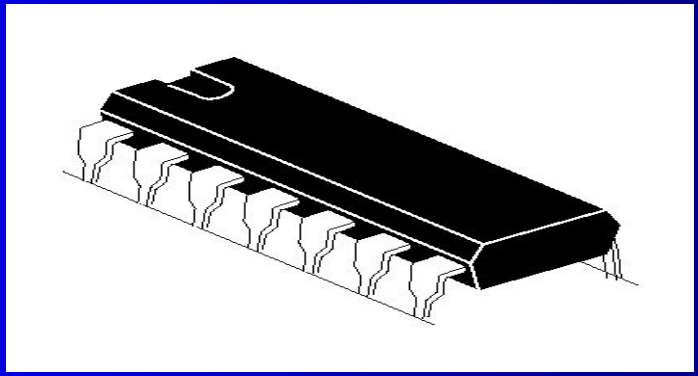
NUE SOT-23-6		Component							Land Pattern			Silkscreen & Assembly		Courtyard	
	Land Pattern Name	P	A (nom)	B (nom)	L (nom)	T (max)	W (max)	H (max)	C	X	Y	D1	D2	G1	G2
1	SOT-23-6N	0.95	1.60	2.90	2.85	0.55	0.50	1.45	2.50	0.60	1.40	2.90	2.90	3.40	4.40

Квадратные PLCC

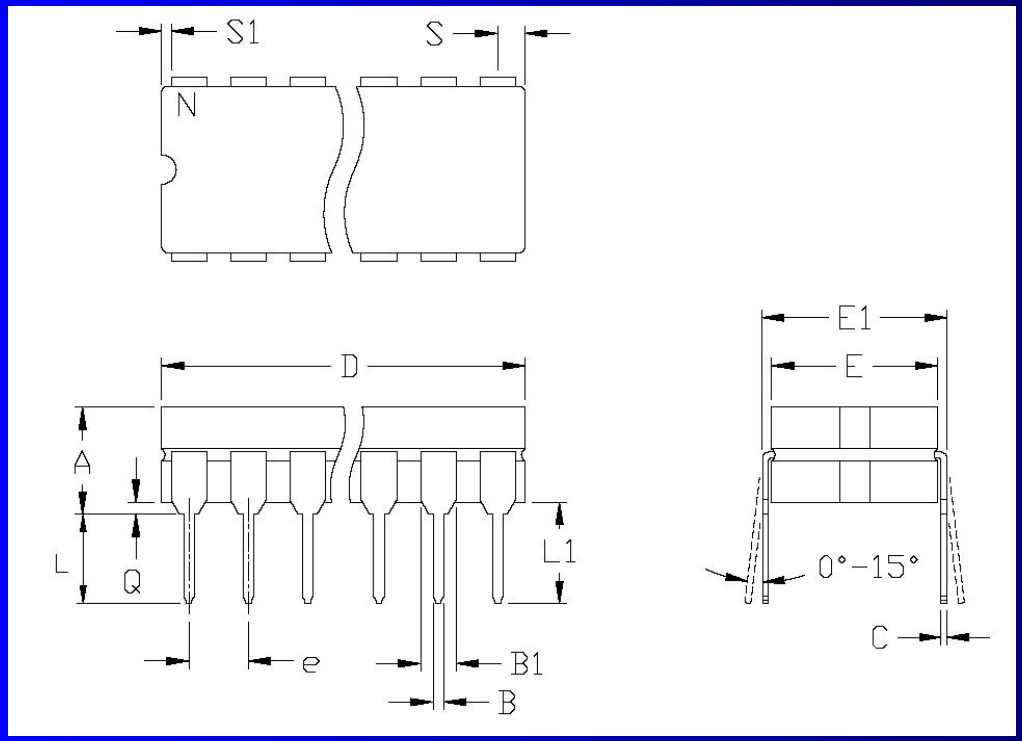


	NUE 1.27mm Square PLCC	Component						Land Pattern			Silkscreen Assembly	Courtyard
	Land Pattern Name	P	A & B	L1 & L2 (nom)	T (max)	W (max)	H (max)	C1 & C2	X	Y	D1 & D2	G1 & G2
1	PLCC-20N	1.27	9.00	9.90	1.80	0.53	4.57	8.30	0.60	2.20	5.30	11.70
2	PLCC-28N	1.27	11.60	12.45	1.80	0.53	4.57	10.90	0.60	2.20	7.90	14.30
3	PLCC-44N	1.27	16.70	17.53	1.80	0.53	4.57	15.90	0.60	2.20	12.90	19.30
4	PLCC-52N	1.27	19.20	20.07	1.80	0.53	5.08	18.50	0.60	2.20	15.50	21.90
5	PLCC-68N	1.27	24.30	25.15	1.80	0.53	5.08	23.60	0.60	2.20	20.60	27.00
6	PLCC-84N	1.27	29.40	30.23	1.80	0.53	5.08	28.60	0.60	2.20	25.60	32.00
7	PLCC-100N	1.27	34.30	35.40	1.80	0.53	5.08	33.80	0.60	2.20	30.80	37.20
8	PLCC-124N	1.27	42.10	42.93	1.80	0.53	5.08	41.30	0.60	2.20	38.30	44.70

Корпуса DIP



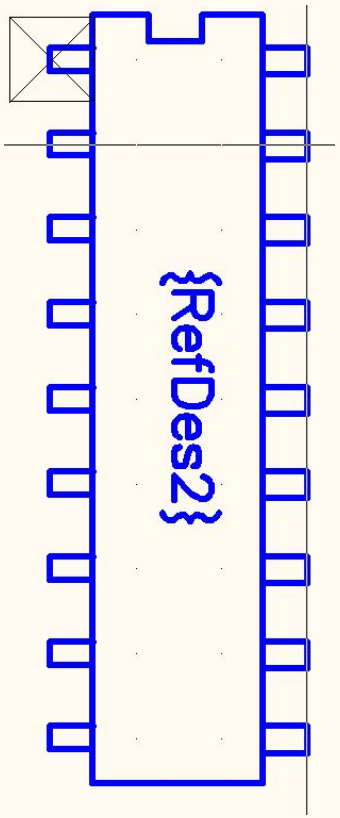
	MILLIMETERS			
	MIN	MAX	N	CASE
D	---	10.29	8	P:D4
D	---	19.94	14	C:D1
D	---	21.34	16	E:D2
D	---	24.38	18	V:D6
D	---	26.92	20	R:D8
D	---	32.51	24	L:D9



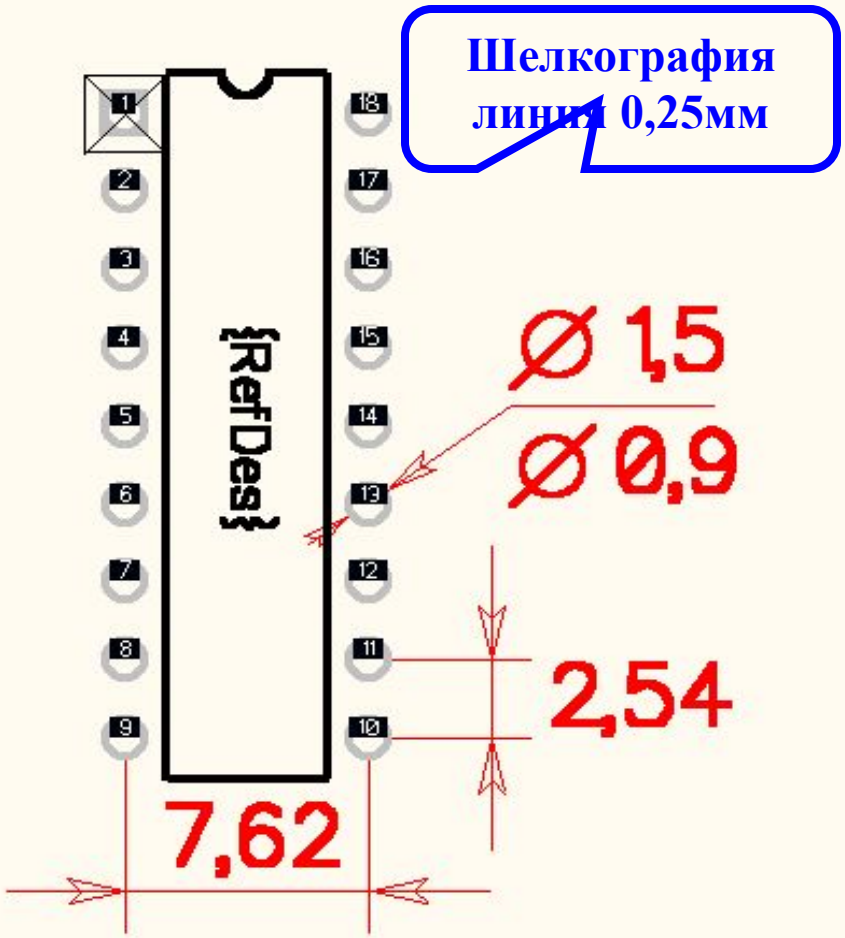
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

Посадочное место стандартный (узкий) DIP

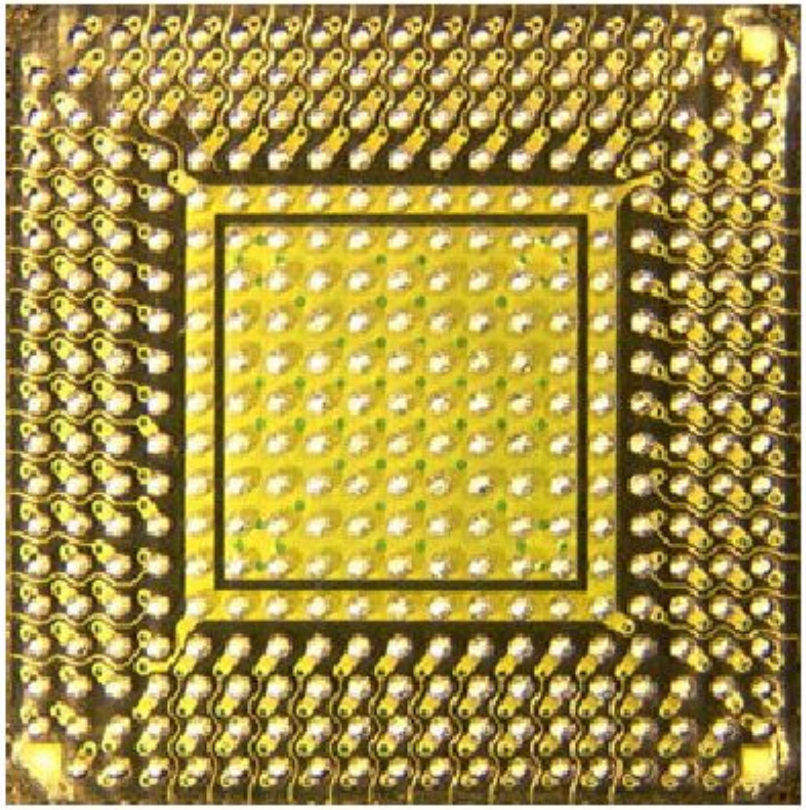
Слой Top Assy



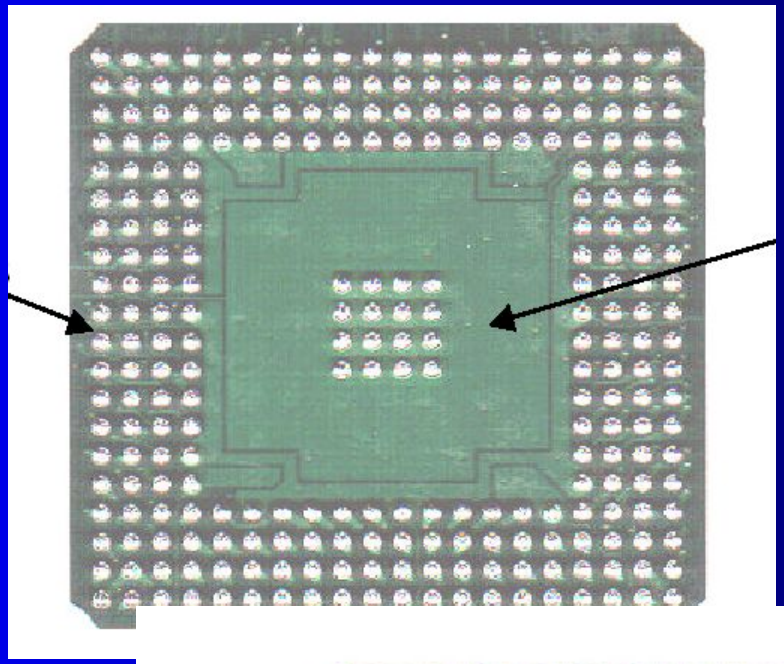
Остальные слои



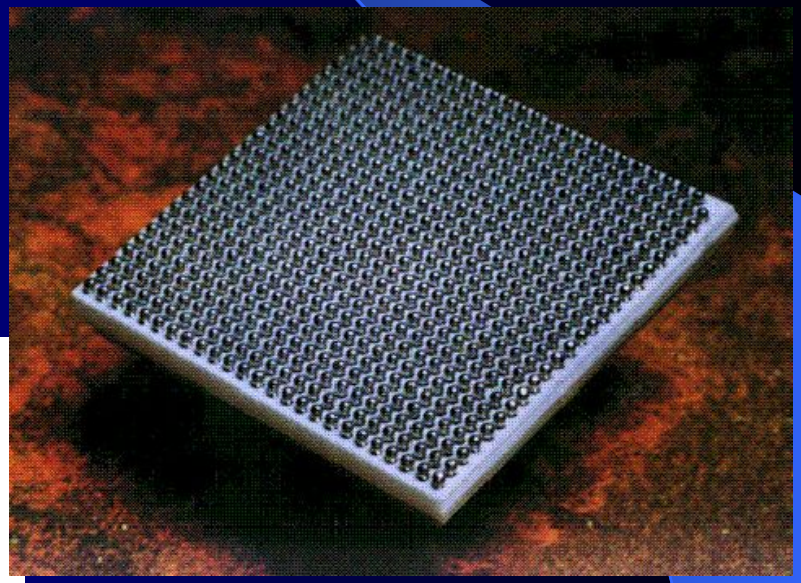
Plastic Ball Grid Array (PBGA) 357 выводов (19x19)

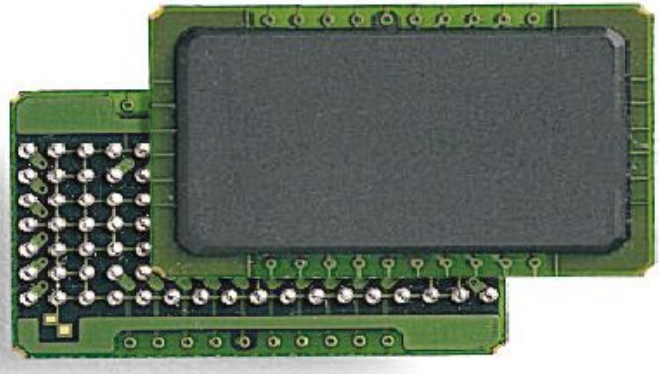


Периферийные площадки



Термальные площадки

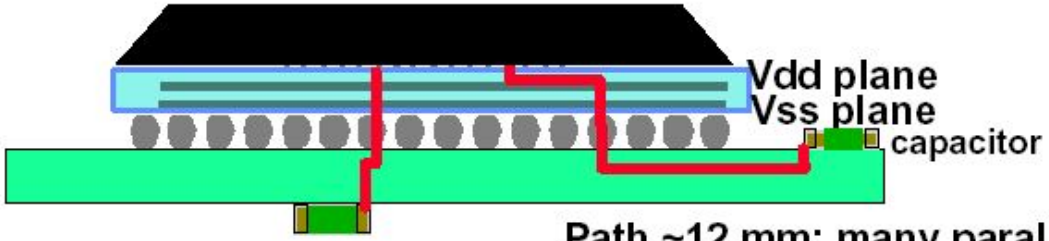




Преимущества BGA корпусов

Lower Inductance in Power Supply paths

Means Lower Switching Noise



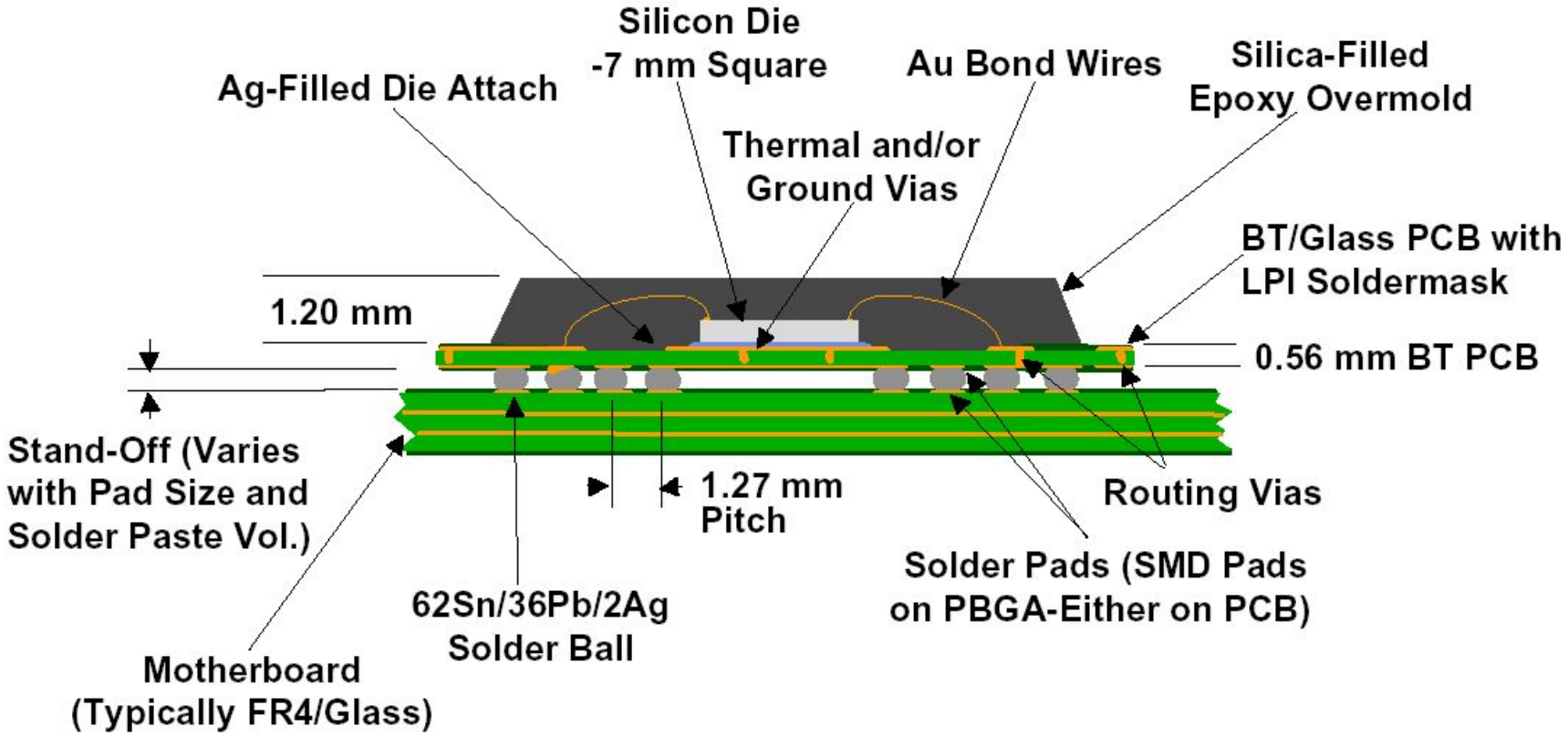
Path ~3.5 mm:
Low Inductance

Path ~12 mm: many parallel paths through reference planes: Low Inductance

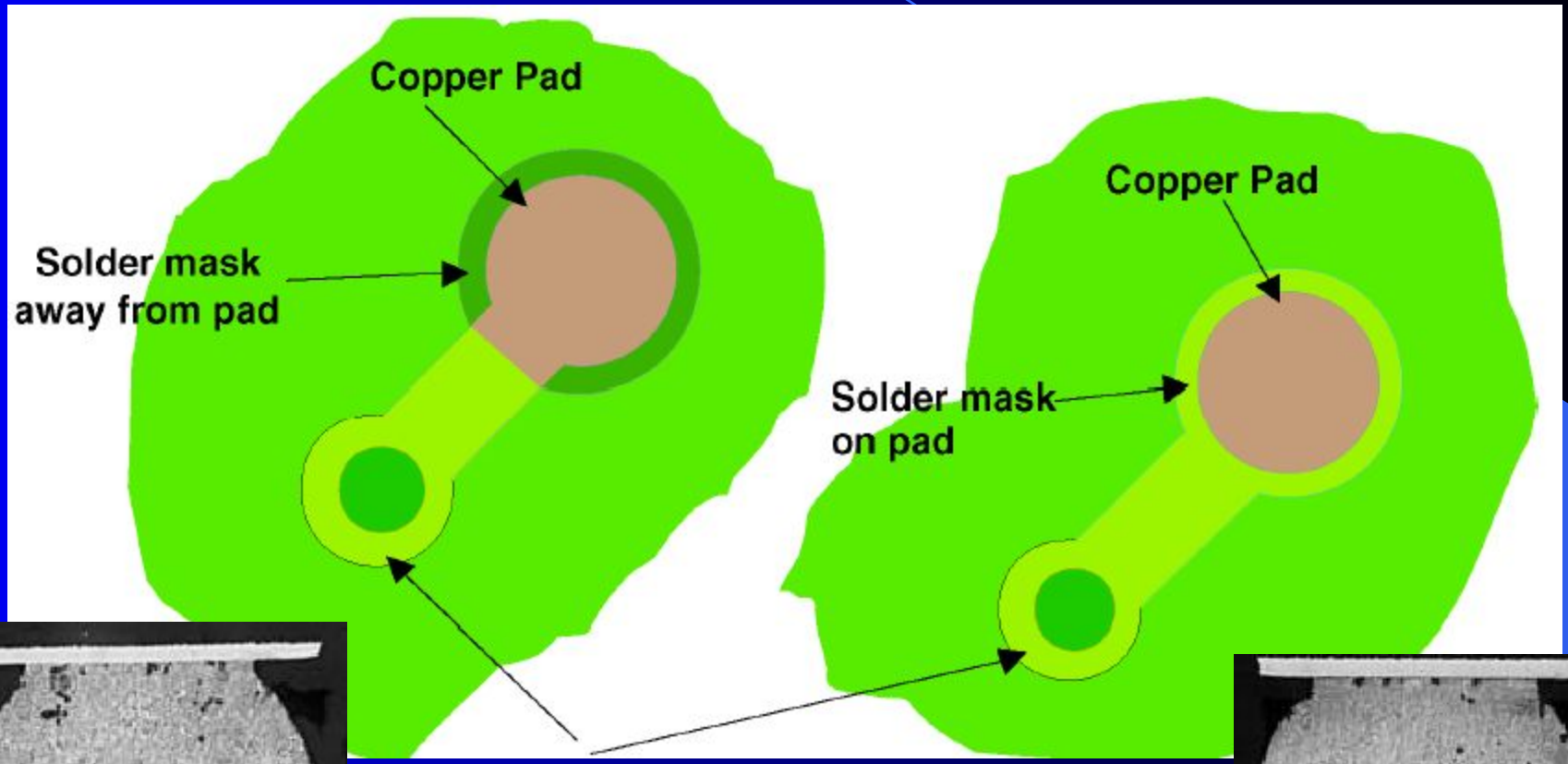
40 mm perimeter leaded package

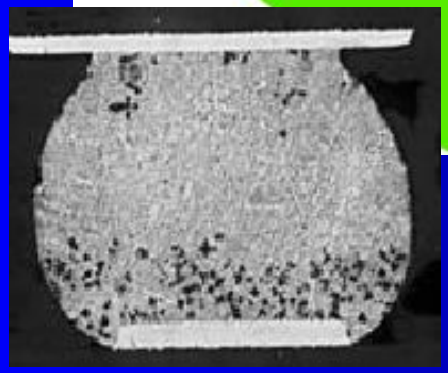
Path ~ 20mm less coupled to signal currents resulting in higher inductance

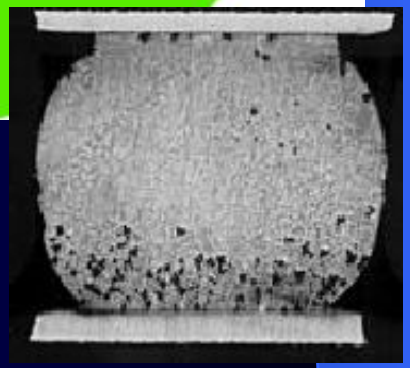
Конструкция PBGA



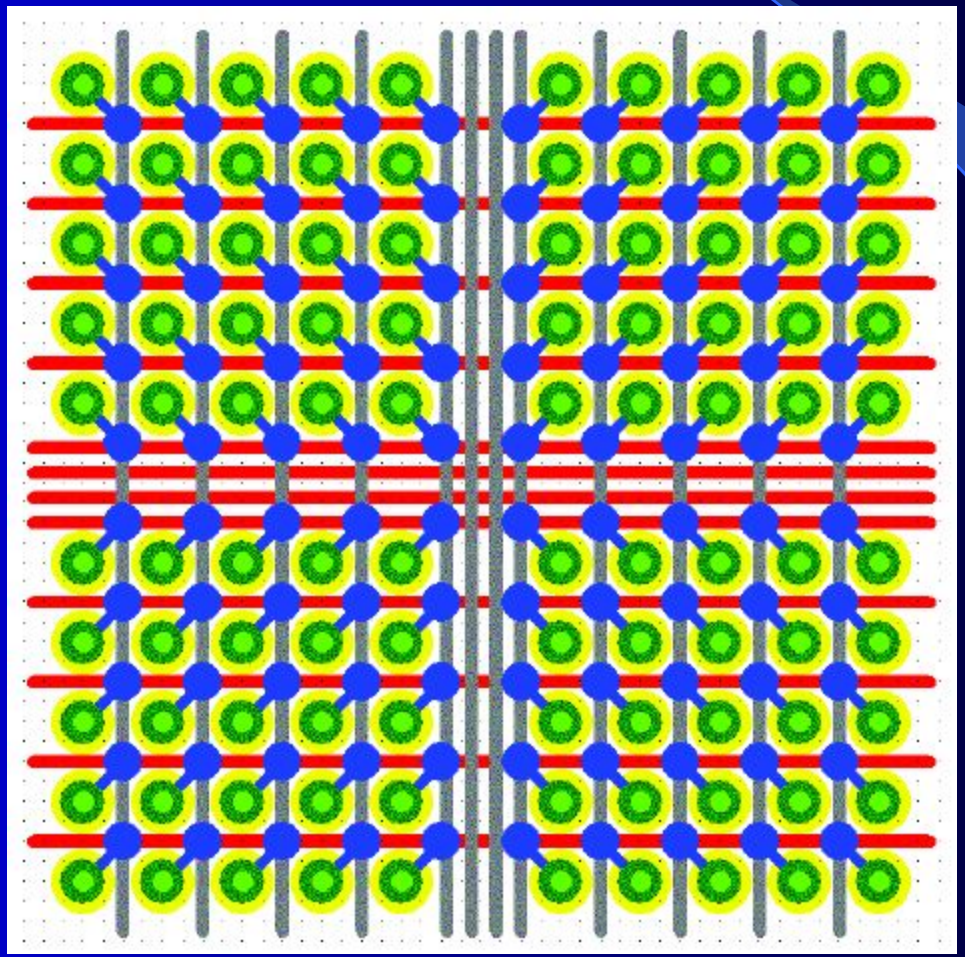
Два варианта площадок BGA





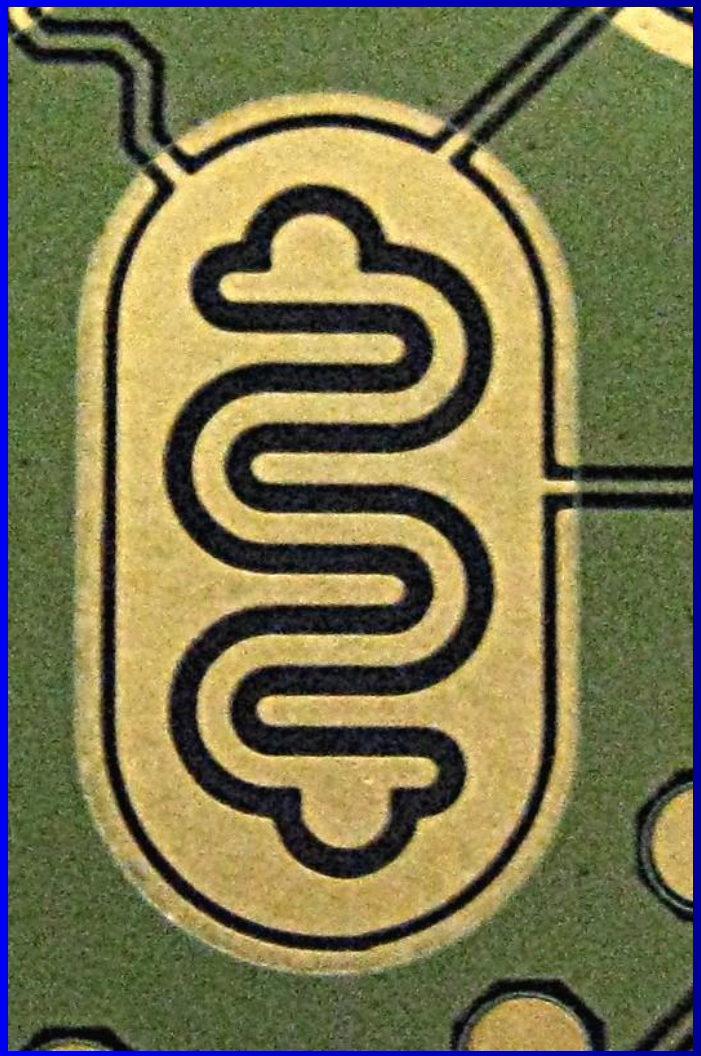


Сложная трассировка BGA

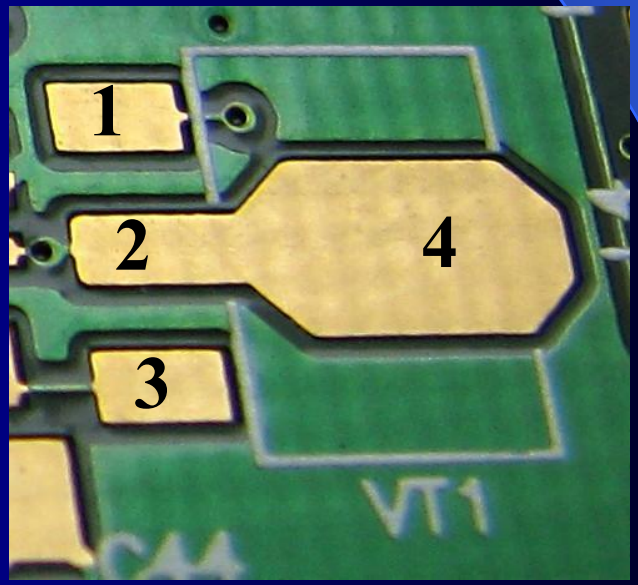


Конструктивные особенности

- **Сложная форма вывода или площадки**

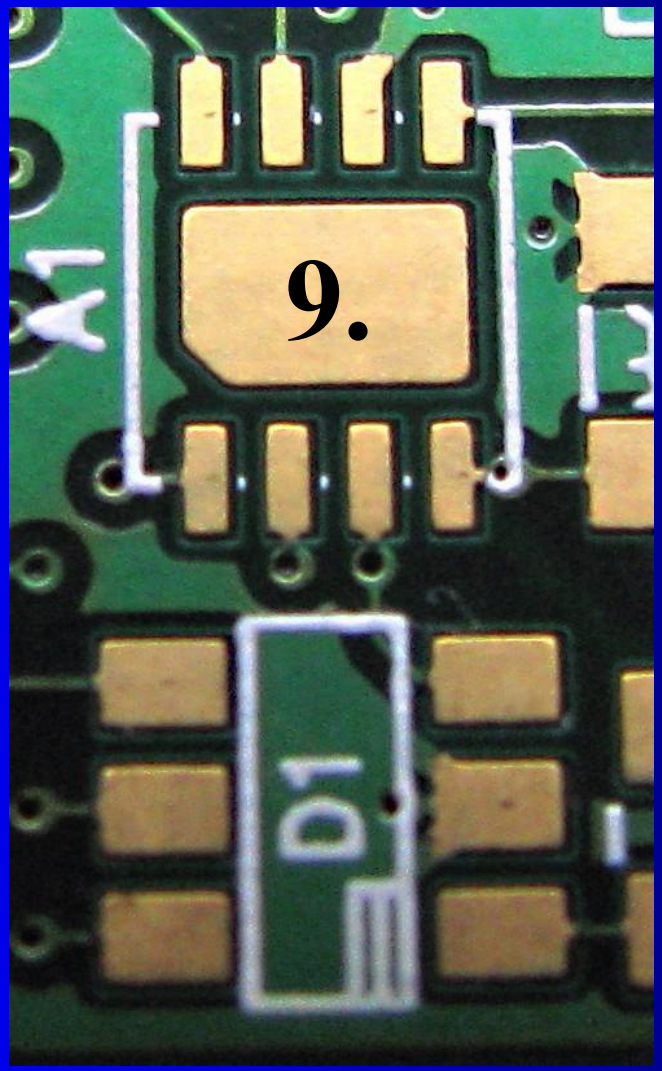


Слияние выводов на топологии



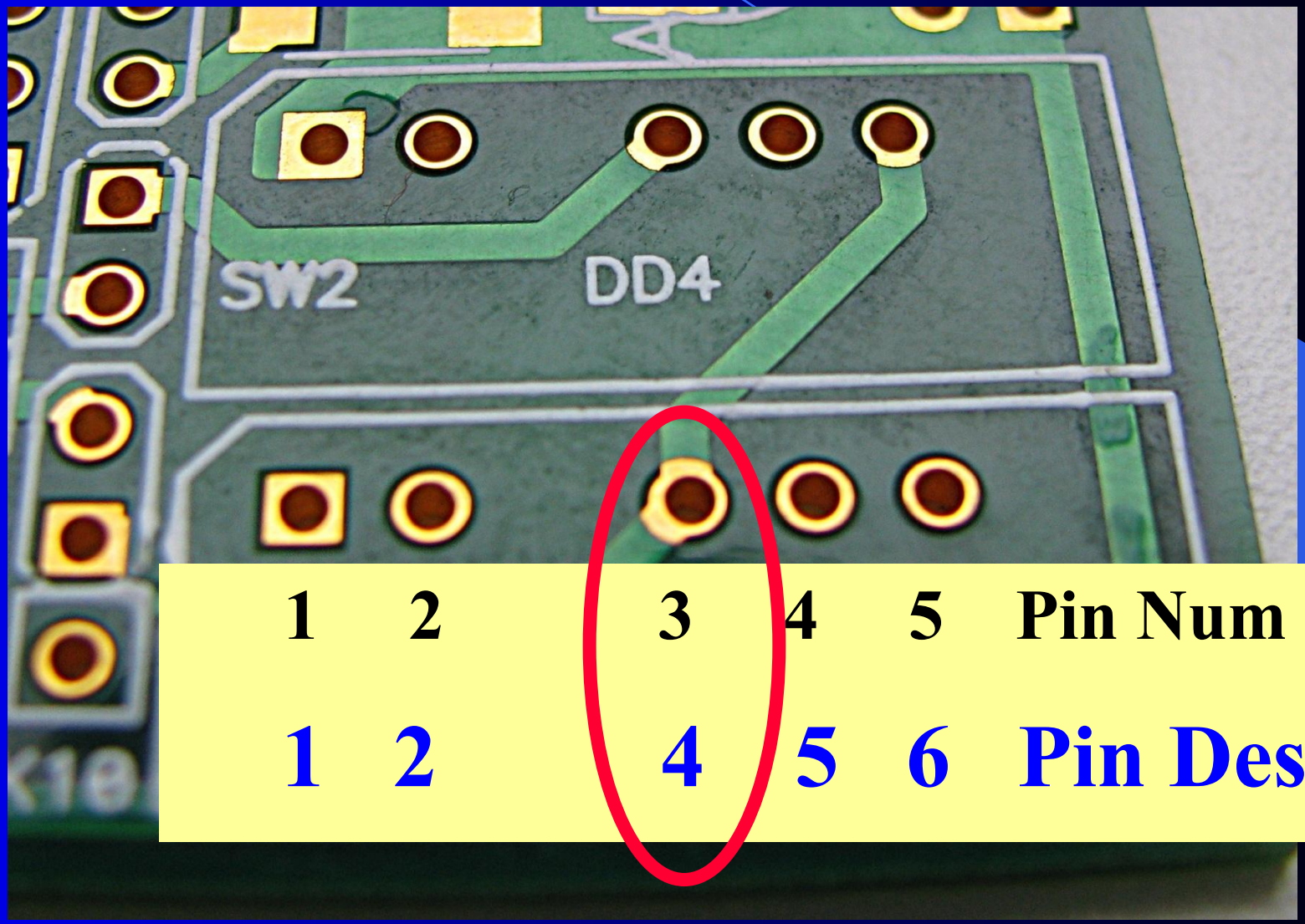
Конструктивные особенности

Дополнительные выводы и точки крепления



Конструктивные особенности

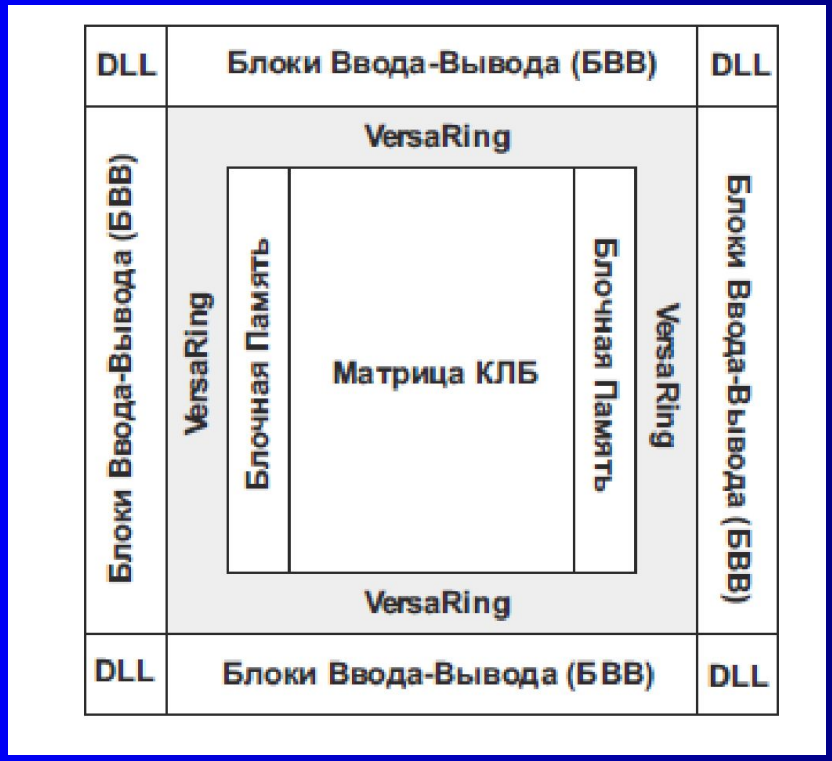
Пропущенные выводы

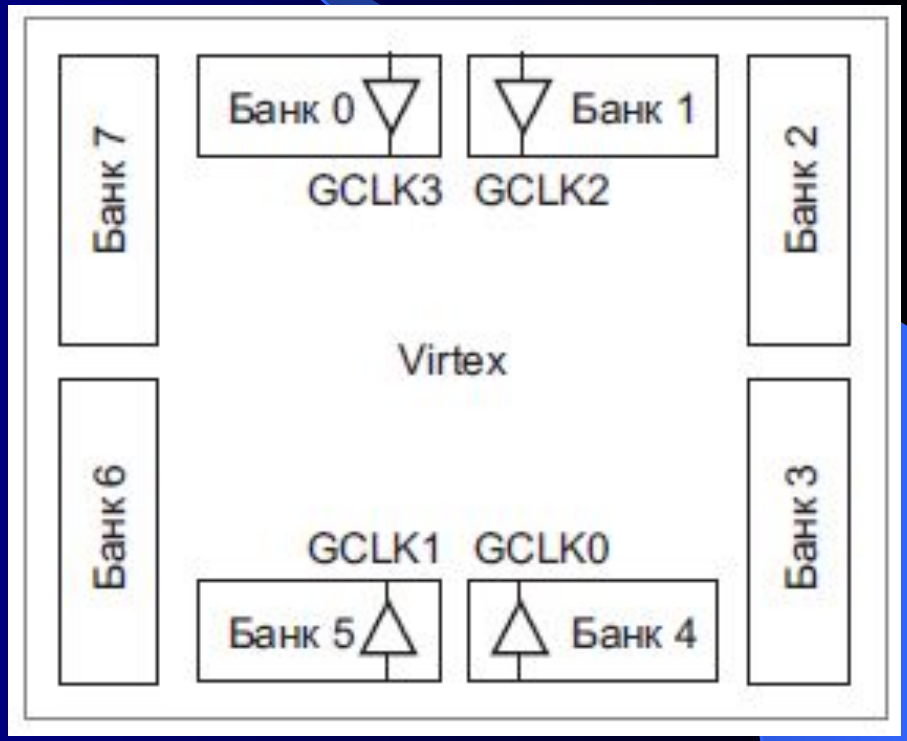


CPLD, FPGA

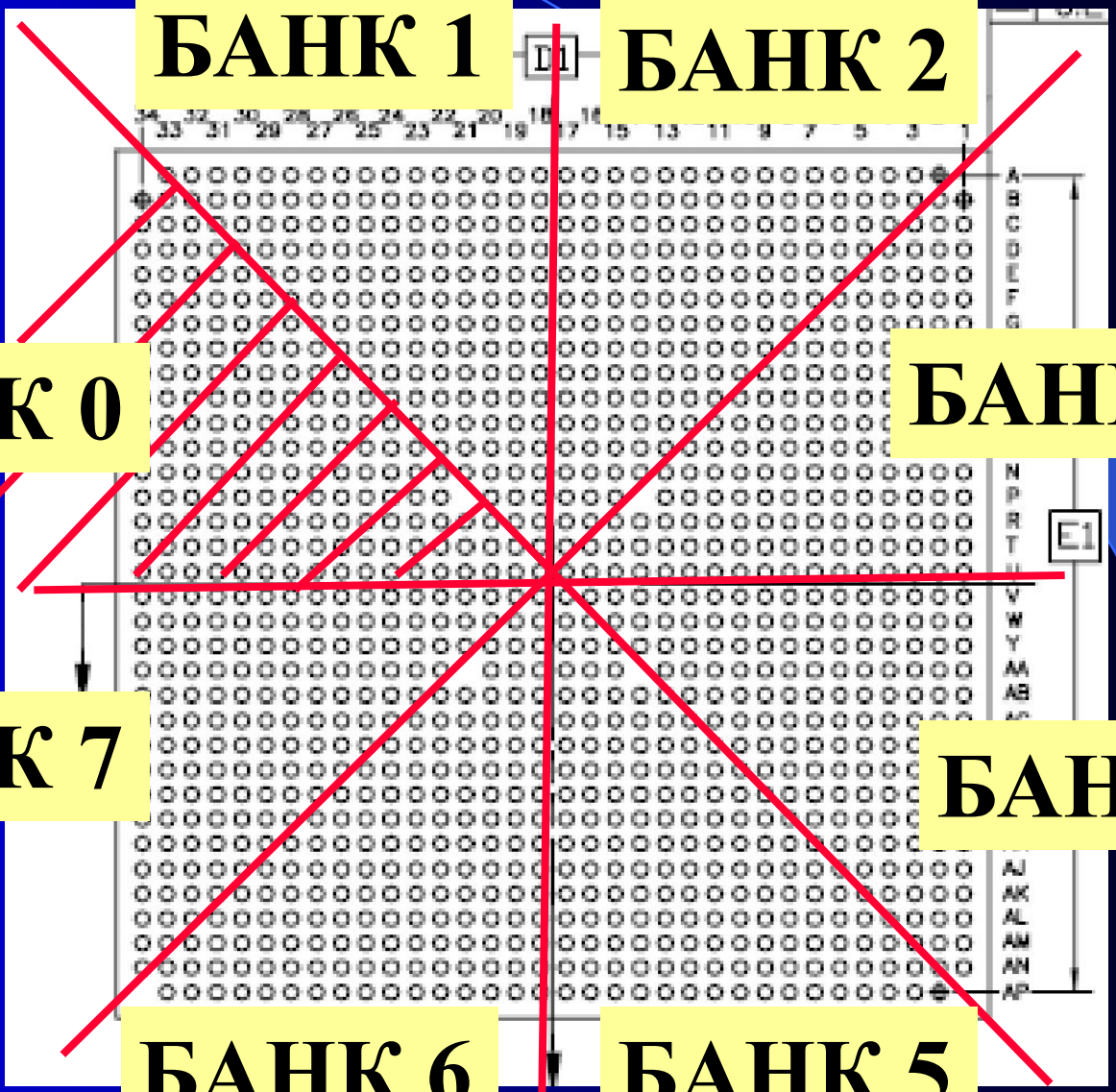
- **FPGA - field-programmable gate array (ПЛМ – программируемая логическая матрица)**
- **CPLD -complex programmable logic device (ПЛИС – программируемая логическая интегральная схема)**

Архитектура ПЛИС Virtex





BGA Корпус 1148 выводов



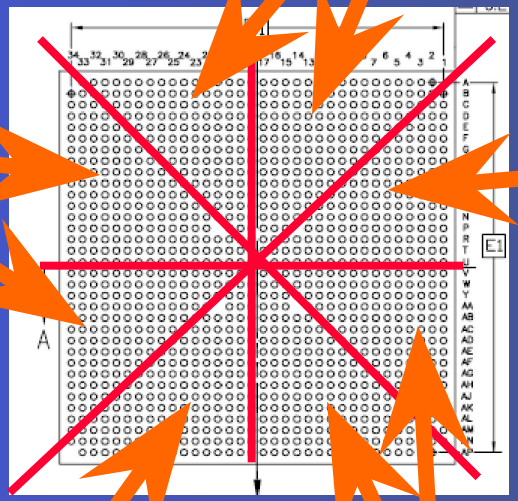
Взаимосвязь размещения элементов на плате и схемы FPGA

RAM

RAM

RAM

Выходной Буфер Данных



Панели Индикации

FLASH Память

Входной Буфер Данных