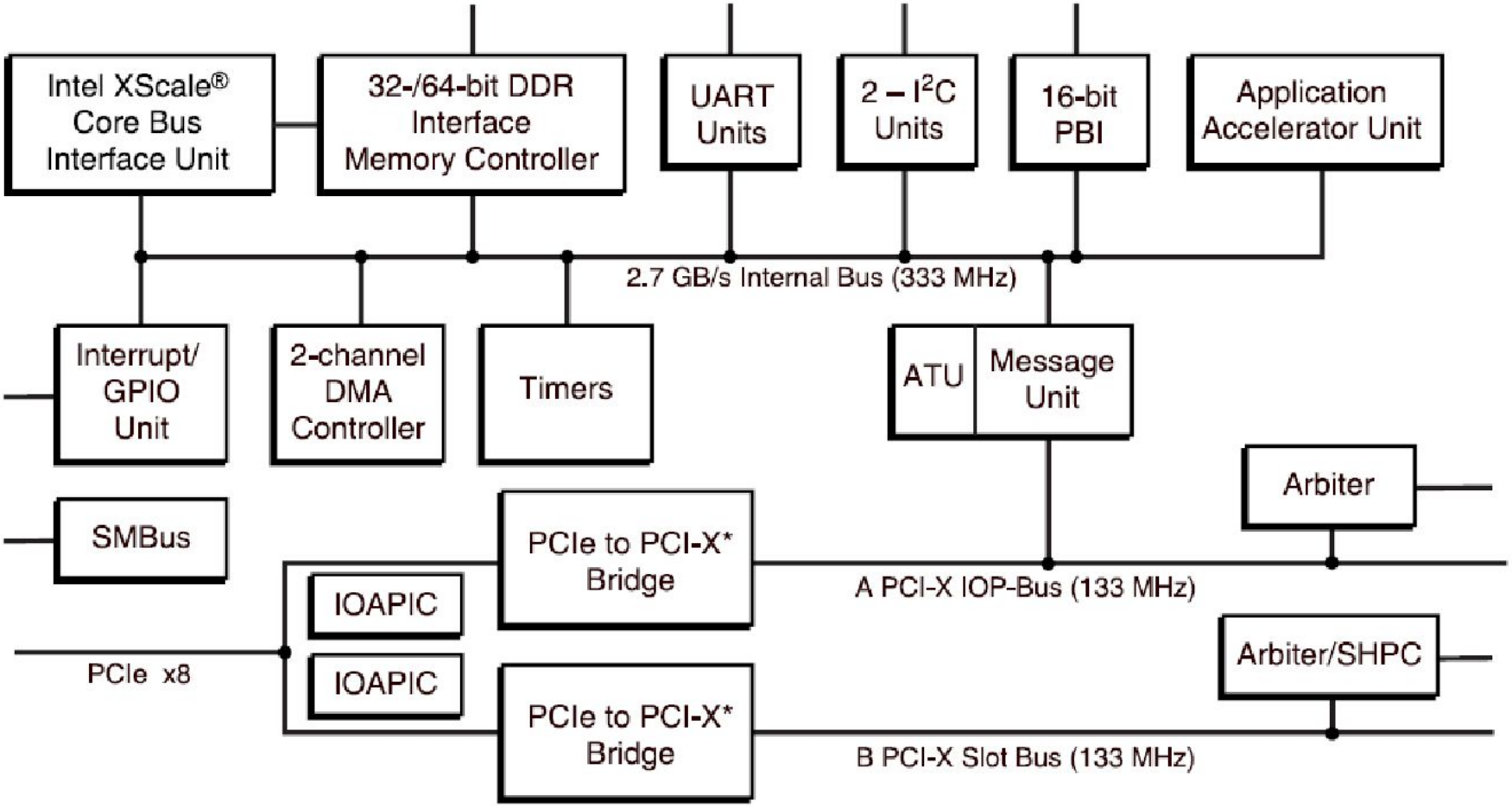
Intel® 80333 I/O Processor



1. **The 80333 core processor is based upon the Intel XScale® core. The core processor operates at a maximum frequency of 800 MHz. The instruction cache is 32 Kbytes in size and is 32-way set associative. Also, the core processor includes a data cache that is 32 Kbytes and is 32-way set associative and a mini data cache that is 2 Kbytes and is 2-way set associative.**
2. **An Address Translation Unit (ATU) allows PCI transactions direct access to the 80333 local memory. The Address Translation Unit supports transactions between PCI address space and80333 address space. Address translation for the ATU is controlled through programmable registers accessible from both the PCI interface and the Intel XScale® core.**
3. **The Messaging Unit (MU) provides data transfer between the 80333 and PCI-Express system. It uses interrupts to notify each system when new data arrives. The MU has four messaging mechanisms: Message Registers, Doorbell Registers, Circular Queues and Index Registers. Each allows a host processor or external PCI device and the 80333 to communicate through message passing and interrupt generation.**

4. **The DMA Controller allows low-latency, high-throughput data transfers between PCI bus agents and the local memory. Two separate DMA channels accommodate data transfers to the PCI bus. Both channels include a local memory to local memory transfer mode. The DMA Controller supports chaining and unaligned data transfers. It is programmable through the Intel XScale® core only.**
5. **The 80333 includes 8 General Purpose I/O (GPIO) pins.**
6. **The Memory Controller allows direct control of a DDR SDRAM memory subsystem. It features programmable chip selects and support for error correction codes (ECC). The memory controller can be configured for DDR SDRAM at 333 MHz and DDR-II at 400 MHz. The memory controller supports pipelined access and arbitration control to maximize performance. The memory controller is dual-ported, with a dedicated interface for the Intel XScale® core Bus Interface Unit and a second interface to the Internal Bus. The memory controller interface configuration support includes Unbuffered DIMMs, Registered DIMMs, and discrete DDR SDRAM devices.**

7. **The Application Accelerator Unit (AA)** provides low-latency, high-throughput data transfer capability between the AA unit, the 80333 local memory and the PCI bus. It executes data transfers from and to the 80333 local memory, from the PCI bus to the 80333 local memory, or from the 80333 local memory to the PCI bus. The AA unit performs XOR operations, computes parity, generates and verifies an eight byte Data Integrity field, performs memory block fills, and provides the necessary programming interface. The AA unit in the 80333 has been enhanced to support RAID 6 functionality.