

Модель прерываний в IA-64

IA-64 Interruption Model

- Parallel instruction execution, . . .
 - Exception delivery is sequential & precise
 - All exceptions reported on the excepting instruction (including numeric exceptions)
- “Interruption” is IA-64 term for...

Abort	Fault	Trap	Interrupt
<ul style="list-style-type: none">• Hardware reset• Machine check	Exception taken <u>before</u> instruction commit, e.g. TLB miss	Exception taken <u>after</u> instruction commit, e.g. FP trap	Asynchronous external event: <ul style="list-style-type: none">• device or platform management interrupt• soft-reset

*IA-64 Provides Precise Exception Model
To Match Today's OS Designs*

Модель прерываний в IA-64

IA-64 Interruption Process

Normal Instruction Execution Flow:
• *Instruction A executed*

Application Code

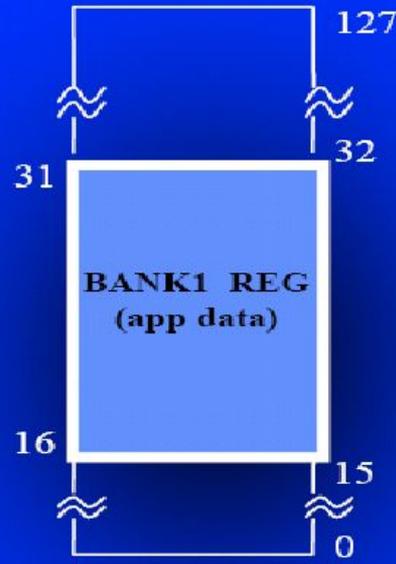
IP →	0x1000	INST A
	0x1010	INST B
	0x1020	INST C
	⋮	⋮

IVT Code

0x4000	INST X
0x4010	INST Y
0x4020	RFI
⋮	⋮

Current Processor State

IP	0x1000
PSR	



Interruption Registers

IIP	
IPSR	
⋮	
⋮	

Модель прерываний в IA-64

IA-64 Interruption Process

Normal Instruction Execution Flow:

- *Instruction B executed*

Application Code

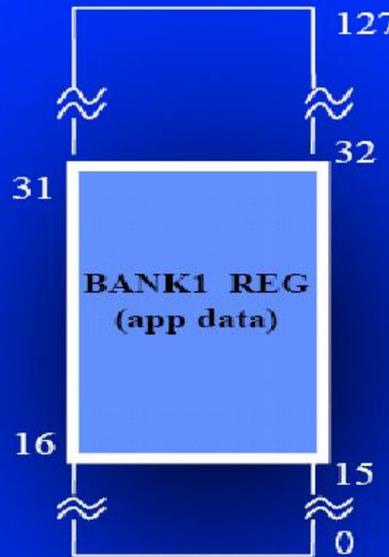
<i>IP</i> →	0x1000	INST A
	0x1010	INST B
	0x1020	INST C
	⋮	⋮

IVT Code

	0x4000	INST X
	0x4010	INST Y
	0x4020	RFI
	⋮	⋮

Current Processor State

<i>IP</i>	0x1010
<i>PSR</i>	



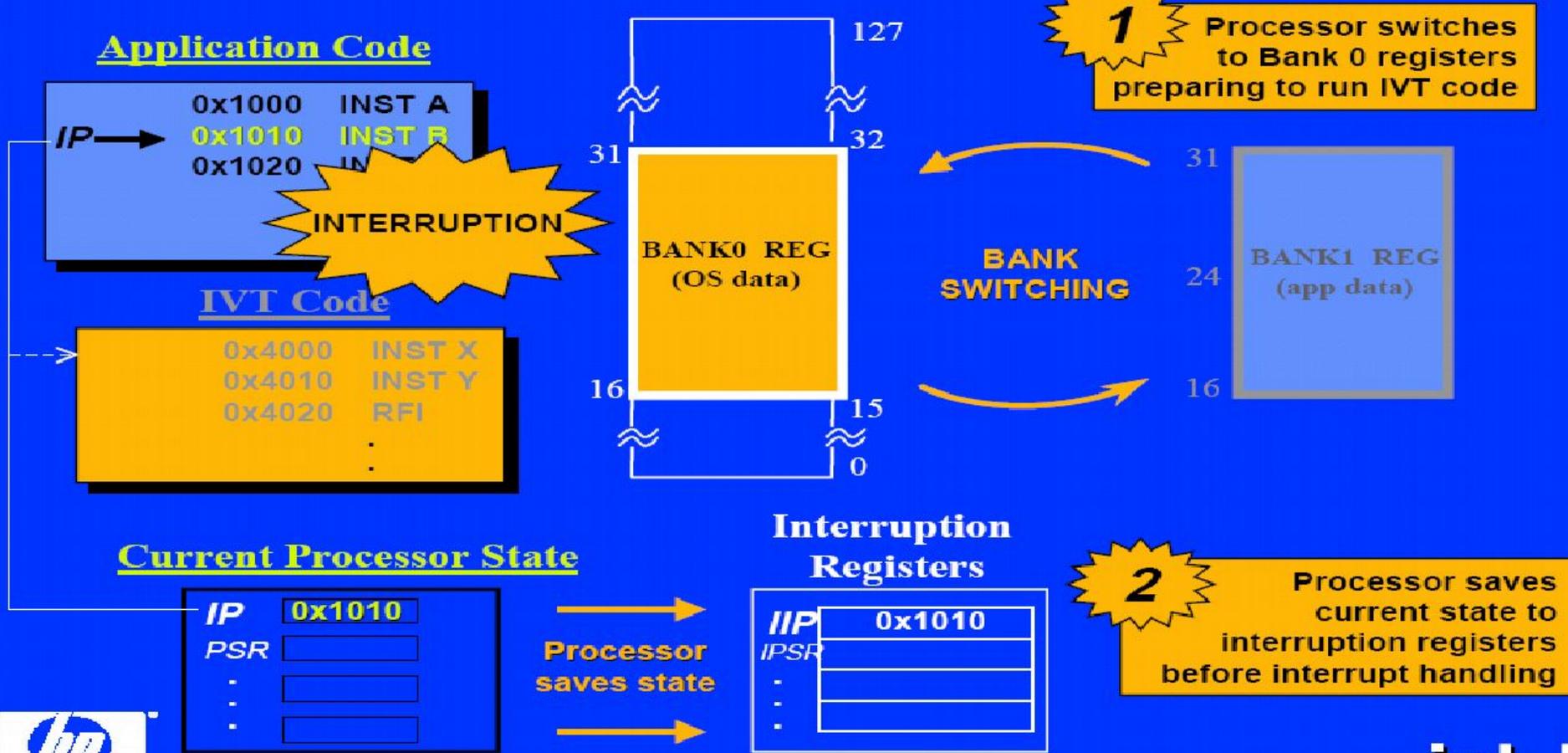
Interruption Registers

<i>IIP</i>	
<i>IPSR</i>	
⋮	
⋮	

Модель прерываний в IA-64

IA-64 Interruption Process

Interruption Delivery



Модель прерываний в IA-64

IA-64 Interruption Process

Interruption Handling

- *Instruction X* executed in interrupt vector table

Application Code

0x1000	INST A
0x1010	INST B
0x1020	INST C
⋮	⋮

Interrupt Vector Table (IVT) Code

<i>IP</i> → 0x4000	INST X
0x4010	INST Y
0x4020	RFI
⋮	⋮

Current Processor State

<i>IP</i>	0x4000
<i>PSR</i>	
⋮	
⋮	



Interruption Registers

<i>IIP</i>	0x1010
<i>IPSR</i>	
⋮	
⋮	



Модель прерываний в IA-64

IA-64 Interruption Process

Interruption Handling
• *Instruction Y executed in interrupt vector table*

Application Code

0x1000	INST A
0x1010	INST B
0x1020	INST C
⋮	⋮

IVT Code

$IP \rightarrow$	0x4000	INST X
	0x4010	INST Y
	0x4020	RFI
	⋮	⋮

Current Processor State

IP	0x4010
PSR	
⋮	
⋮	

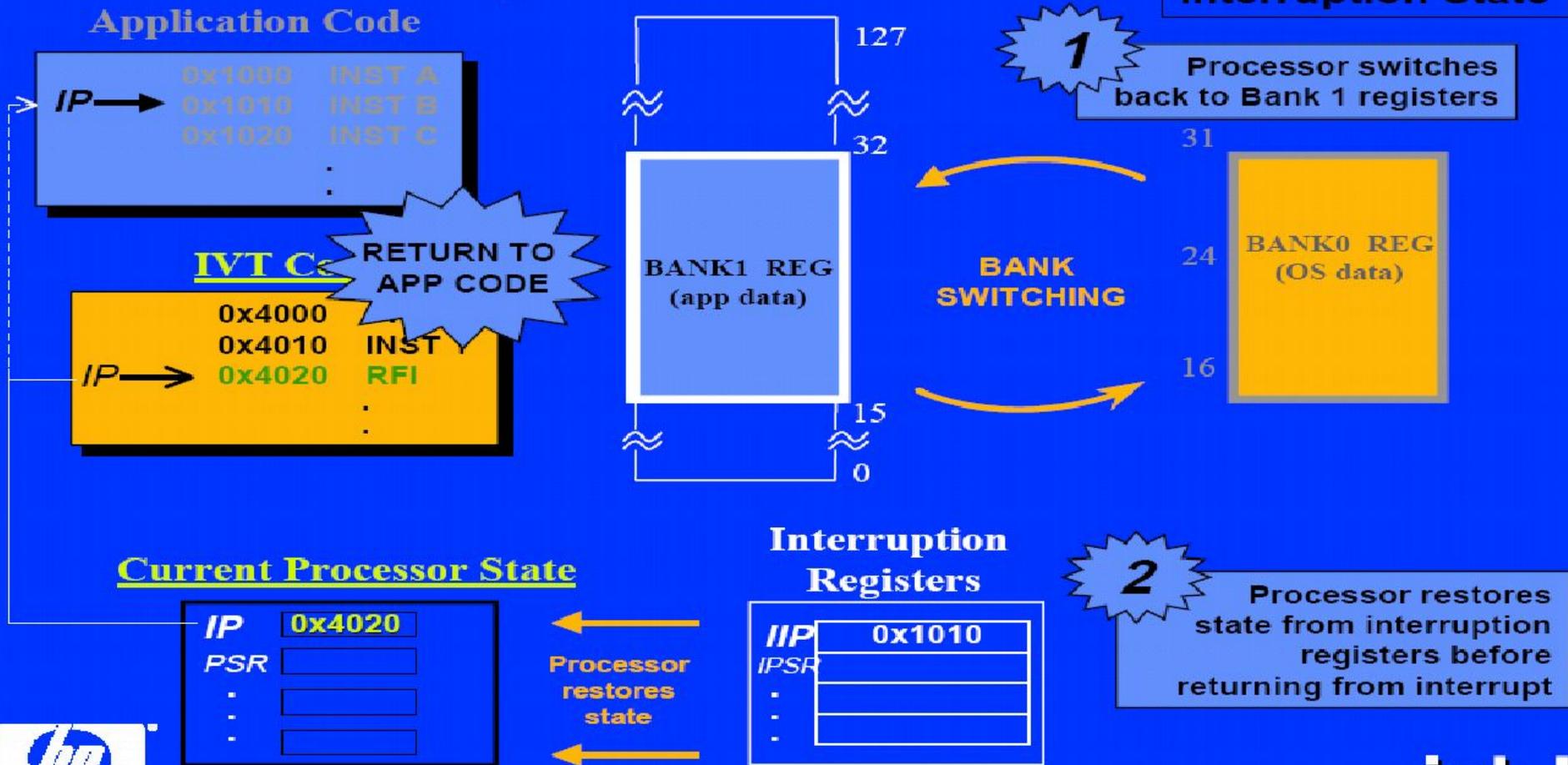


Interruption Registers

IIP	0x1010
$IPSR$	
⋮	
⋮	

Модель прерываний в IA-64

IA-64 Interruption Process



Модель прерываний в IA-64

IA-64 Interruption Process

Resume Normal Instruction Execution:

- *Instruction B executed*

Application Code

<i>IP</i> →	0x1000	INST A
	0x1010	INST B
	0x1020	INST C
	⋮	⋮

IVT Code

	0x4000	INST X
	0x4010	INST Y
	0x4020	RFI
	⋮	⋮

Current Processor State

<i>IP</i>	0x1010
<i>PSR</i>	



Interruption Registers

<i>IIP</i>	
<i>IPSR</i>	
⋮	
⋮	