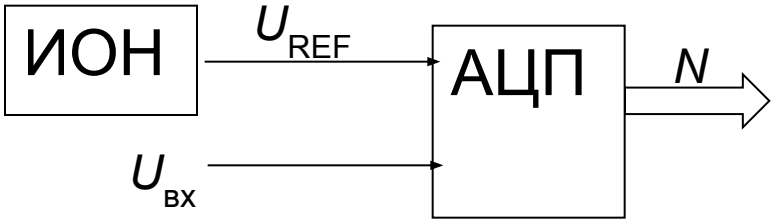
ЦИФРОВАЯ ИЗМЕРИТЕЛЬНАЯ ТЕХНИКА

ГЛАВА 4: ЦИТ В ОБЛАСТИ ЭЛЕКТРИЧЕСКИХ СИГНАЛОВ И ЦЕПЕЙ
ЧАСТЬ 3

В.Г. Кнорринг

АНАЛОГО-ЦИФРОВЫЕ ПРЕОБРАЗОВАТЕЛИ – АЦП



АЦП, как и ЦАП, может быть:

- самостоятельным модулем;
- частью цифрового прибора;
- частью микроконтроллера или микроконвертера;
- микросхемой, требующей дополнительных элементов для правильного функционирования.

ПРИНЦИПЫ ДЕЙСТВИЯ АЦП

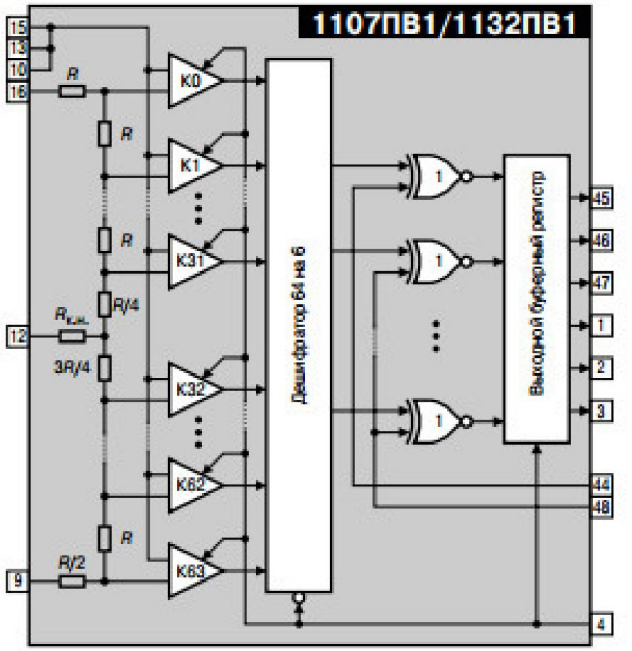
- Предварительное преобразование напряжения
  - в перемещение
    - твёрдого тела
    - электронного луча
    - луча света?
  - в длительность интервала времени
  - в частоту гармонического или импульсного сигнала
- Сравнение напряжений
  - с помощью делителя на одинаковых резисторах
  - с помощью ЦАП
  - цепями, развёрнутыми в пространстве
- Сравнение интегралов (charge balance)
  - двухтактное или многотактное интегрирование
  - сигма-дельта модуляция

АЦП С ПРЕДВАРИТЕЛЬНЫМ ПРЕОБРАЗОВАНИЕМ

- АЦП с преобразованием в перемещение твёрдого тела строились на основе самопишущих приборов и приборов со световым отсчётом («digizet»). Сейчас вышли из употребления..
- АЦП с преобразованием в перемещение электронного луча использовались в ранних системах цифровой связи, обеспечивая высокое быстродействие. Сейчас вышли из употребления.
- АЦП с преобразованием в параметры светового луча (например, поворот плоскости поляризации), возможно, получат распространение в связи с развитием фотоники.
- АЦП с преобразованием в длительность интервала времени преимущественно применялись в ранних электронных цифровых вольтметрах. Возможно, они сохранились в амплитудных анализаторах ядерной физики (см. главу 2).
- АЦП с преобразованием в частоту применялись в некоторых цифровых вольтметрах. Сейчас они (с помощью микросхем, рассмотренных в главе 2) могут использоваться для решения нестандартных измерительных задач.

АЦП СО СРАВНЕНИЕМ НАПРЯЖЕНИЙ С ПОМОЩЬЮ ДЕЛИТЕЛЯ НА ОДИНАКОВЫХ РЕЗИСТОРАХ – FLASH ADC, АЦП СЧИТЫВАНИЯ

СТРУКТУРНАЯ СХЕМА



1107ПВ1 − 6 разрядов, 20 МГц

19-1170; Rev 0; 12/98

EVALUATION KIT AVAILABLE

MAXIM

8-Bit, 750Msps Flash ADC

MAX1151

General Description

The MAX1151 is a parallel flash analog-to-digital converter (ADC) capable of digitizing full-scale (0V to -2V) inputs into 8-bit digital words at an update rate of 750Msps. The ECL-compatible outputs are demuxed into two separate output banks, each with differential data-ready outputs to ease the task of data capture. The MAX1151's wide input bandwidth and low capacitance eliminate the need for external track/hold amplifiers for most applications. A proprietary decoding scheme reduces metastable errors to 1LSB. This device operates from a single -5.2V supply, with a nominal power dissipation of 5.5W.

Features

- 1:2 Demuxed ECL-Compatible Outputs
- Wide Input Bandwidth: 900MHz
- Low Input Capacitance: 15pF
- Metastable Errors Reduced to 1LSB
- Single -5.2V Supply

Applications

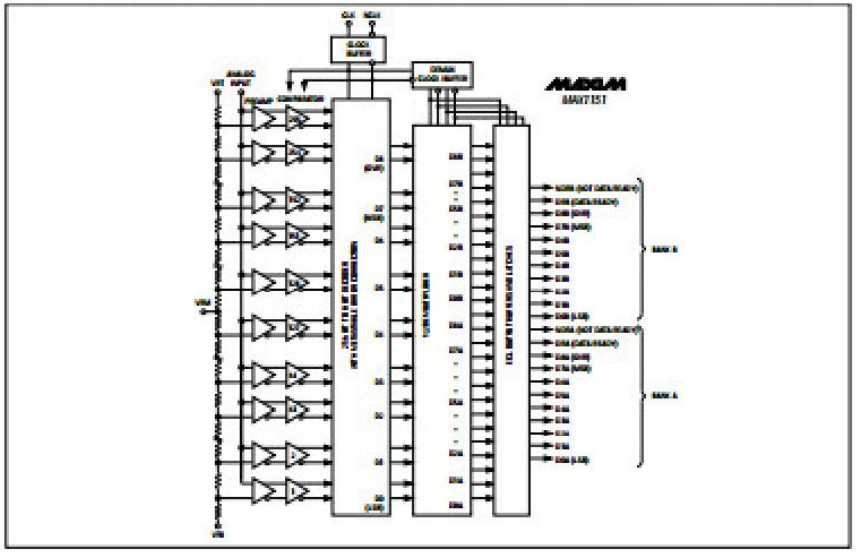
Digital Oscilloscopes
Data Acquisition
Transient-Capture Applications
Radar, EW, ECM
Direct RF/IF Downconversion

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1151AI2S	-20°C to +85°C	80 MQUAD
MAX1151BI2S	-20°C to +85°C	80 MQUAD

Pin Configuration appears on last page.

Functional Diagram



MAXIM — Maxim Integrated Products 1

For the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Современных микросхем при быстром поиске не было найдено

ПАРАЛЛЕЛЬНО-ПОСЛЕДОВАТЕЛЬНЫЕ (PIPELINED – КОНВЕЙЕРНЫЕ) АЦП

Согласно статье

Analog-to-Digital Converter Architectures and Choices for System Design

by **Brian Black**

конвейерные АЦП относятся к одному из трёх основных классов современных системных АЦП. Два других класса – это АЦП последовательных приближений и АЦП с ΣΔ-модуляторами.

ТОЛЬКО ЭТИ ТРИ КЛАССА ВСТРЕЧАЮТСЯ В ТАБЛИЦЕ ВЫБОРА АЦП ФИРМЫ ANALOG DEVICES

Фрагмент таблицы:

A/D Converters

Развернуть фильтры | Сортировать по Новейшим | Выбрать Параметры | Восстановить таблицу | Загрузить в Excel

Наименован...	Eval / Ref Circuit	Bits (bits)	Sample Rate (max) (SPS)	Channels	Device Architecture	INL in LSB (typ) (LSBs)	Vin Range (typ) (V p-p)	ADC SNR in dBFS (typ) (dBFS)	Power (typ) (W)	Temp Range	Output Data Format	Input Type	US Price 1000 to 4999 ($ US)	Vref Source
	0 Вы...	16 В...	16.6 - 3G	13 Выб...	7 Выбран...	0.04 - 35	0.039 - 40	45 - 112	21u - 711	12 В...	14 Вы...	9 Вы...	0.98 - 1326	5 Выб...
AD4006		18	1M	1	SAR	0.8	5	95	7m	-40 to 12...	Serial, SPI	Pseudo ...	$15.95	External
AD4002		18	2M	1	SAR	0.8	5	95	14m	-40 to 12...	Serial, SPI	Pseudo ...	$22.45	External
AD9695-625		14	625M	2	Pipelined	2	1.7	67.2	980m	-40 to 85...	JESD204B	Different...	$406.26	Int/Ext
AD9695-1300		14	1.3G	2	Pipelined	1	1.59	65.6	1.6	-40 to 85...	JESD204B	Different...	$831.30	Int/Ext
AD9689-2600		14	2.6G	2	Pipelined	6	1.7	61.3	3.1	-40 to 85...	JESD204B	Different...	$1,108.34	Int/Ext
AD9689-2000		14	2G	2	Pipelined	2	1.7	62.7	2.5	-40 to 85...	JESD204B	Different...	$934.86	Int/Ext
AD4008		16	500k	1	SAR	0.2	5	93	2m	-40 to 12...	Serial, SPI	Pseudo ...	$6.75	External
AD7771		24	128k	8	Sigma-Delta	1.5	2.5	66	133m	-40 to 12...	SPI	Different...	$8.46	External, ...
AD7617		14	1M	16	SAR	0.3	20	85	230m	-40 to 12...	Parallel, ...	Pseudo ...	$10.76	Int/Ext
AD7616-P		16	1M	16	SAR	1	20	90.5	230m	-40 to 12...	Parallel	Pseudo ...	$11.96	Int/Ext
AD4020		20	1.8M	1	SAR	1	10	100.5	15m	-40 to 12...	Serial, SPI	Different...	$29.50	External
AD4011		18	500k	1	SAR	0.4	10	100.5	4m	-40 to 12...	Serial, SPI	Different...	$11.45	External
AD4007		18	1M	1	SAR	0.4	10	100.5	8m	-40 to 12...	Serial, SPI	Different...	$18.95	External
ADAQ7988		16	500k	1	SAR	0.5	5	91.5	21m	-55 to 12...	QSPI, Se...	Pseudo ...	$9.75	External

КОНВЕЙЕРНЫЕ АЦП – «ГИБРИД» АЦП СЧИТЫВАНИЯ И ПОСЛЕДОВАТЕЛЬНЫХ ПРИБЛИЖЕНИЙ

(По той же статье)

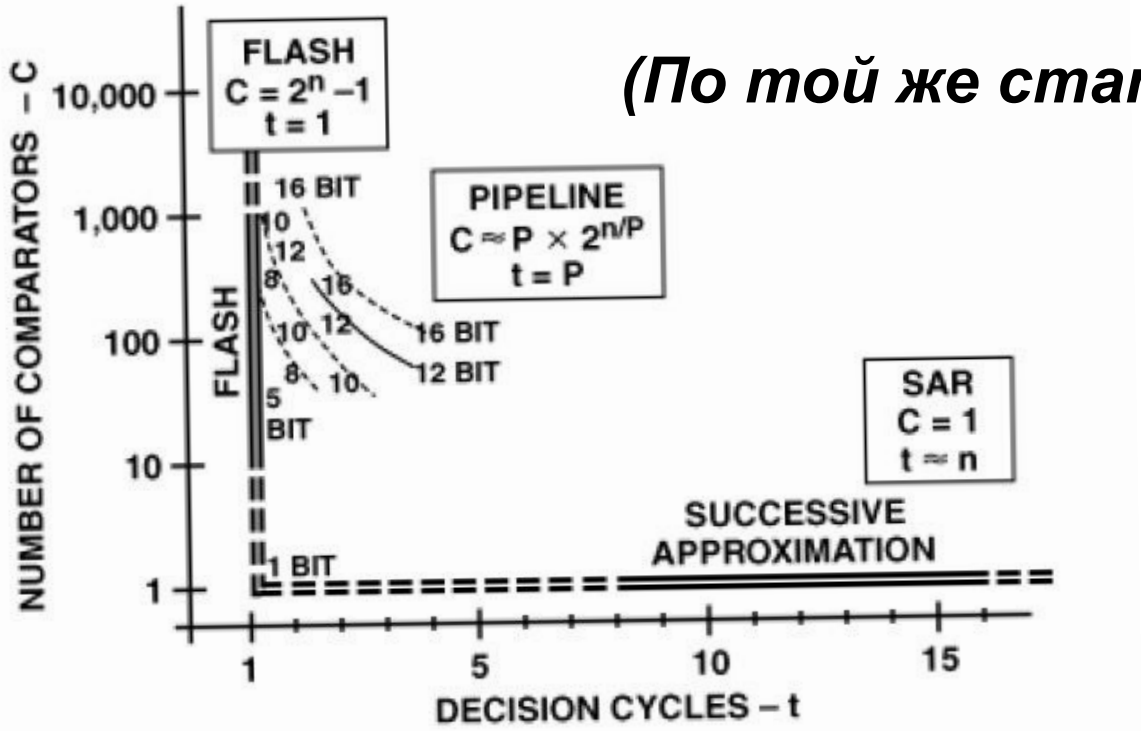


Figure 1. Tradeoff between decision cycles and comparators.

Они заняли нишу средней разрядности и быстродействия от десятков до сотен миллионов преобразований в секунду

СТУПЕНЬ КОНВЕЙЕРНОГО АЦП

(По той же статье)

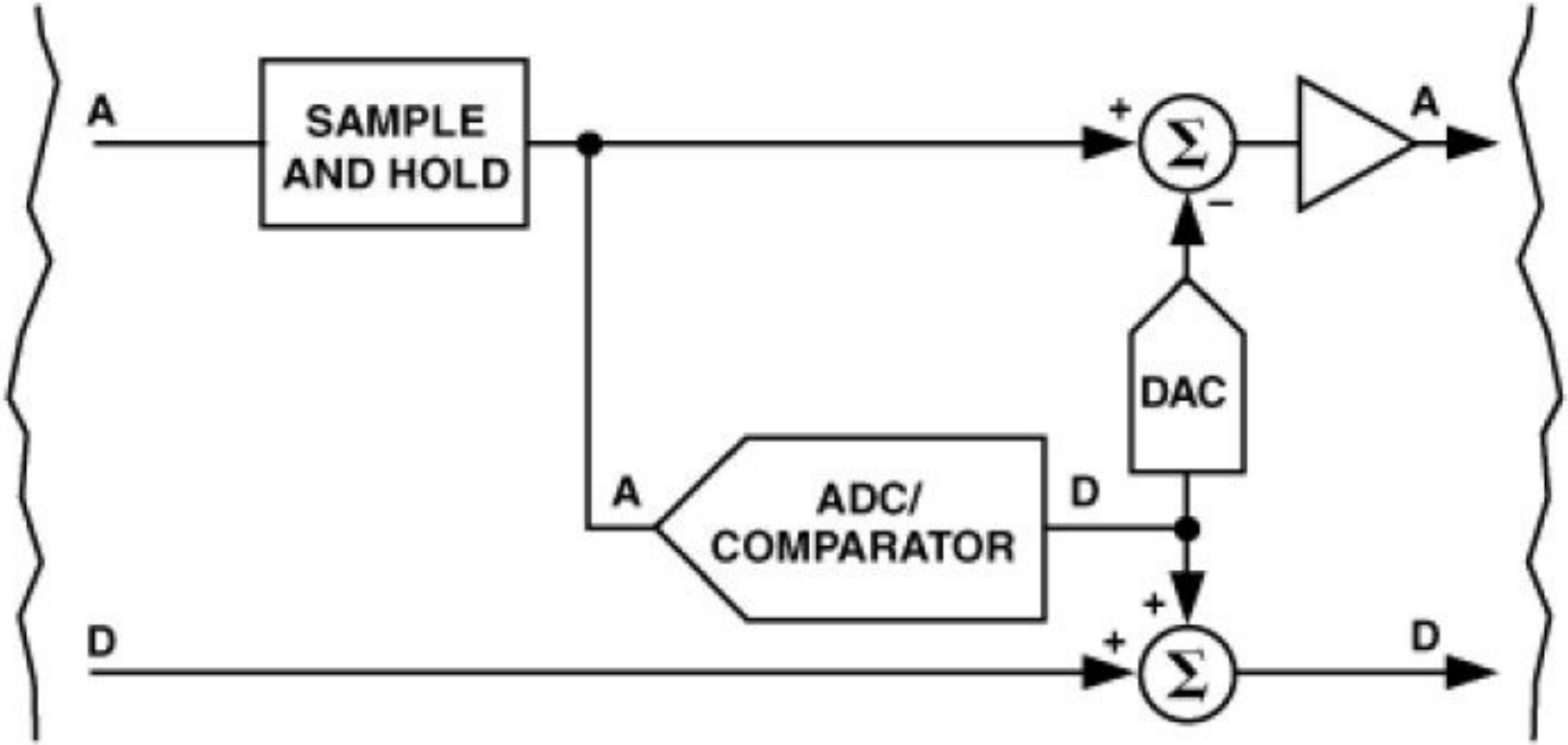
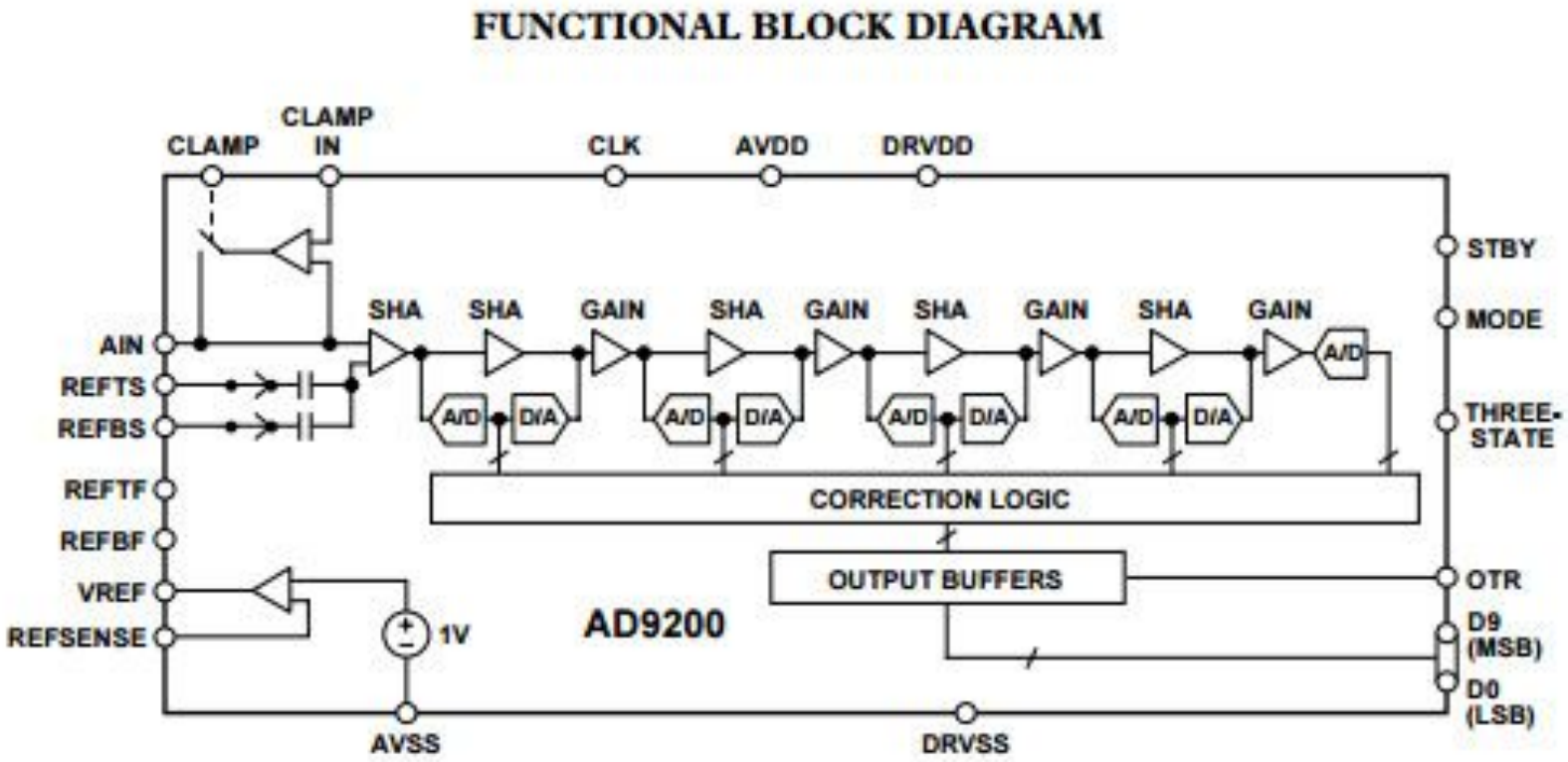


Figure 3. A single pipelined converter stage.

ТИПИЧНАЯ ОБЩАЯ СТРУКТУРА КОНВЕЙЕРНОГО АЦП



Таким образом, принцип действия конвейерных АЦП является частным случаем сравнения напряжений цепями, развёрнутыми в пространстве

ПРИМЕР СОВРЕМЕННОЙ МИКРОСХЕМЫ КОНВЕЙЕРНОГО АЦП

ANALOG DEVICES

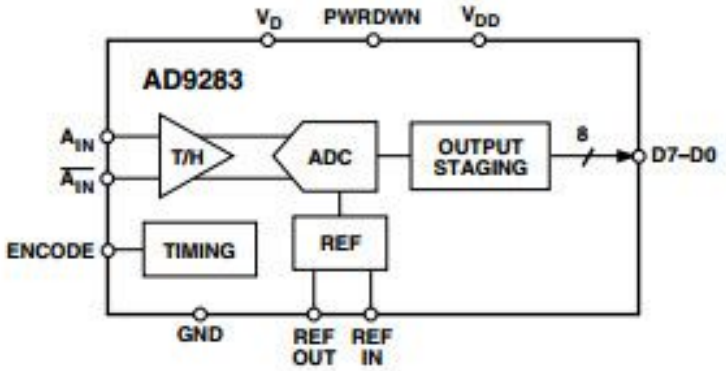
8-Bit, 50 MSPS/80 MSPS/100 MSPS 3 V A/D Converter

AD9283

FEATURES
8-Bit, 50, 80, and 100 MSPS ADC
Low Power: 90 mW at 100 MSPS
On-Chip Reference and Track/Hold
475 MHz Analog Bandwidth
SNR = 46.5 dB @ 41 MHz at 100 MSPS
1 V p-p Analog Input Range
Single 3.0 V Supply Operation (2.7 V–3.6 V)
Power-Down Mode: 4.2 mW

APPLICATIONS
Battery Powered Instruments
Hand-Held Scopemeters
Low Cost Digital Oscilloscopes

FUNCTIONAL BLOCK DIAGRAM



ОПИСАНИЕ МИКРОСХЕМЫ AD9283

Theory of Operation

The analog signal is applied differentially or single-endedly to the inputs of the AD9283. The signal is buffered and fed forward to an on-chip sample-and-hold circuit. The ADC core architecture is a bit-per-stage pipeline type converter utilizing switch capacitor techniques. The bit-per-stage blocks determine the 5 MSBs and drive a FLASH converter to encode the 3 LSBs. Each of the 5 MSB stages provides sufficient overlap and error correction to allow optimization of performance with respect to comparator accuracy. The output staging block aligns the data, carries out the error correction and feeds the data to the eight output buffers. The AD9283 includes an on-chip reference (nominally 1.25 V) and generates all clocking signals from one externally applied encode command. This makes the ADC easy to interface with and requires very few external components for operation.

ВРЕМЕННЫЕ ДИАГРАММЫ МИКРОСХЕМЫ AD9283

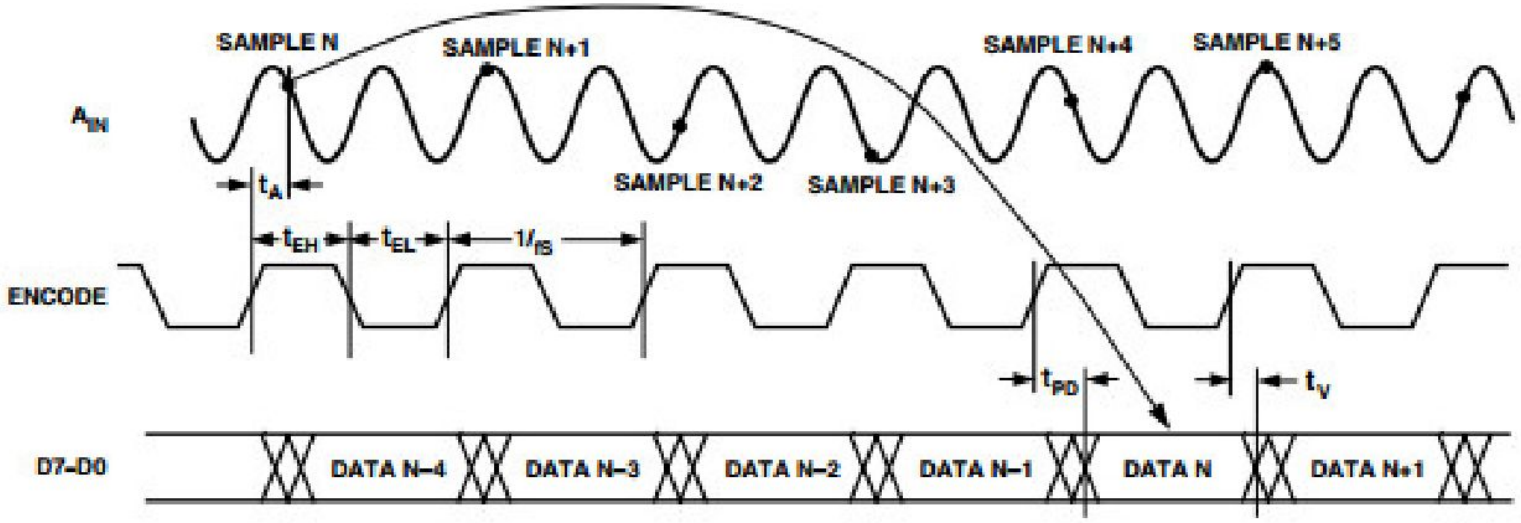


Figure 1. Timing Diagram

АЦП С АНАЛОГОВОЙ СВЁРТКОЙ

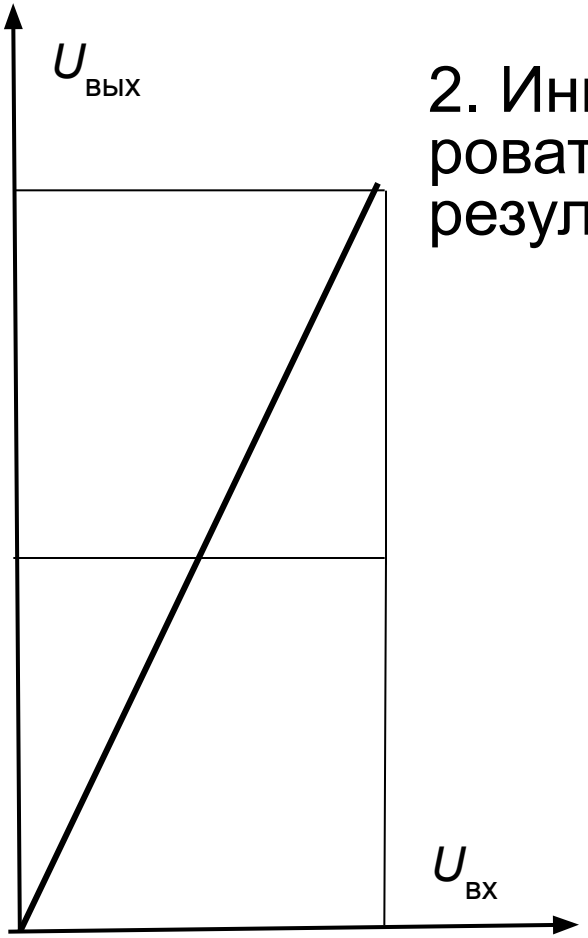
- ***Параллельно-последовательное преобразование***, как и другие принципы развёртывания цепей сравнения в пространстве, обеспечило высокую скорость преобразования при умеренной сложности АЦП.
- Из других испробованных принципов принципиальный интерес представляет ***аналоговая свёртка***. Только в АЦП с аналоговой свёрткой каждый компаратор срабатывает независимо от поведения компараторов предшествовавших ступеней. Хотя интерес разработчиков к аналоговой свёртке, по-видимому, затух, об этом принципе нужно сказать несколько слов.

  Остальные известные структуры с развёртыванием цепей сравнения в пространстве можно не рассматривать.

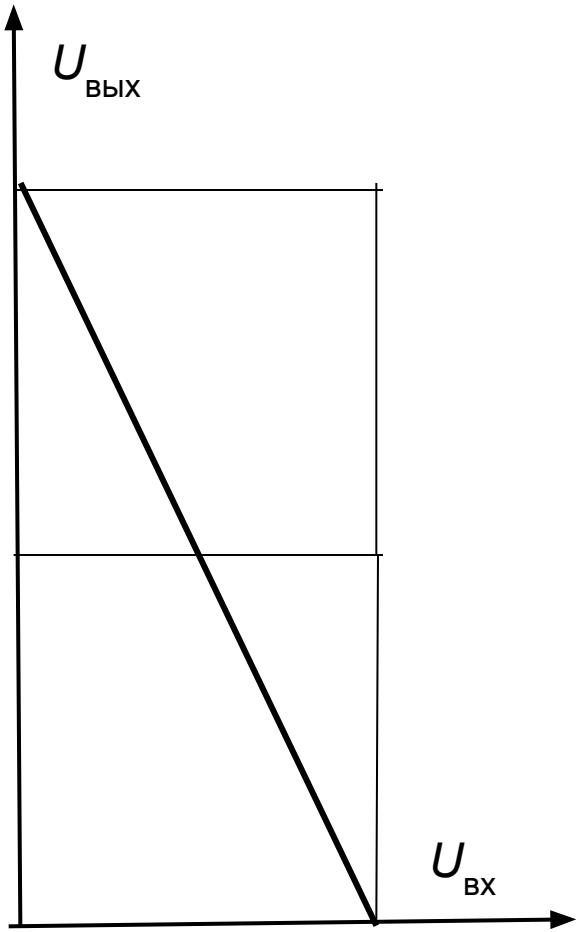
КАСКАД АНАЛОГОВОЙ СВЁРТКИ

Диаграммы работы АЦП с аналоговой свёрткой строятся в функции не времени, а *входного напряжения*

1. Удвоить входное напряжение

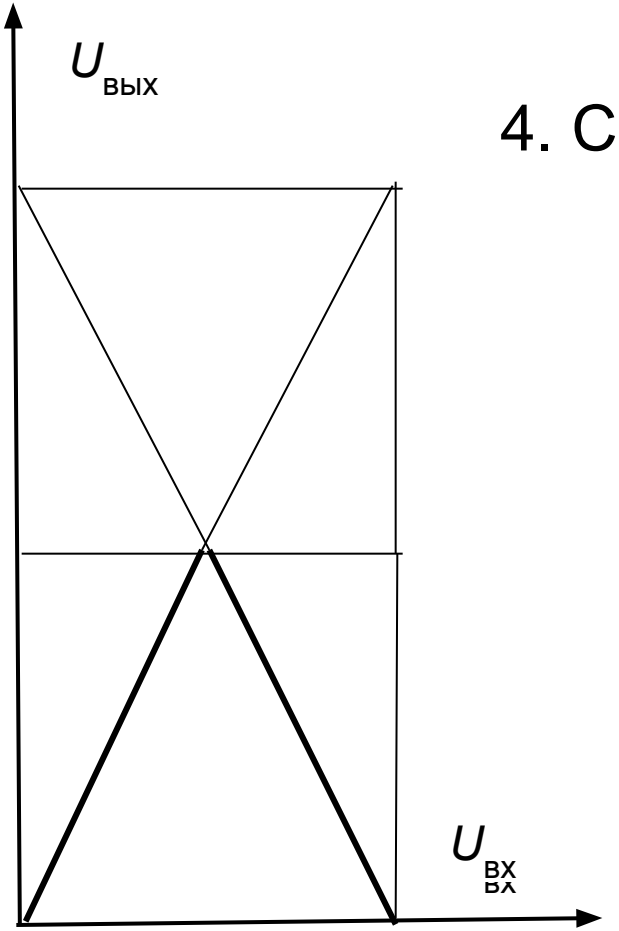


2. Инвертировать результат

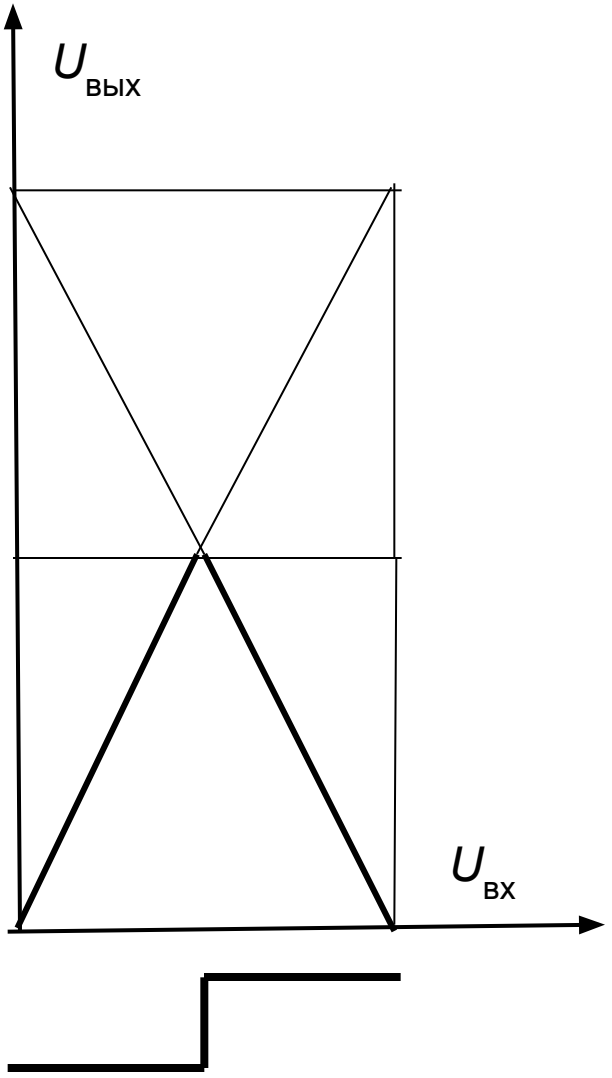


Продолжение операций в каскаде аналоговой свёртки

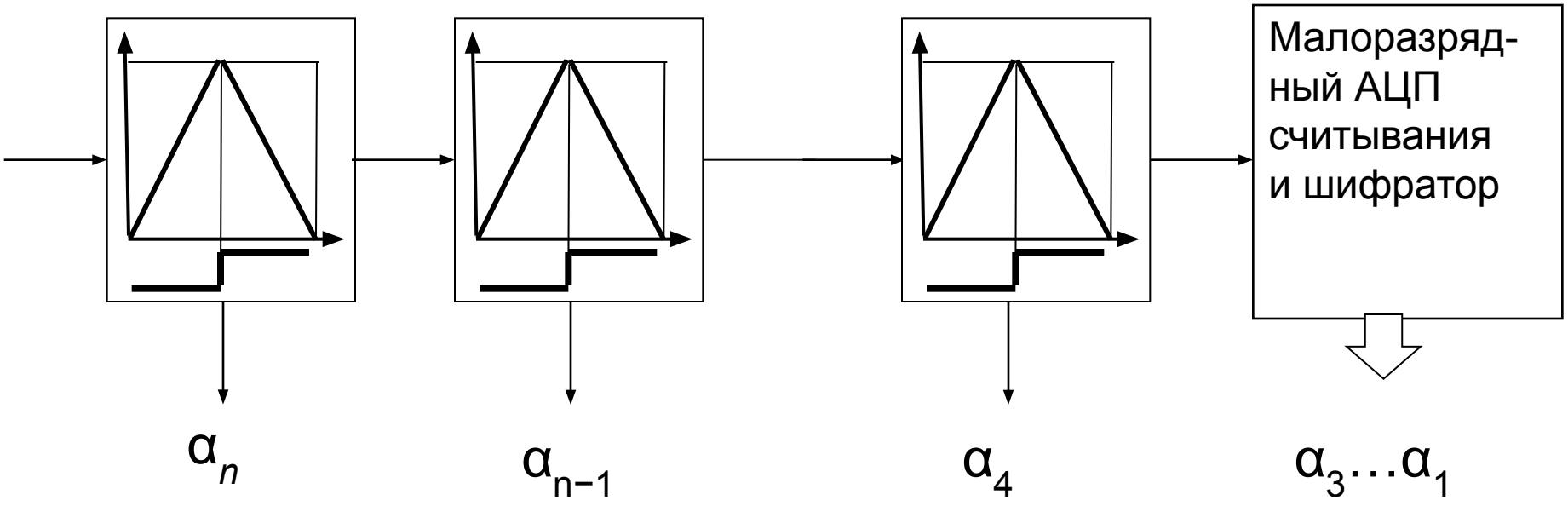
3. Выбрать меньшее



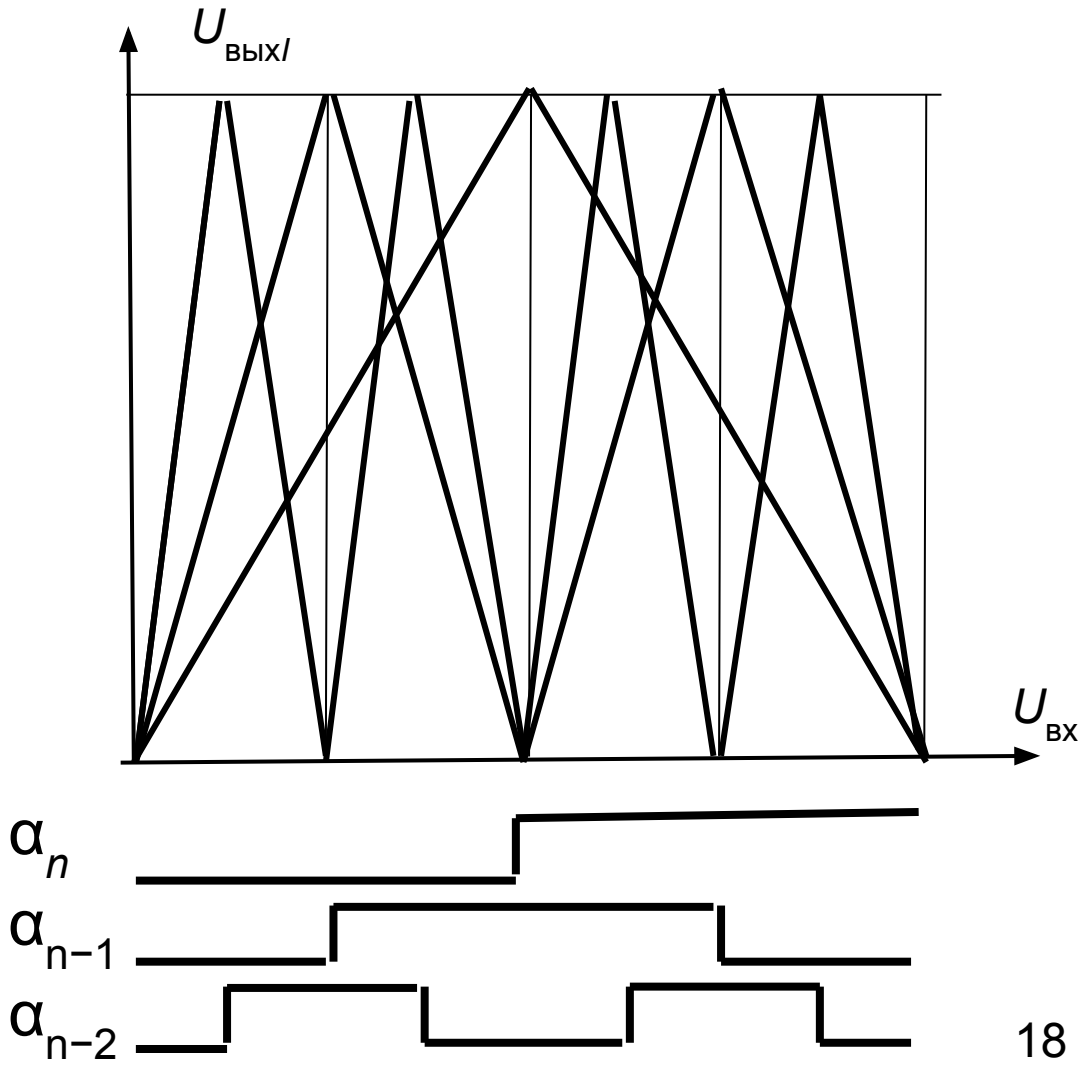
4. Сравнить



СТРУКТУРА СВЁРТОЧНОГО АЦП



ПОСТРОЕНИЕ ОБЩЕЙ ДИАГРАММЫ РАБОТЫ СВЁРТОЧНОГО АЦП

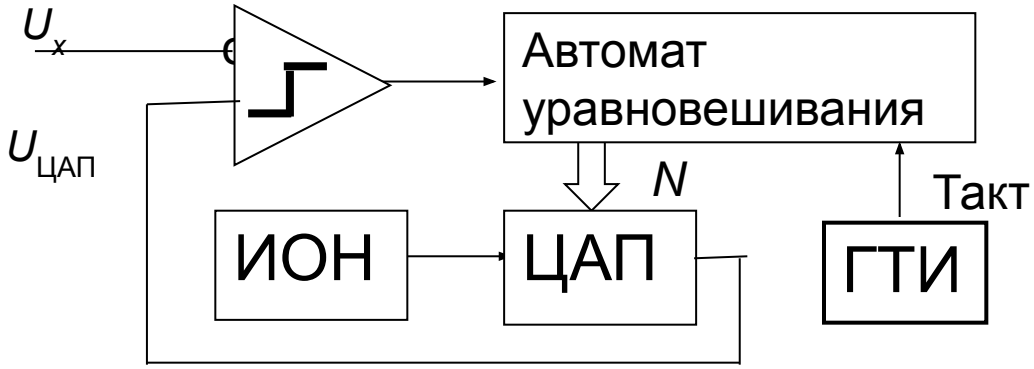


ОСОБЕННОСТЬ СВЁРТОЧНОГО АЦП

Последовательность каскадов аналоговой свёртки формирует цифровой результат в коде Грея. Для обеспечения однородности выходной код оконечного АЦП считывания тоже преобразуют в код Грея.

Это позволяет считывать цифровой результат преобразования *в произвольный момент времени*.

АЦП СО СРАВНЕНИЕМ НАПРЯЖЕНИЙ С ПОМОЩЬЮ ЦАП



В зависимости от устройства автомата уравновешивания возможны разные алгоритмы преобразования.

- При счётчике, прекращающем счёт, если $U_{ЦАП} > U_x$, получается *развёртывающее преобразование*.
- При реверсивном счётчике, меняющем направление счёта в зависимости от знака разности $U_x - U_{ЦАП}$, получается *следящее преобразование*.
- При регистре последовательных приближений (sequential approximation register, SAR) получается *поразрядное уравновешивание* (дихотомия, последовательное приближение). Последний термин неточен, но укоренился именно он.

- ***Развёртывающее преобразование***, по-видимому, сейчас используется только радиолюбителями.
- ***Следящее преобразование*** было довольно популярно в 1960-х годах. Сейчас применяется для решения специальных задач (например, в микросхемах для работы с СКВТ).
- ***Последовательное приближение*** в своё время было основным алгоритмом работы цифровых вольтметров (сейчас вытеснено двухтактным интегрированием). Продолжают выпускаться микросхемы АЦП последовательного приближения, самостоятельные и в составе микроконтроллеров, часто многоканальные..
- Некоторые другие алгоритмы уравновешивания (например, подекадное развёртывание) были предложены для цифровых вольтметров, но перестали применяться.

Принцип последовательного приближения и соответствующие микросхемы АЦП следует рассмотреть подробнее. У микросхем сначала расмотрим аналоговую сторону, затем цифровую сторону − интерфейсы.

ПРИМЕР ПОСЛЕДОВАТЕЛЬНОГО ПРИБЛИЖЕНИЯ

Таблица 5

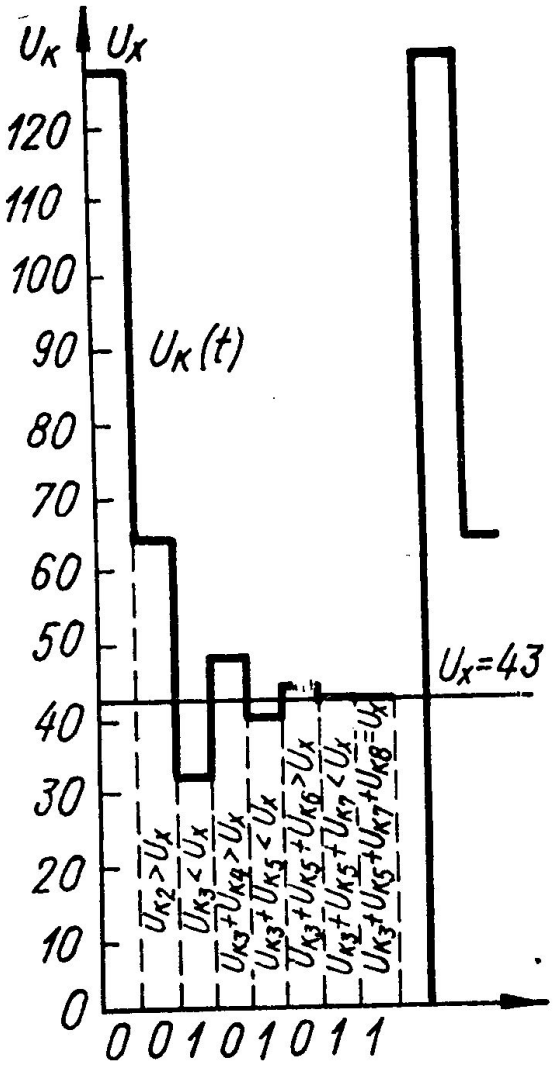
Пример процесса поразрядного уравновешивания

$a_0a_1a_2a_3a_4a_5a_6a_7a_8a_9$	$U_{комп}$	Компа-ратор	Последний включенный разряд
1 0 0 0 0 0 0 0 0 0	512	мало	остается
1 **1** 0 0 0 0 0 0 0 0	512+256=768	много	отбрасывается
1 0 **1** 0 0 0 0 0 0	512+128=640	много	отбрасывается
1 0 0 **1** 0 0 0 0 0	512+64=576	мало	остается
1 0 0 1 **1** 0 0 0 0	576+32=608	много	отбрасывается
1 0 0 1 0 **1** 0 0 0	576+16=592	много	отбрасывается
1 0 0 1 0 0 **1** 0 0	576+8=584	мало	остается
1 0 0 1 0 0 1 **1** 0	584+4=588	много	отбрасывается
1 0 0 1 0 0 1 0 **1**	584+2=586	мало	остается
1 0 0 1 0 0 1 0 1 **1**	586+1=587	много	отбрасывается
1 0 0 1 0 0 1 0 1 0	Окончательный результат, равен десятичному 586		

По книге: Солопченко Г.Н. Измерительные информационные системы. – СПб.: Изд-во Политехн. ун-та, 2010, с. 117. Разряды пронумерованы от старшего к младшему, диапазон преобразования АЦП 0…1023 мВ. U_x = 586,5 мВ.

ПРИМЕР В ВИДЕ ВРЕМЕННÓЙ ДИАГРАММЫ

По книге: Орнатский, с.423. Диапазон преобразования АЦП 0…255 В. U_x = 43 В.



ПОПРАВКА К ПРИМЕРАМ СОЛОПЧЕНКО И ОРНАТСКОГО

The ideal transfer characteristics for the AD4002/AD4006/ AD4010 are shown in Figure 32 and Table 9.

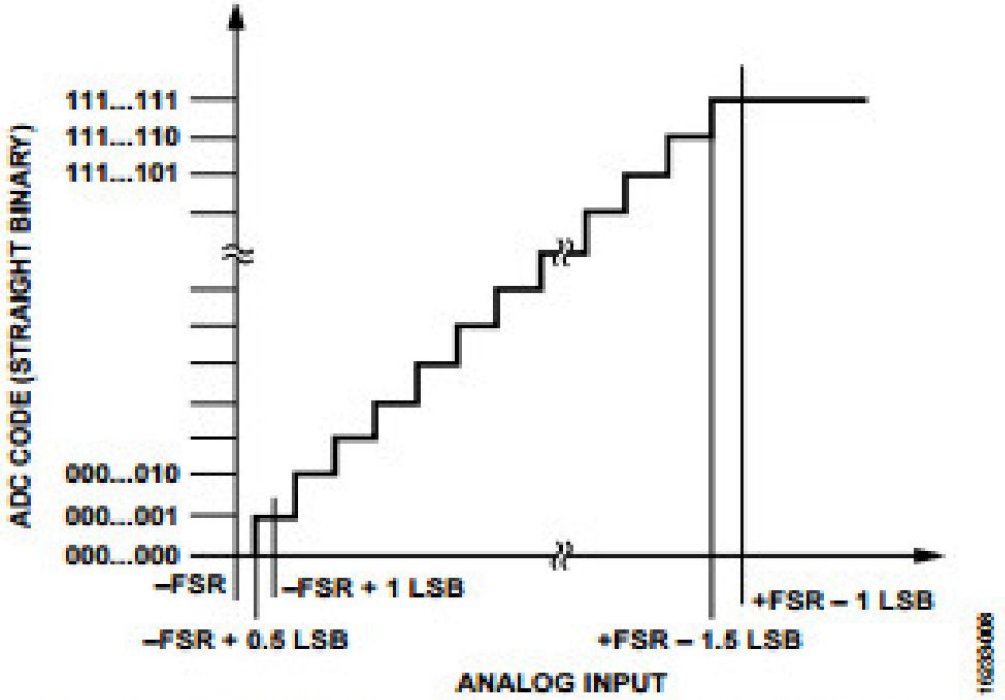
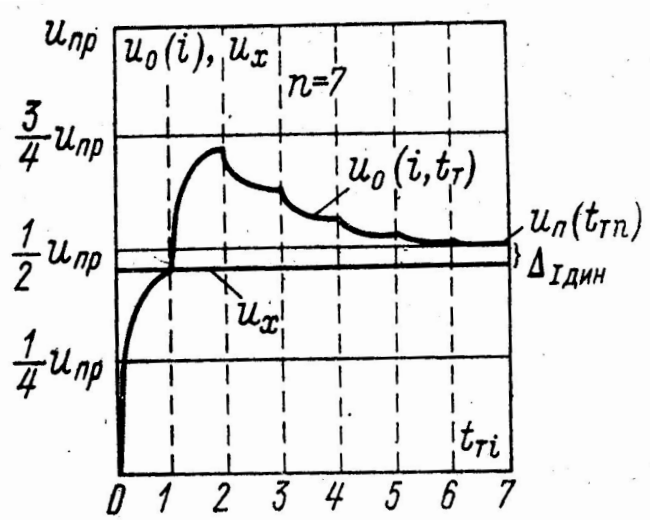


Figure 32. ADC Ideal Transfer Function (FSR Is Full-Scale Range)

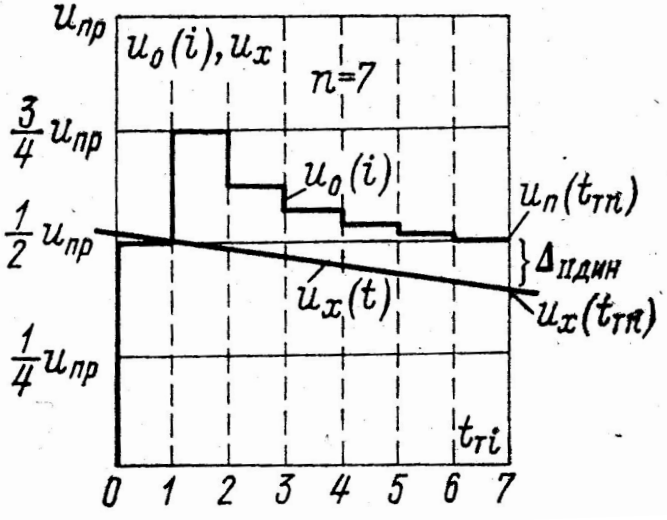
Для получения симметричного распределения погрешности квантования напряжение ЦАП нужно сместить на половину кванта!

НЕКОТОРЫЕ СВОЙСТВА АЦП ПОСЛЕДОВАТЕЛЬНЫХ ПРИБЛИЖЕНИЙ

Инерционность ЦАП ограничивает быстродействие



Изменение преобразуемого напряжения вызывает динамическую погрешность



По книге: Островерхов В.В. Динамические погрешности аналого-цифровых преобразователей. – Л.: Энергия, 1975, с. 18.

ПОСТОЯНСТВО ПРЕОБРАЗУЕМОГО НАПРЯЖЕНИЯ ОБЕСПЕЧИВАЕТСЯ ВСТРОЕННЫМИ *УСТРОЙСТВАМИ ВЫБОРКИ – ХРАНЕНИЯ* УВХ (SAMPLE/HOLD, TRACK/HOLD)

Типичная структура УВХ в фазах выборки и хранения заимствована из фирменного описания микросхем AD7811/AD7812.

В действительности «хранения» не происходит: заряд, полученный конденсатором выборки от входного сигнала, снимается с него в ходе преобразования ёмкостным цифроаналоговым преобразователем.

Правильнее говорить не о фазе хранения, а о фазе преобразования

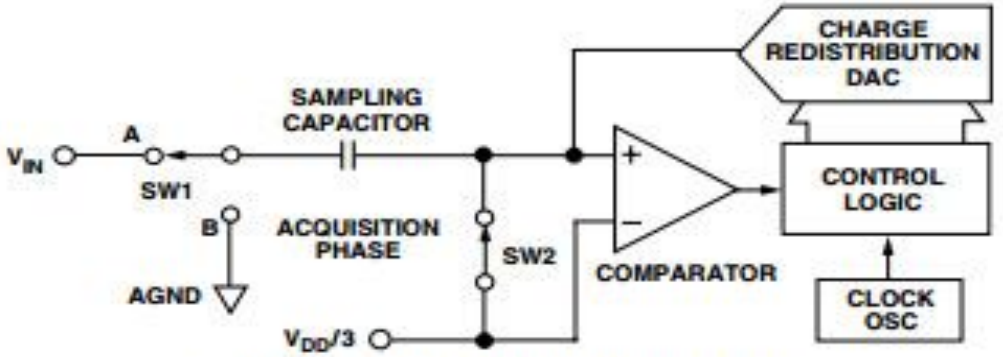


Figure 2. ADC Acquisition Phase

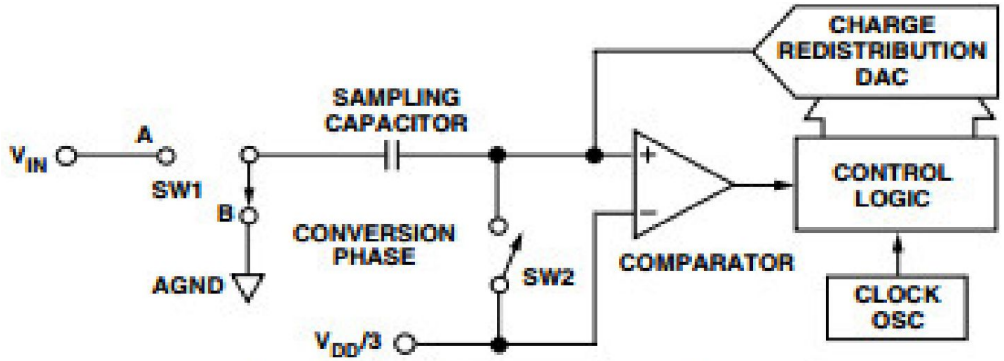
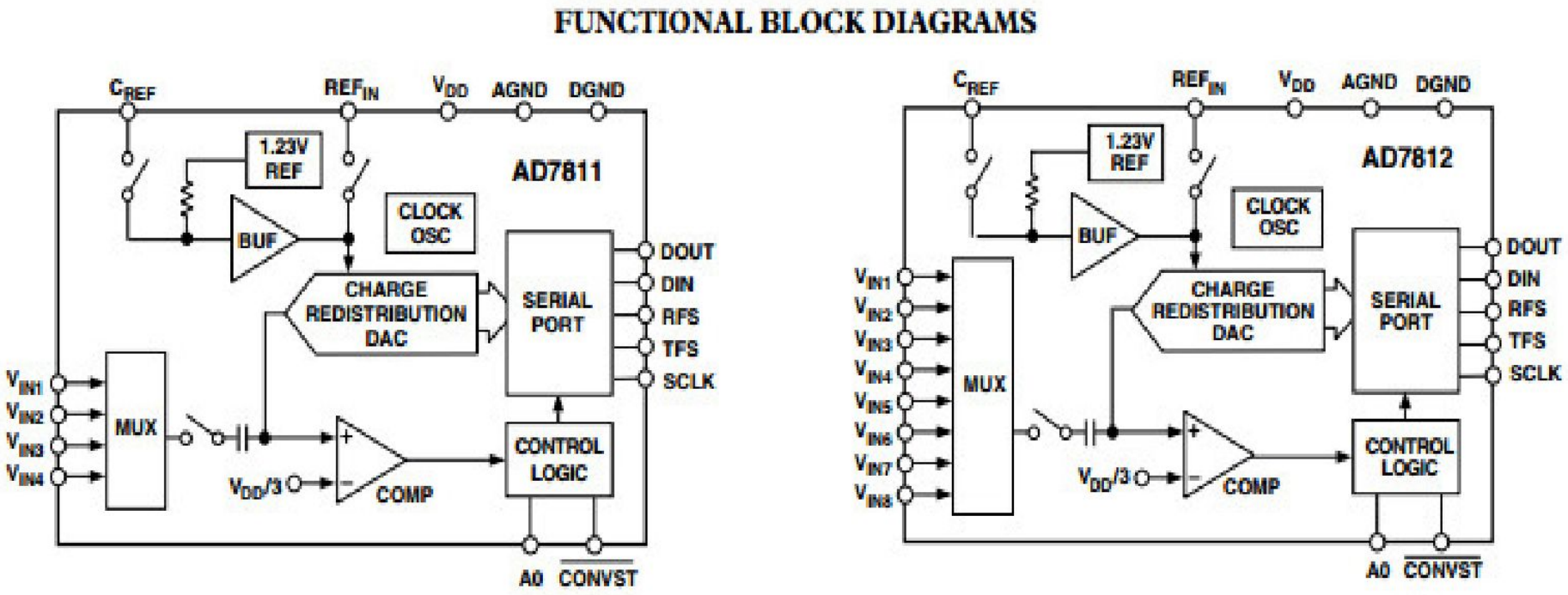


Figure 3. ADC Conversion Phase

СТРУКТУРЫ МИКРОСХЕМ АЦП AD7811/AD7812



Общее описание этих микросхем – на следующем слайде.

ANALOG DEVICES

2.7 V to 5.5 V, 350 kSPS, 10-Bit 4-/8-Channel Sampling ADCs

AD7811/AD7812

FEATURES

10-Bit ADC with 2.3 µs Conversion Time
The AD7811 has Four Single-Ended Inputs that Can Be Configured as Three Pseudo Differential Inputs with Respect to a Common, or as Two Independent Pseudo Differential Channels
The AD7812 has Eight Single-Ended Inputs that Can Be Configured as Seven Pseudo Differential Inputs with Respect to a Common, or as Four Independent Pseudo Differential Channels
Onboard Track and Hold
Onboard Reference 2.5 V ± 2.5%
Operating Supply Range: 2.7 V to 5.5 V
Specifications at 2.7 V–3.6 V and 5 V ± 10%
DSP-/Microcontroller-Compatible Serial Interface
High Speed Sampling and Automatic Power-Down Modes
Package Address Pin on the AD7811 and AD7812 Allows Sharing of the Serial Bus in Multipackage Applications
Input Signal Range: 0 V to V_{REF}
Reference Input Range: 1.2 V to V_{DD}
Qualified for Automotive Applications

GENERAL DESCRIPTION

The AD7811 and AD7812 are high speed, low power, 10-bit A/D converters that operate from a single 2.7 V to 5.5 V supply. The devices contain a 2.3 µs successive approximation A/D converter, an on-chip track/hold amplifier, a 2.5 V on-chip reference and a high speed serial interface that is compatible with the serial interfaces of most DSPs (Digital Signal Processors) and microcontrollers. The user also has the option of using an external reference by connecting it to the V_{REF} pin and setting the EXTREF bit in the control register. The V_{REF} pin may be tied to V_{DD}. At slower throughput rates the power-down mode may be used to automatically power down between conversions.

The control registers of the AD7811 and AD7812 allow the input channels to be configured as single-ended or pseudo differential. The control register also features a software convert start and a software power-down. Two of these devices can share the same serial bus and may be individually addressed in a multipackage application by hardwiring the device address pin. The AD7811 is available in a small, 16-lead 0.3" wide, plastic dual-in-line package (mini-DIP), in a 16-lead 0.15" wide, Small Outline IC (SOIC) and in a 16-lead, Thin Shrink Small Outline Package (TSSOP). The AD7812 is available in a small, 20-lead 0.3" wide, plastic dual-in-line package (mini-DIP), in a 20-lead, Small Outline IC (SOIC) and in a 20-lead, Thin Shrink Small Outline Package (TSSOP).

PRODUCT HIGHLIGHTS

1. Low Power, Single Supply Operation
   Both the AD7811 and AD7812 operate from a single 2.7 V to 5.5 V supply and typically consume only 10 mW of power. The power dissipation can be significantly reduced at lower throughput rates by using the automatic power-down mode e.g., 315 µW @ 10 kSPS, V_{DD} = 3 V—see Power vs. Throughput.
2. 4-/8-Channel, 10-Bit ADC
   The AD7811 and AD7812 have four and eight single-ended input channels respectively. These inputs can be configured as pseudo differential inputs by using the Control Register.
3. On-chip 2.5 V (±2.5%) reference circuit that is powered down when using an external reference.
4. Hardware and Software Control
   The AD7811 and AD7812 provide for both hardware and software control of Convert Start and Power-Down.

СТРУКТУРА ПСЕВДО–ДИФФЕРЕНЦИАЛЬНОГО ВХОДА АЦП

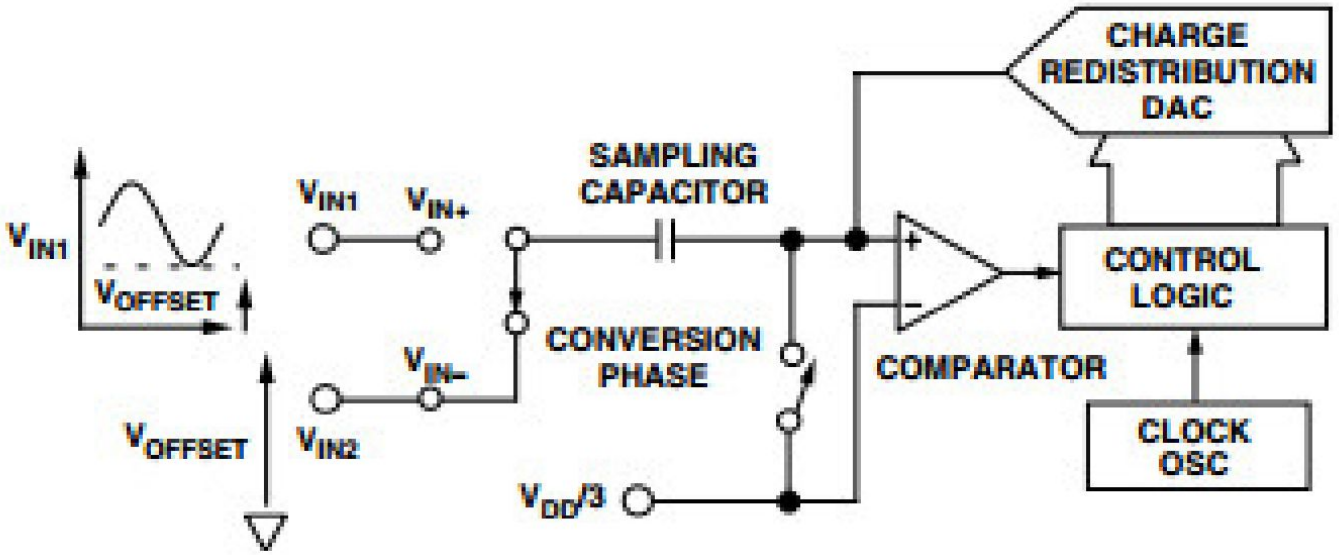


Figure 6. Pseudo Differential Input Scheme

ПРОГРАММНЫЙ ВЫБОР СТРУКТУРЫ ВХОДНОЙ ЦЕПИ ЧЕТЫРЁХКАНАЛЬНОГО АЦП AD7811

(ДЛЯ ВОСЬМИКАНАЛЬНОГО АЦП AD7812 ИМЕЕТСЯ АНАЛОГИЧНАЯ, БОЛЕЕ СЛОЖНАЯ ТАБЛИЦА)

Table I. AD7811 Channel Configurations

$V_{IN4}/\overline{AGND}$	DIF/$\overline{SGL}$	CH1	CH0	Description
0	0	0	0	V_{IN1} Single-Ended with Respect to AGND
0	0	0	1	V_{IN2} Single-Ended with Respect to AGND
0	0	1	0	V_{IN3} Single-Ended with Respect to AGND
0	0	1	1	V_{IN4} Single-Ended with Respect to AGND
1	0	0	0	V_{IN1} Pseudo Differential with Respect to V_{IN4}
1	0	0	1	V_{IN2} Pseudo Differential with Respect to V_{IN4}
1	0	1	0	V_{IN3} Pseudo Differential with Respect to V_{IN4}
X	1	0	0	$V_{IN1}(+)$ Pseudo Differential with Respect to $V_{IN2}(-)$
X	1	0	1	$V_{IN3}(+)$ Pseudo Differential with Respect to $V_{IN4}(-)$
X	1	1	0	Internal Test. SAR Input Equal to $V_{REF}/2$
X	1	1	1	Internal Test. SAR Input Equal to V_{REF}

НАЛИЧИЕ В СТРУКТУРЕ АЦП БЛОКА SIGNAL SCALING МОЖЕТ ОЗНАЧАТЬ ВХОД ЧЕРЕЗ РЕЗИСТИВНЫЙ ДЕЛИТЕЛЬ НАПРЯЖЕНИЯ

ANALOG DEVICES

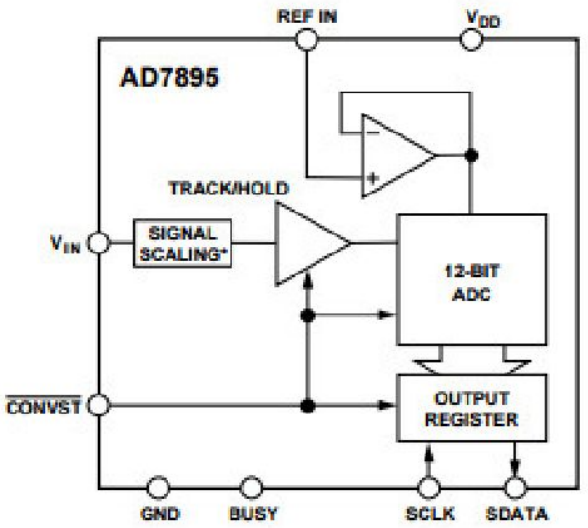
5 V, 12-Bit, Serial 3.8 µs ADC in 8-Pin Package

AD7895

FEATURES

- Fast 12-Bit ADC with 3.8 µs Conversion Time
- 8-Pin Mini-DIP and SOIC
- Single 5 V Supply Operation
- High Speed, Easy-to-Use, Serial Interface
- On-Chip Track/Hold Amplifier
- Selection of Input Ranges
  - ±10 V for AD7895-10
  - ±2.5 V for AD7895-3
  - 0 V to +2.5 V for AD7895-2
- High Input Impedance
- Low Power: 20 mW max
- 14-Bit Pin Compatible Upgrade (AD7894)

FUNCTIONAL BLOCK DIAGRAM



РЕЗИСТИВНЫЙ ДЕЛИТЕЛЬ НА ВХОДЕ МИКРОСХЕМ АЦП AD7895-10 И AD7895-3

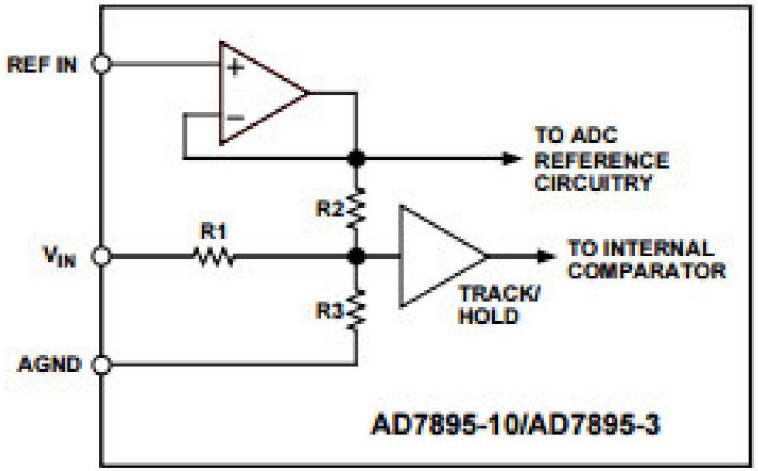


Figure 2. AD7895-10/AD7895-3 Analog Input Structure

ANALOG INPUT			
AD7895-10			
Input Voltage Range	±10	±10	Volts
Input Resistance	24	24	kΩ min
AD7895-3			
Input Voltage Range	±2.5	±2.5	Volts
Input Resistance	9	9	kΩ min
AD7895-2			
Input Voltage Range	0 to +2.5	0 to +2.5	Volts
Input Current	500	500	nA max

РЕЗИСТИВНЫЕ ДЕЛИТЕЛИ НА ВХОДЕ МИКРОСХЕМ АЦП AD7899

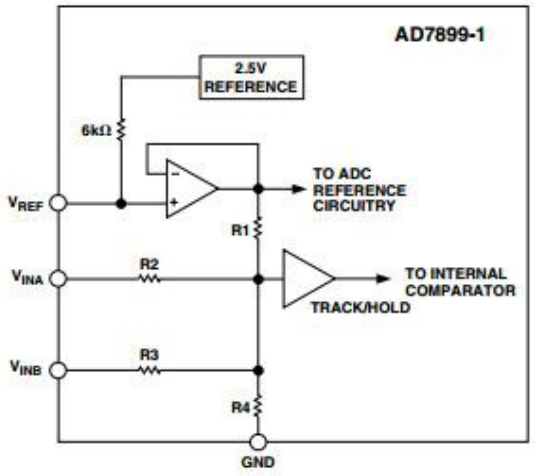


Figure 2. AD7899-1 Analog Input Structure

For the AD7899-1, R1 = 4 kΩ, R2 = 16 kΩ, R3 = 16 kΩ and R4 = 8 kΩ. The resistor input stage is followed by the high input impedance stage of the track/hold amplifier.

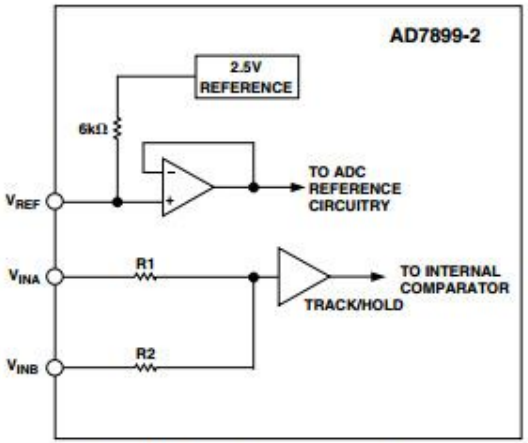


Figure 3. AD7899-2 Analog Input Structure

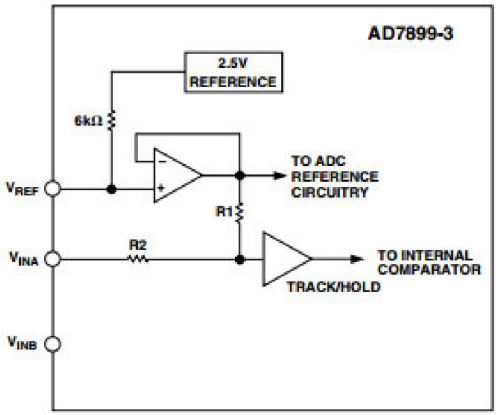


Figure 4. AD7899-3 Analog Input Structure

ИСТОЧНИКИ ОПОРНОГО НАПРЯЖЕНИЯ ДЛЯ МИКРОСХЕМ АЦП

Источник опорного напряжения U_{REF} может быть:

- внешним для микросхемы (external);
- внутренним, встроенным в микросхему (internal);
- внутренним с возможностью подачи внешнего опорного напряжения (при отключении внутреннего источника, как у AD7811/AD7812, или без его отключения).

Иногда под внутренним опорным напряжением АЦП имеется в виду напряжение питания. Тогда обычно указывается диапазон преобразования от нуля до V_{DD} и рекомендуется питание АЦП от микросхемы ИОН.

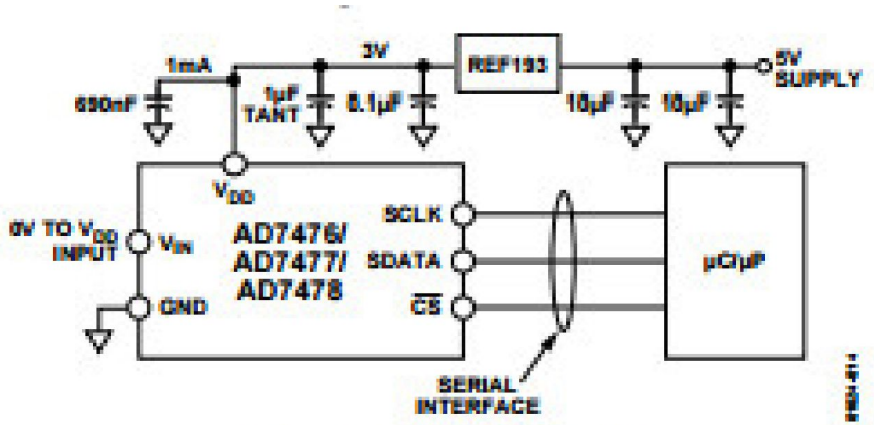


Figure 14. REF193 as Power Supply

ПОДАЧА ВНЕШНЕГО ОПОРНОГО НАПРЯЖЕНИЯ БЕЗ ОТКЛЮЧЕНИЯ ВНУТРЕННЕГО ИСТОЧНИКА В МИКРОСХЕМЕ АЦП AD7899

ANALOG DEVICES

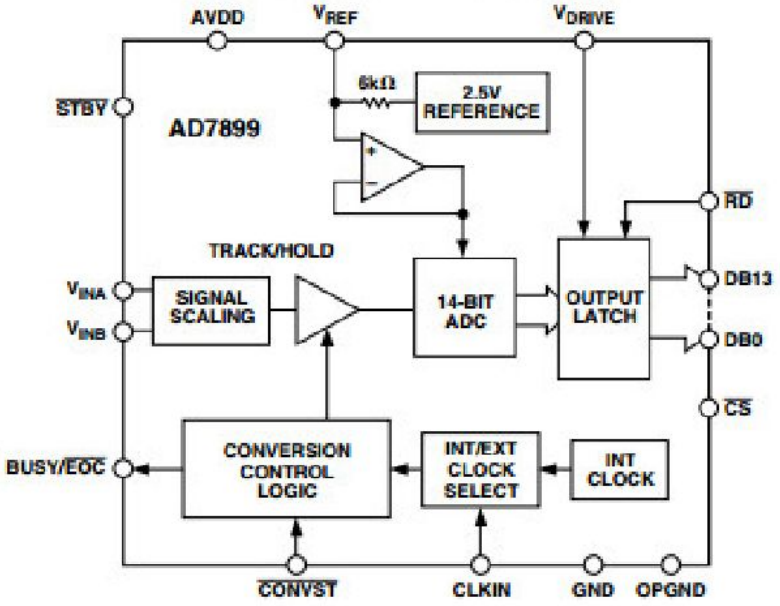
5 V Single Supply 14-Bit 400 kSPS ADC

AD7899

FEATURES

- Fast (2.2 μs) 14-Bit ADC
- 400 kSPS Throughput Rate
- 0.3 μs Track/Hold Acquisition Time
- Single Supply Operation
- Selection of Input Ranges: ±10 V, ±5 V and ±2.5 V
  0 V to 2.5 V and 0 V to 5 V
- High-Speed Parallel Interface which Also Allows
  Interfacing to 3 V Processors
- Low Power, 80 mW Typ
- Power-Saving Mode, 20 μW Typ
- Overvoltage Protection on Analog Inputs
- Power-Down Mode via STBY Pin

FUNCTIONAL BLOCK DIAGRAM



Пояснения к источнику опорного напряжения в структуре микросхемы AD7899

Reference Section

The AD7899 contains a single reference pin, labelled V_{REF}, which either provides access to the part's own 2.5 V reference or allows an external 2.5 V reference to be connected to provide the reference source for the part. The part is specified with a 2.5 V reference voltage.

To use the internal reference as the reference source for the AD7899, simply connect a 0.1 μF capacitor from the V_{REF} pin to AGND. The voltage that appears at this pin is internally buffered before being applied to the ADC. If this reference is required for use external to the AD7899, it should be buffered, as the part has a FET switch in series with the reference output resulting in a source impedance for this output of 6 kΩ nominal. The tolerance on the internal reference is ±10 mV at 25°C with a typical temperature coefficient of 25 ppm/°C and a maximum error over temperature of ±20 mV.

If the application requires a reference with a tighter tolerance or the AD7899 needs to be used with a system reference, the user has the option of connecting an external reference to this V_{REF} pin. The external reference will effectively overdrive the internal reference and thus provide the reference source for the ADC. The reference input is buffered before being applied to the ADC with the maximum input current of ±100 μA. Suitable reference sources for the AD7899 include the AD680, AD780, REF192, and REF43 precision 2.5 V references.

AD7899 – ПРИМЕР МИКРОСХЕМЫ АЦП С ПАРАЛЛЕЛЬНЫМ ИНТЕРФЕЙСОМ

Преобразование запускается сигналом CONVST.
Об окончании преобразования микроконтроллер узнаёт по снятию микросхемой АЦП сигнала BUSY или по появлению сигнала EOC (End Of Conversion). Используется также мнемоника DR − Data Ready. У некоторых микросхем АЦП сигнал об окончании преобразования отстствует.

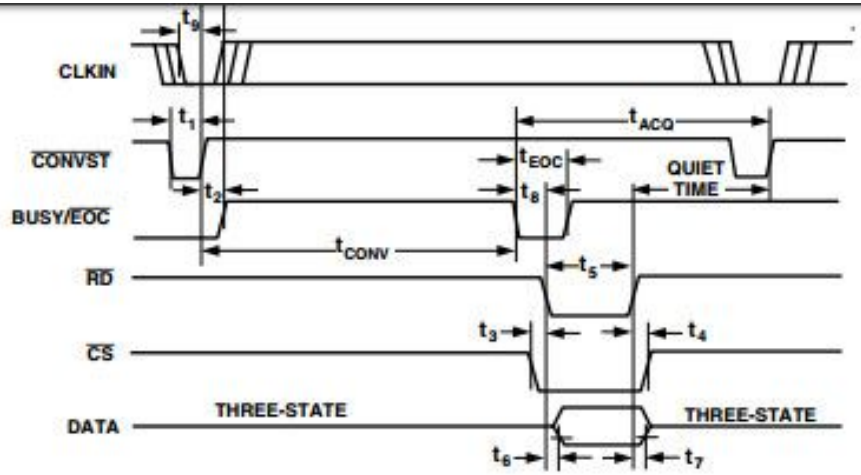


Figure 6. Conversion Sequence Timing Diagram (EOC Mode)

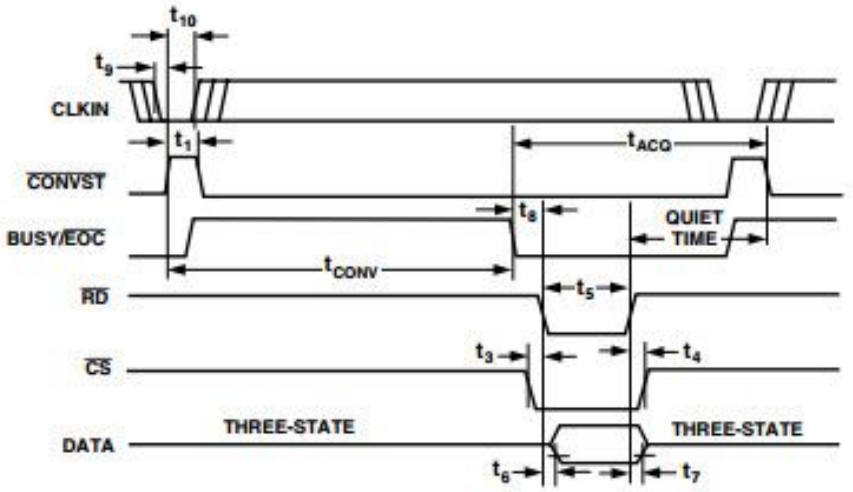


Figure 7. Conversion Sequence Timing Diagram (BUSY Mode)

Вывод V_{DRIVE} позволяет сопрягать микросхему АЦП с микроконтроллером, напряжение питания которого отличается от напряжения питания АЦП.

ВЫБОР ИСТОЧНИКА ТАКТОВЫХ ИМПУЛЬСОВ В АЦП AD7899

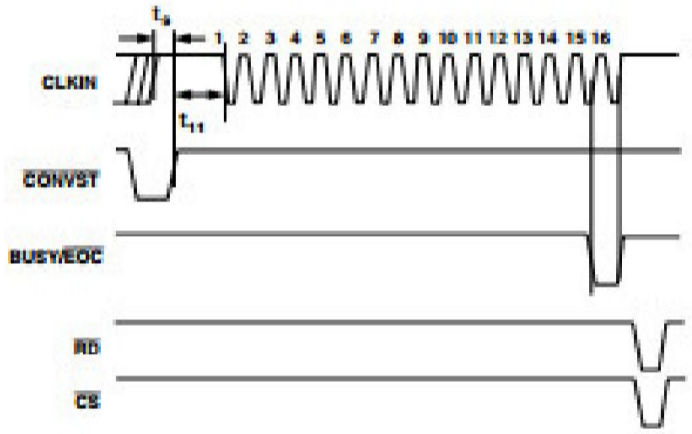


Figure 5. Using an External Clock

Selecting a Conversion Clock

The AD7899 has an internal laser trimmed oscillator which can be used to control the conversion process. Alternatively an external clock source can be used to control the conversion process. The highest external clock frequency allowed is 6.5 MHz. This means a conversion time of 2.46 µs compared to 2.2 µs using the internal clock. However in some instances it may be useful to use an external clock when high throughput rates are not required. For example two or more AD7899s may be synchronized by using the same external clock for all devices. In this way there is no latency between output logic signals due to differences in the frequency of the internal clock oscillators.

On the rising edge of $\overline{\text{CONVST}}$ the AD7899 will examine the status of the CLKIN pin. If this pin is low it will use the internal laser trimmed oscillator as the conversion clock. If the CLKIN pin is high the AD7899 will wait for an external clock to be supplied to this pin which will then be used as the conversion clock. The first falling edge of the external clock should not happen for at least 100 ns after the rising edge of $\overline{\text{CONVST}}$ to ensure correct operation. Figure 5 shows how the BUSY/$\overline{\text{EOC}}$ output is synchronized to the CLKIN signal. Each conversion requires 16 clocks. The result of the conversion is transferred to the output data register on the falling edge of the 15th clock cycle. When the internal clock is selected the status of the CLKIN pin is free to change during conversion but the CLKIN setup and hold times must be observed in order to ensure that the correct conversion clock is used. The CLKIN pin can also be tied low permanently if the internal conversion clock is to be used.

AD7862 – ПРИМЕР *МНОГОКАНАЛЬНОЙ* МИКРОСХЕМЫ АЦП С ПАРАЛЛЕЛЬНЫМ ИНТЕРФЕЙСОМ

ANALOG DEVICES

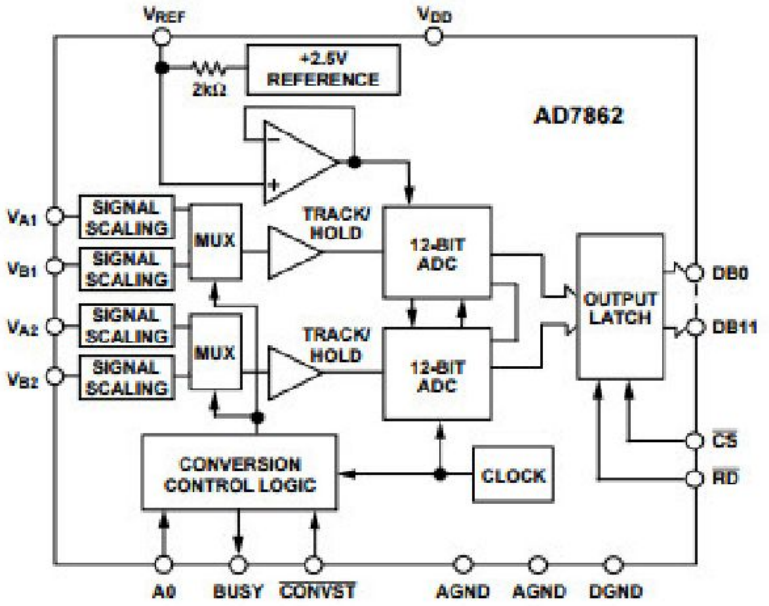
Simultaneous Sampling Dual 250 kSPS 12-Bit ADC

AD7862

FEATURES
Two Fast 12-Bit ADCs
Four Input Channels
Simultaneous Sampling & Conversion
4 μs Throughput Time
Single Supply Operation
Selection of Input Ranges:
  ±10 V for AD7862-10
  ±2.5 V for AD7862-3
  0 V to 2.5 V for AD7862-2
High Speed Parallel Interface
Low Power, 60 mW typ
Power Saving Mode, 50 μW typ
Overvoltage Protection on Analog Inputs
14-Bit Pin Compatible Upgrade (AD7863)

APPLICATIONS
AC Motor Control
Uninterrupted Power Supplies
Data Acquisition Systems
Communications

FUNCTIONAL BLOCK DIAGRAM



ВРЕМЕННЫЕ ДИАГРАММЫ АЦП AD7862 БЕЗ ПЕРЕХОДА В РЕЖИМ ПОНИЖЕННОГО ПОТРЕБЛЕНИЯ

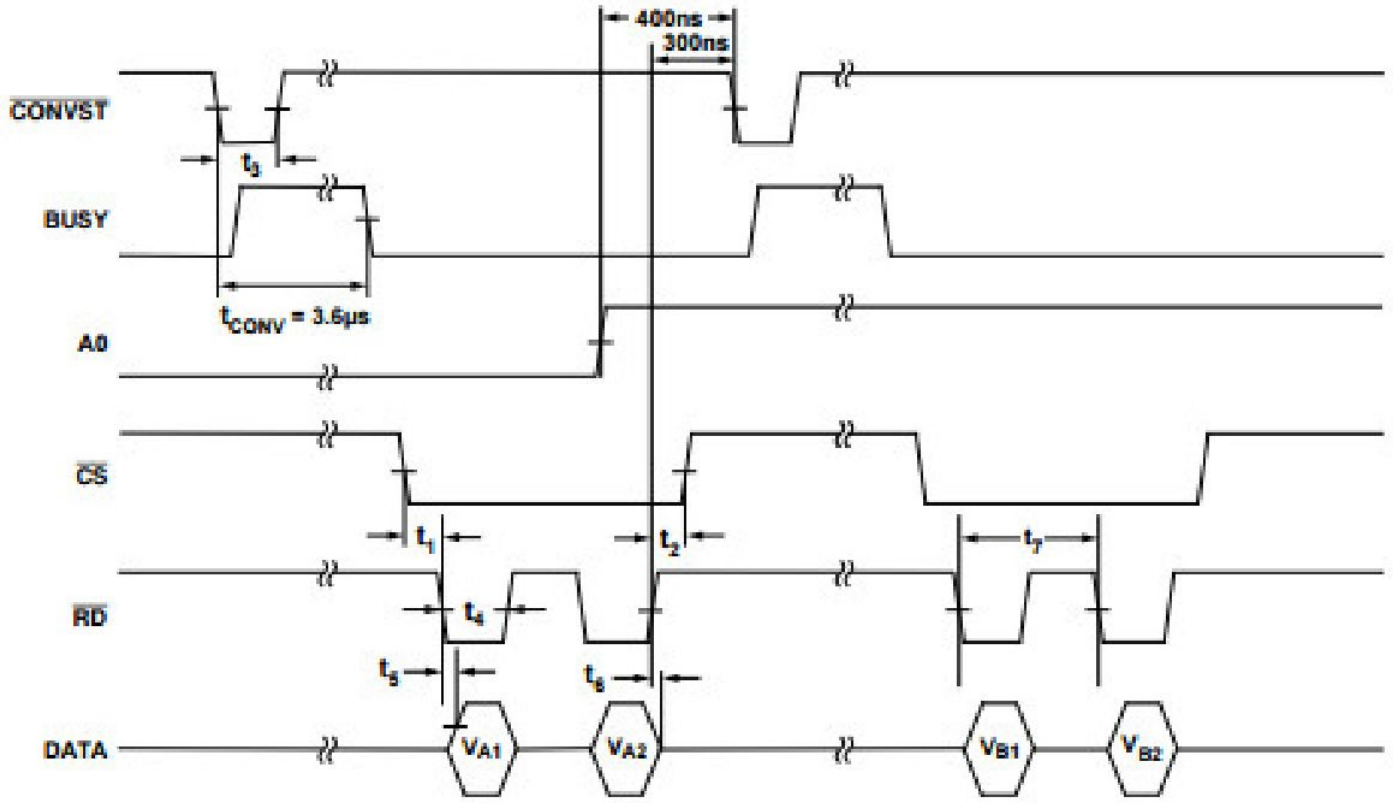


Figure 5a. Mode 1 Timing Operation Diagram for High Sampling Performance

ВРЕМЕННЫЕ ДИАГРАММЫ АЦП AD7862 С ПЕРЕХОДОМ В РЕЖИМ ПОНИЖЕННОГО ПОТРЕБЛЕНИЯ

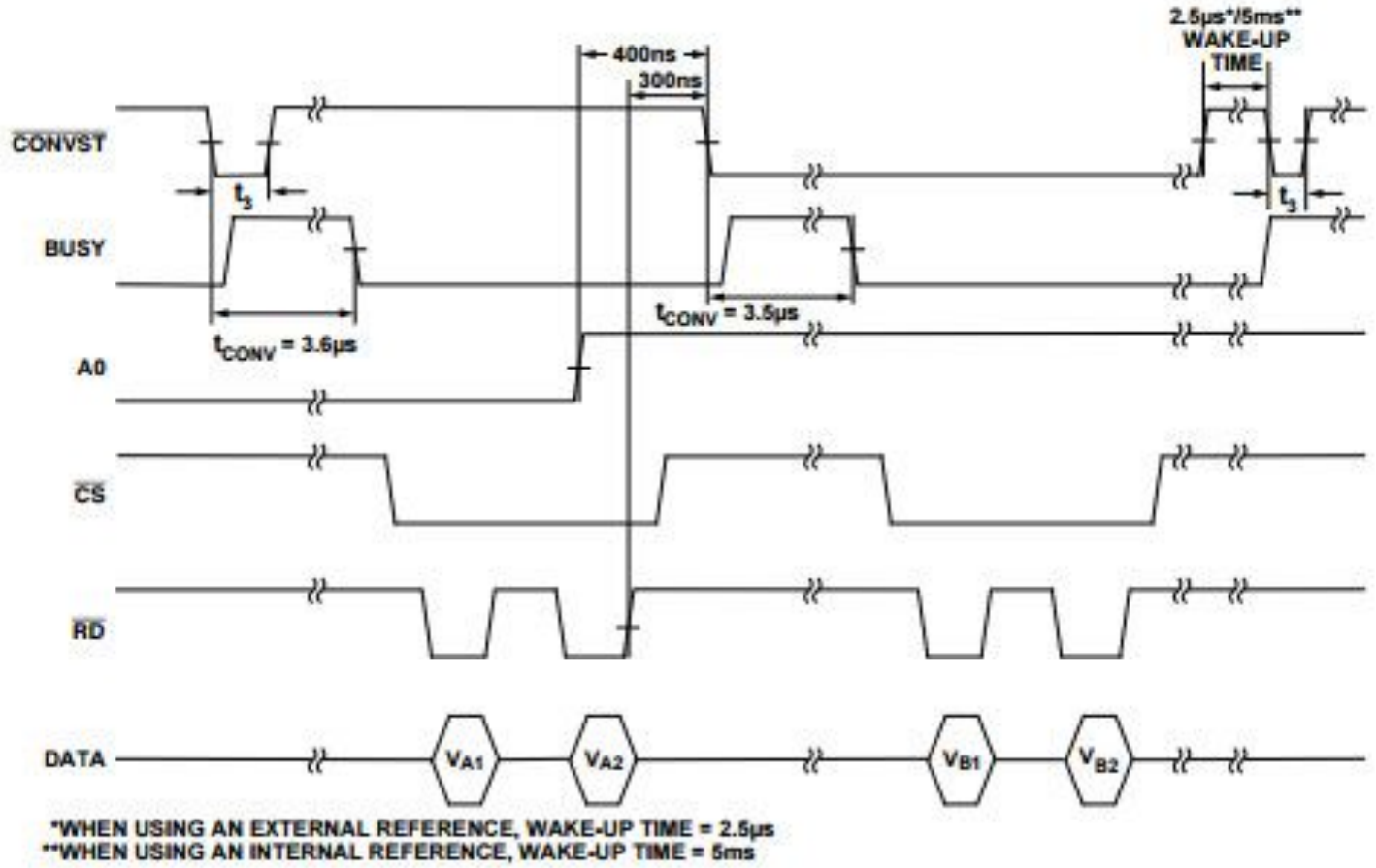


Figure 6. Mode 2 Timing Where Automatic Sleep Function Is Initiated

ПОСЛЕДОВАТЕЛЬНЫЙ ИНТЕРФЕЙС ПОЗВОЛЯЕТ РЕЗКО СОКРАТИТЬ ЧИСЛО ВЫВОДОВ МИКРОСХЕМЫ

ANALOG DEVICES

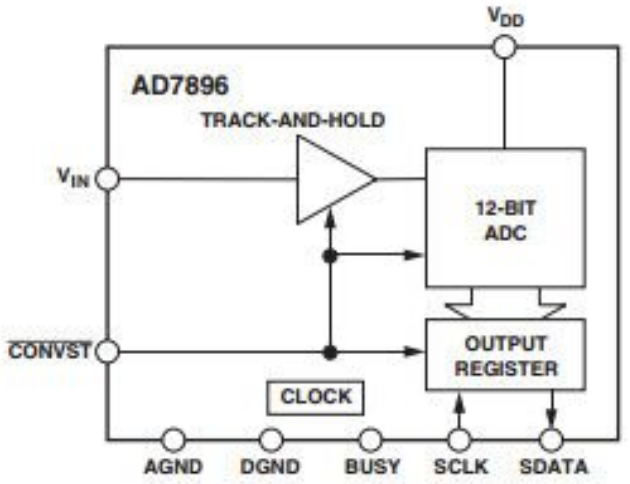
2.7 V to 5.5 V, 12-Bit, 8 µs ADC in 8-Lead SOIC/PDIP

AD7896

FEATURES

- 100 kHz Throughput Rate
- Fast 12-Bit Sampling ADC with 8 µs Conversion Time
- 8-Lead PDIP and SOIC
- Single 2.7 V to 5.5 V Supply Operation
- High Speed, Easy-to-Use Serial Interface
- On-Chip Track-and-Hold Amplifier
- Analog Input Range Is 0 V to Supply
- High Input Impedance
- Low Power: 9 mW Typ

FUNCTIONAL BLOCK DIAGRAM



ВРЕМЕННЫЕ ДИАГРАММЫ АЦП AD7896 (РАЗДЕЛЬНЫЕ ПРОЦЕССЫ ПРЕОБРАЗОВАНИЯ И ВЫДАЧИ КОДОВОГО РЕЗУЛЬТАТА)

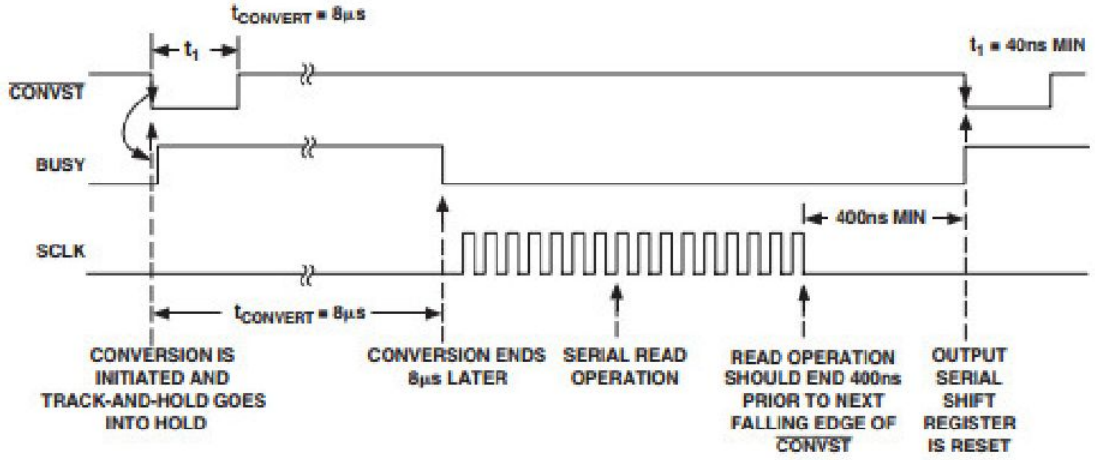


Figure 2. Mode 1 Timing Operation Diagram for High Sampling Performance

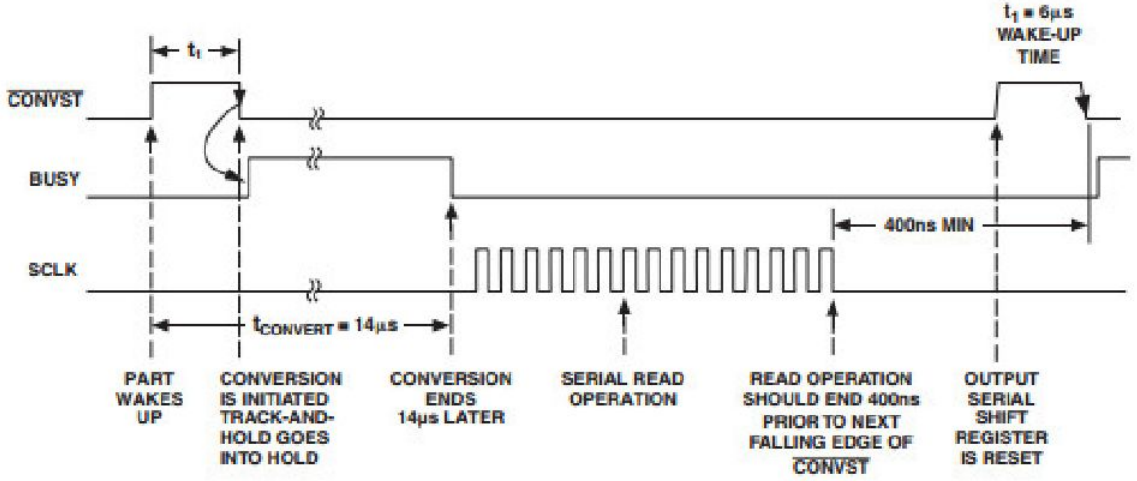


Figure 3. Mode 2 Timing Diagram Where Automatic Sleep Function Is Initiated

МИКРОСХЕМА АЦП БЕЗ ВЫВОДА BUSY

ANALOG DEVICES

1 MSPS, Ultralow Power, 12-Bit ADC in 8-Lead LFCSP

Data Sheet **AD7091**

FEATURES

- Fast throughput rate of 1 MSPS
- Specified for V_{DD} of 2.09 V to 5.25 V
- INL of ±1 LSB maximum
- Analog input range of 0 V to V_{DD}
- Ultralow power
  - 367 µA typical at 3 V and 1 MSPS
  - 324 nA typical at 3 V in power-down mode
- Reference provided by V_{DD}
- Flexible power/throughput rate management
- High speed serial interface: SPI®-/QSPI™-/MICROWIRE®-/DSP-compatible
- Busy indicator
- Power-down mode
- 8-lead, 2 mm × 2 mm LFCSP package
- Temperature range: −40°C to +125°C

APPLICATIONS

- Battery-powered systems
  - Handheld meters
  - Medical instruments
  - Mobile communications
- Instrumentation and control systems
- Data acquisition systems
- Optical sensors
- Diagnostic/monitoring functions
- Energy harvesting

FUNCTIONAL BLOCK DIAGRAM

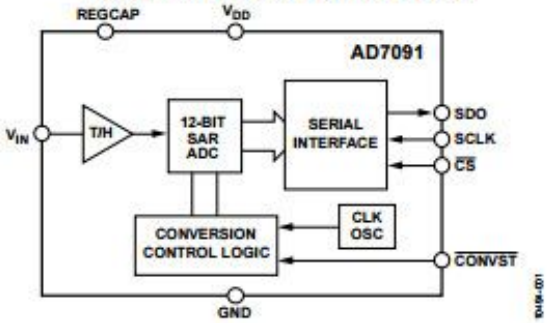


Figure 1.

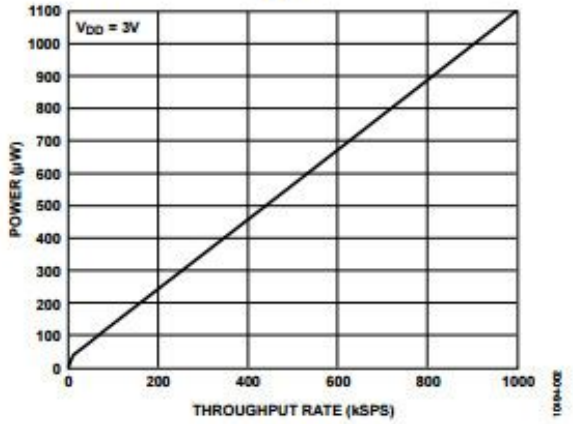


Figure 2. Power Dissipation vs. Throughput Rate

ОРГАНИЗАЦИЯ ПРЕРЫВАНИЯ ПО ГОТОВНОСТИ АЦП AD7091

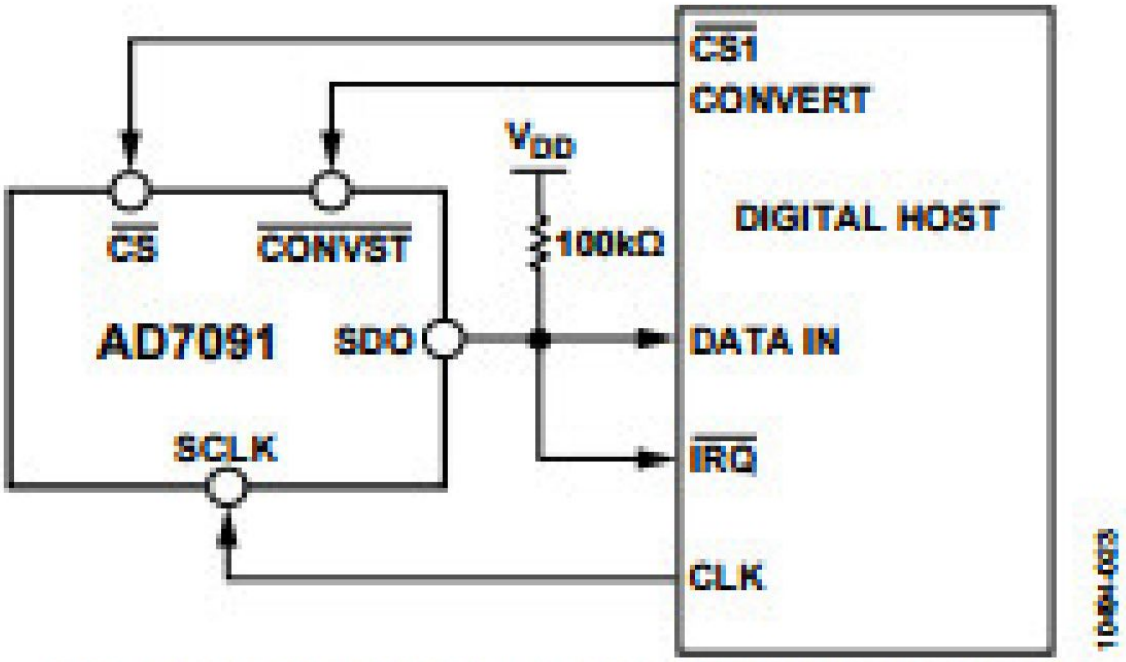


Figure 25. Connection Diagram with Busy Indicator

ВРЕМЕННЫЕ ДИАГРАММЫ АЦП AD7091 С СИГНАЛИЗАЦИЕЙ ГОТОВНОСТИ ПО ВЫВОДУ SDO

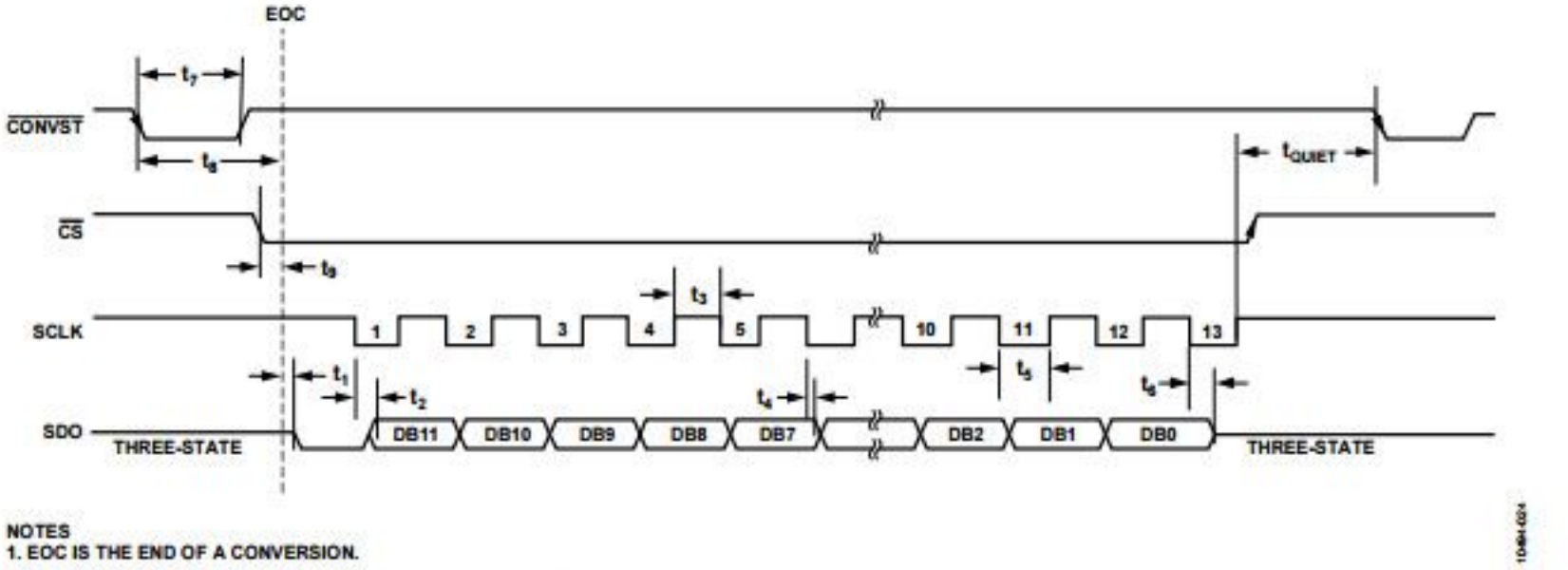


Figure 26. Serial Port Timing with Busy Indicator

Сигнал CS должен быть подан до готовности АЦП

МИКРОСХЕМЫ АЦП С СОВМЕЩЁННЫМИ ПРОЦЕССАМИ ПРЕОБРАЗОВАНИЯ И ВЫДАЧИ КОДОВОГО РЕЗУЛЬТАТА НЕ ТРЕБУЮТ СИГНАЛОВ ЗАПУСКА И ГОТОВНОСТИ

ANALOG DEVICES

Differential Input, 555 kSPS 12-Bit ADC in an 8-Lead SOT-23

Data Sheet

AD7452

FEATURES

- Specified for V_{DD} of 3 V and 5 V
- Low power at max throughput rate
  - 3.3 mW max at 555 kSPS with 3 V supplies
  - 7.25 mW max at 555 kSPS with 5 V supplies
- Fully differential analog input
- Wide input bandwidth
  - 70 dB SINAD at 100 kHz input frequency
- Flexible power/serial clock speed management
- No pipeline delays
- High speed serial interface
  - SPI/QSPI™/MICROWIRE™/DSP compatible
- Power-down mode: 1 µA max
- 8-lead SOT-23 package

APPLICATIONS

- Transducer interface
- Battery-powered systems
- Data acquisition systems
- Portable instrumentation
- Motor control

FUNCTIONAL BLOCK DIAGRAM

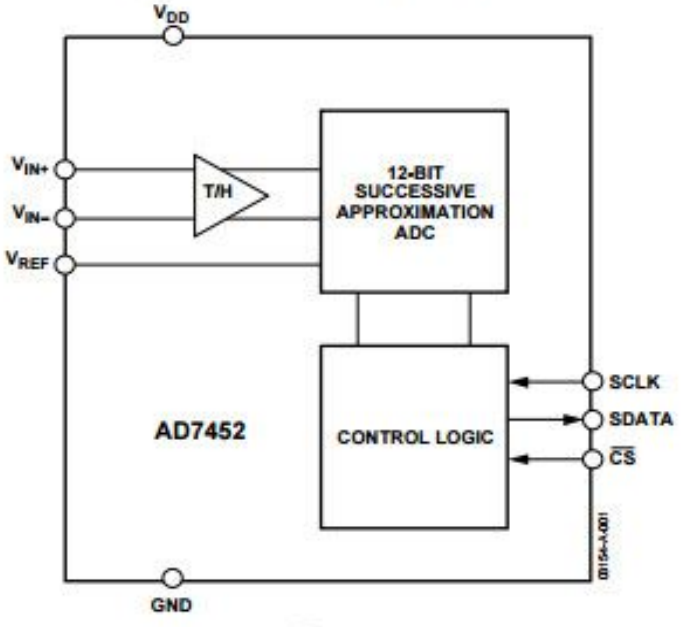


Figure 1.

ВРЕМЕННЫЕ ДИАГРАММЫ АЦП AD7452 С СОВМЕЩЁННЫМИ ПРОЦЕССАМИ ПРЕОБРАЗОВАНИЯ И ВЫДАЧИ КОДОВОГО РЕЗУЛЬТАТА

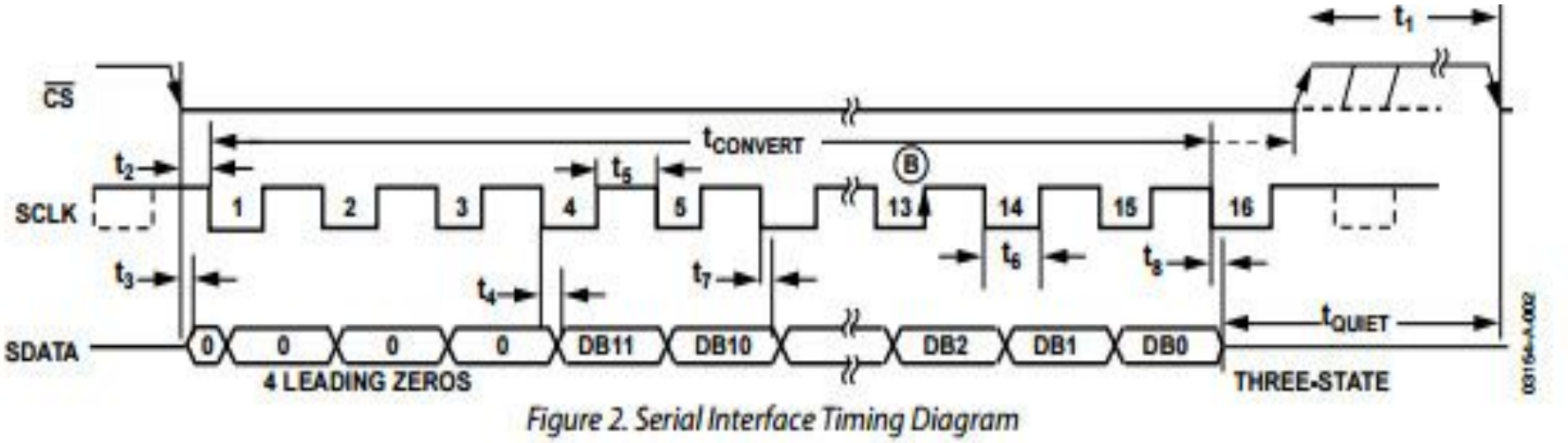


Figure 2. Serial Interface Timing Diagram

Сигнал CS переводит устройство выборки/хранения в режим хранения, инициализирует регистр последовательных приближений и выводит цепь SDATA из состояния высокого импеданса.

По такой структуре могут строиться микросхемы АЦП с шестью выводами.

В ОПИСАНИИ АЦП AD7476/AD7477/AD7478 ОБСУЖДЕНЫ ПРОБЛЕМЫ СОПРЯЖЕНИЯ ПРИ СОВМЕЩЁННОМ РЕЖИМЕ

SERIAL INTERFACE

Figure 23, Figure 24, and Figure 25 show the detailed timing diagrams for serial interfacing to the AD7476, AD7477, and AD7478, respectively. The serial clock provides the conversion clock and controls the transfer of information from the part during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, takes the bus out of three-state, and samples the analog input at this point. The conversion initiates and requires 16 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed, the track-and-hold goes back into track on the next SCLK rising edge as shown at Point B in Figure 23, Figure 24, and Figure 25. On the sixteenth SCLK falling edge, the SDATA line will go back into three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion terminates and the SDATA line goes back into three-state; otherwise, SDATA returns to three-state on the 16th SCLK falling edge as shown in Figure 23, Figure 24, and Figure 25.

Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7476/AD7477/AD7478.

$\overline{CS}$ going low provides the first leading zero to be read by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with the second leading zero. Thus, the first falling clock edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. The final bit in the data transfer is valid on the 16th falling edge, having clocked out on the previous (15th) falling edge. In applications with a slower SCLK, it is possible to read data on each SCLK rising edge, although the first leading zero has to be read on the first SCLK falling edge after the $\overline{CS}$ falling edge. Therefore, the first rising edge of SCLK after the $\overline{CS}$ falling edge provides the second leading zero. The 15th rising SCLK edge has DB0 provided or the final zero for the AD7477 and AD7478. This may not work with most microcontrollers/DSPs, but could possibly be used with FPGAs and ASICs.

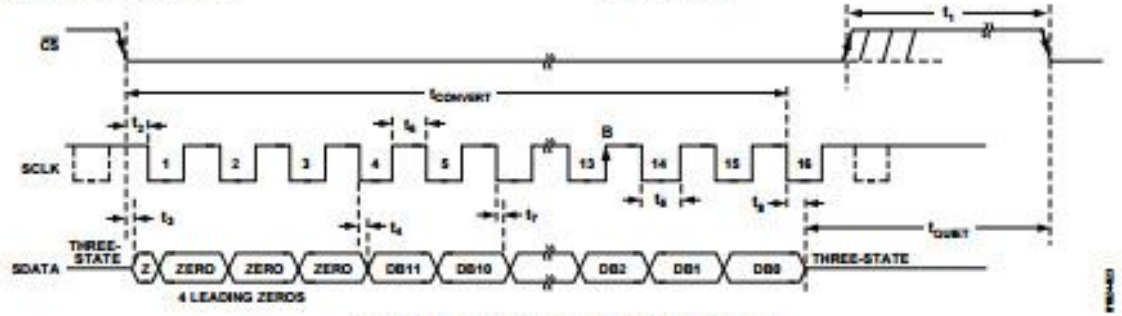


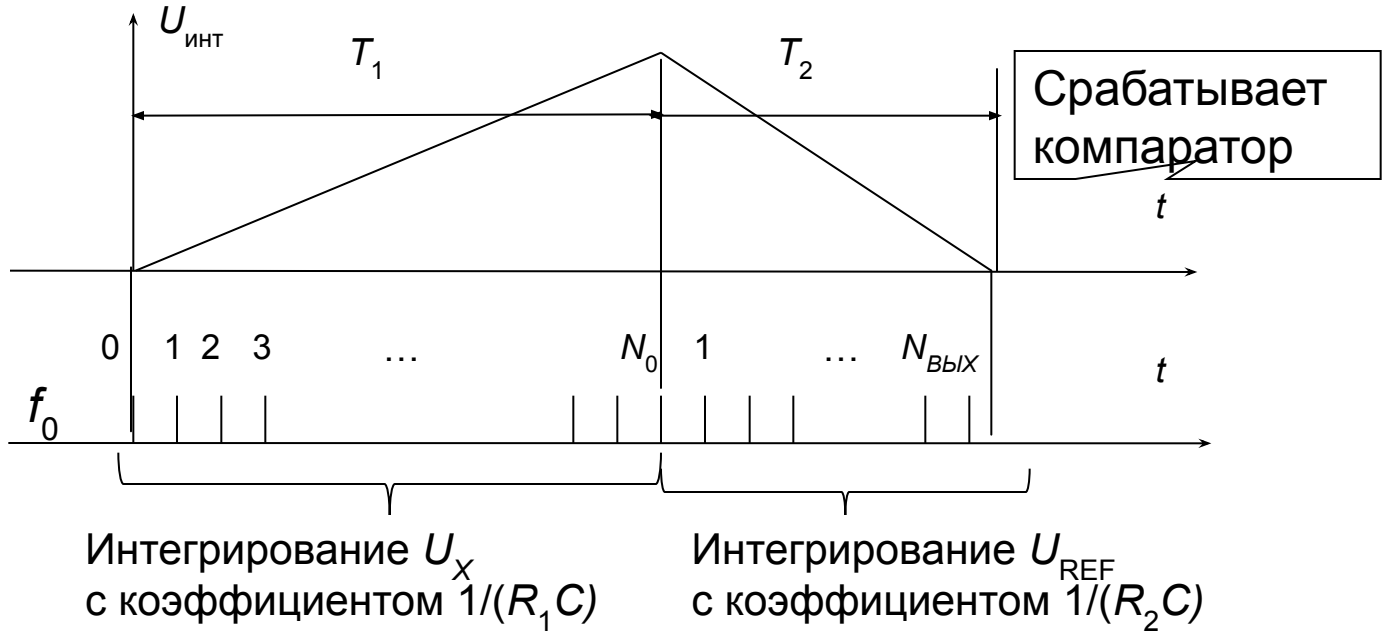
Figure 23. AD7476 Serial Interface Timing Diagram

АЦП СО СРАВНЕНИЕМ ИНТЕГРАЛОВ ПРЕОБРАЗУЕМОГО И ОПОРНОГО НАПРЯЖЕНИЙ

Два важнейших принципа построения АЦП со сравнением интегралов:

- Двухтактное (многотактное) интегрирование
  - В лабораторных цифровых вольтметрах и мультиметрах
  - В микросхемах АЦП, предназначенных для портативных мультиметров и других переносных приборов (термометров, люксметров…) с питанием от гальванических элементов
- Сигма-дельта (ΣΔ) –модуляция
  - В микросхемах АЦП, предназначенных для аудиотехники
  - В низкочастотных измерительных микросхемах АЦП общего назначения
  - В специализированных измерительных микросхемах
  - В микросхемах ΣΔ-модуляторов, не являющихся АЦП

ДВУХТАКТНОЕ ИНТЕГРИРОВАНИЕ



$T_1 = N_0/f_0$ (точно).

$T_2 \approx N_{вых}/f_0$ (с погрешностью квантования).

$N_{вых}/N_0 \approx T_2/T_1$ независимо от частоты f_0.

ВЫВОД ОКОНЧАТЕЛЬНОЙ ФОРМУЛЫ

Из условия возврата интегратора в исходное состояние (полярность U_{REF} противоположна U_x)

$$\frac{T_1}{R_1 C} U_x + \frac{T_2}{R_2 C} U_{REF} = 0.$$

Отсюда, независимо от C,

$$\frac{T_2}{T_1} = \frac{R_2}{R_1} \left| \frac{U_x}{U_{REF}} \right| \approx \frac{N_{ВЫХ}}{N_0}.$$

Окончательно, независимо от f_o и C, с погрешностью квантования, не превышающей одного импульса,

$$N_{ВЫХ} \approx N_0 \frac{R_2}{R_1} \left| \frac{U_x}{U_{REF}} \right|.$$

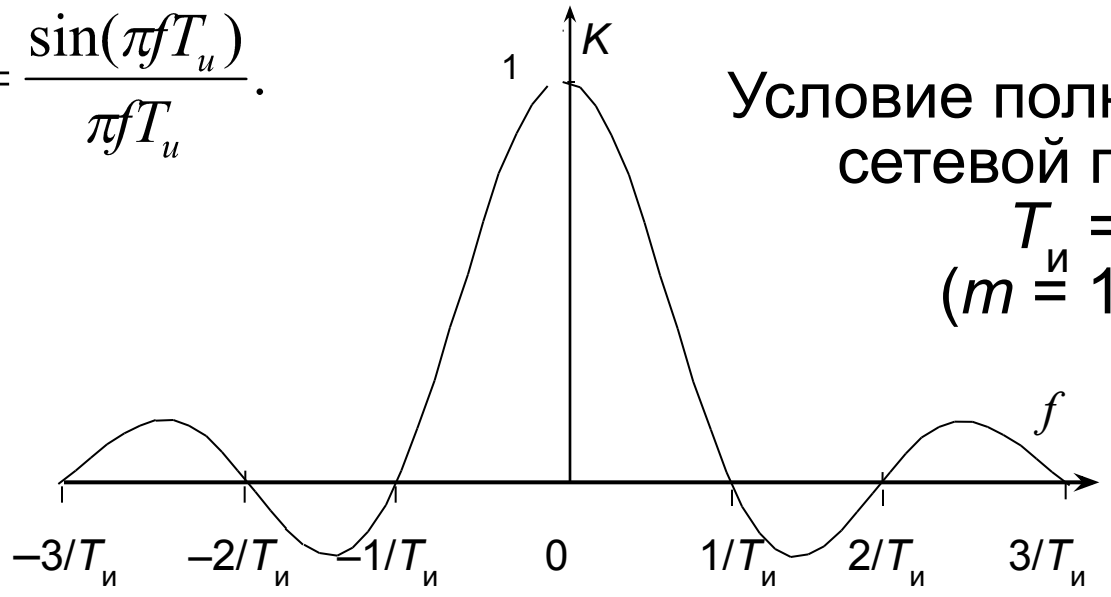
Частоту тактовых импульсов можно изменять, изменяя тем самым время интегрирования T_1 (далее − измерительный интервал T_u), не внося погрешности в результат преобразования!

АЦП ДВУХТАКТНОГО ИНТЕГРИРОВАИЯ ИМЕЮТ СВОЙСТВА ЧАСТОТНОГО ФИЛЬТРА

Интегрирование U_x за время $T_и$ и индикация полученного *среднего значения* напряжения эквивалентны фильтрации входного сигнала с прямоугольной весовой функцией, имеющей ширину $T_и$.

Соответствующая амплитудно- частотная характеристика − функция sinc.

$$K = \frac{\sin(\pi f T_u)}{\pi f T_u}.$$

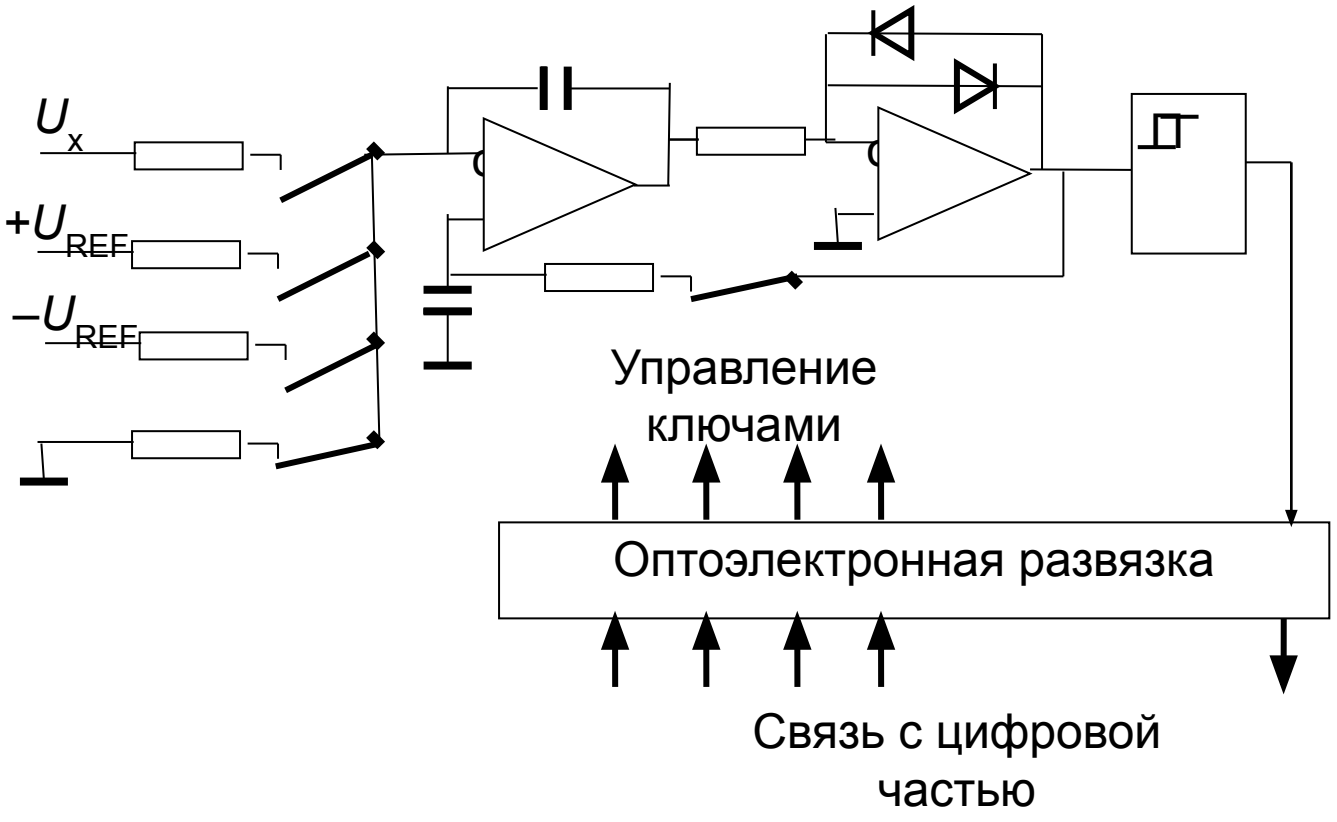


Условие полного подавления сетевой помехи ($f_{сети}$):

$T_и = m/f_{сети}$

(m = 1, 2, 3,…).

АНАЛОГОВЫЙ БЛОК АЦП ДВУХТАКТНОГО ИНТЕГРИРОВАНИЯ
(МОДУЛЯ КАМАК ЗАВОДА «ВИБРАТОР»)



АНАЛОГОВАЯ ЧАСТЬ МИКРОСХЕМЫ КР572ПВ2

(По книге: Гутников, 1988, с. 256)

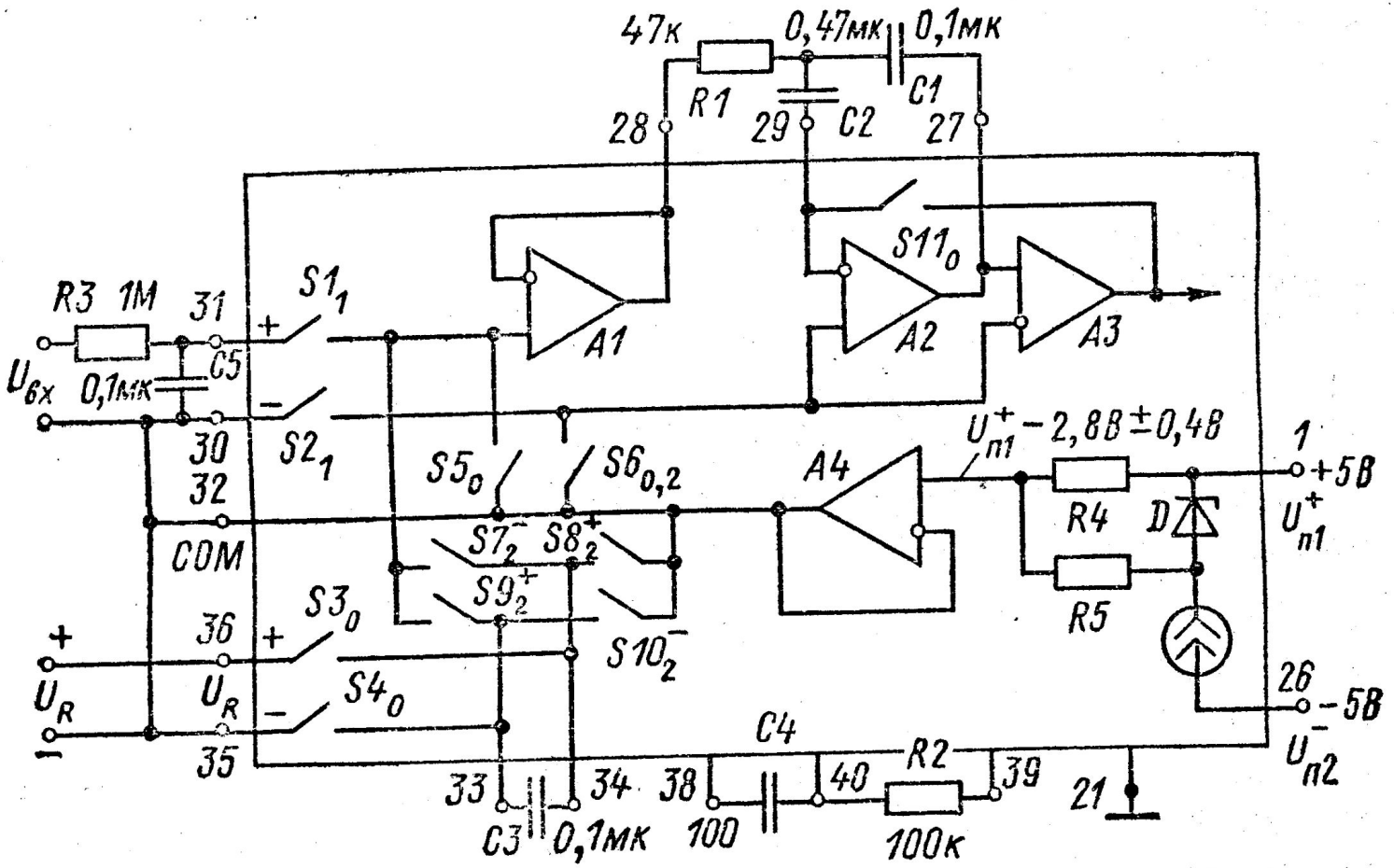


Рис. 10.3. Схема аналоговой части интегрирующего АЦП КР572ПВ2

СХЕМЫ ВКЛЮЧЕНИЯ МИКРОСХЕМЫ КР572ПВ2

(По книге: Гутников, 1988, с. 260)

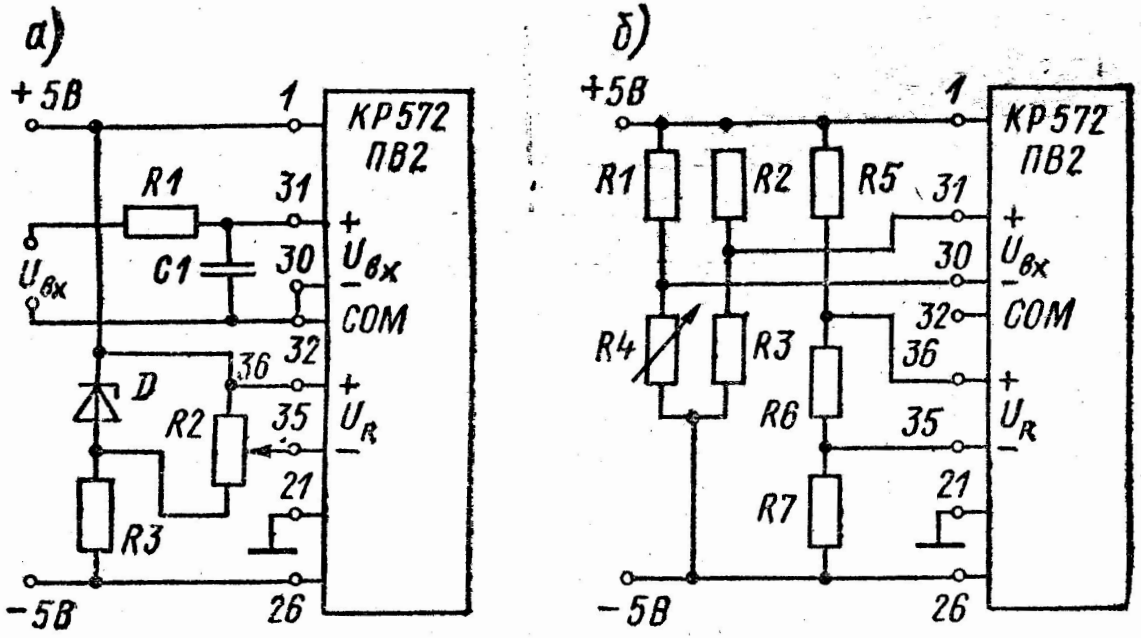


Рис. 10.4. Схемы входных цепей АЦП КР572ПВ2

АНАЛОГОВАЯ ЧАСТЬ МИКРОСХЕМ АЦП ФИРМЫ MAXIM

3½ Digit A/D Converter

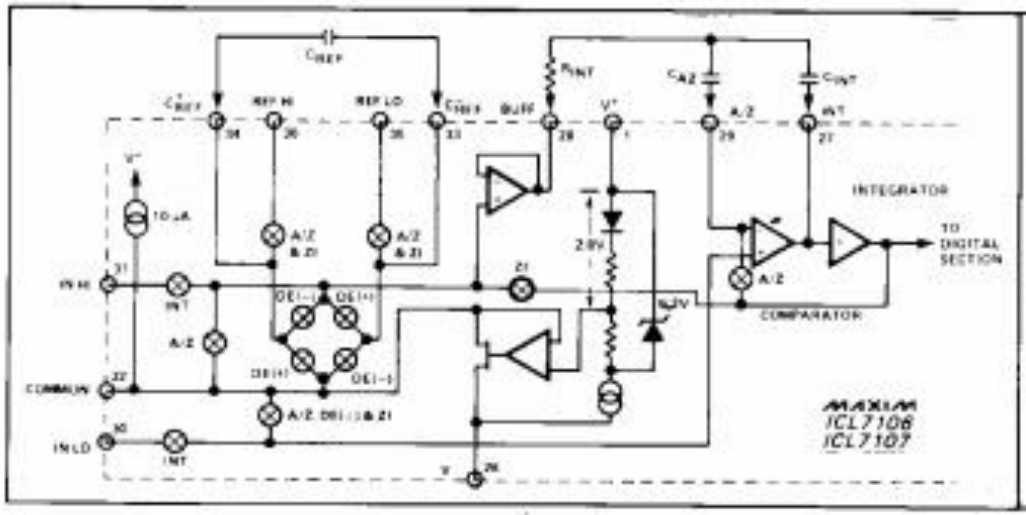


Figure 3. Analog Section of ICL7106/ICL7107

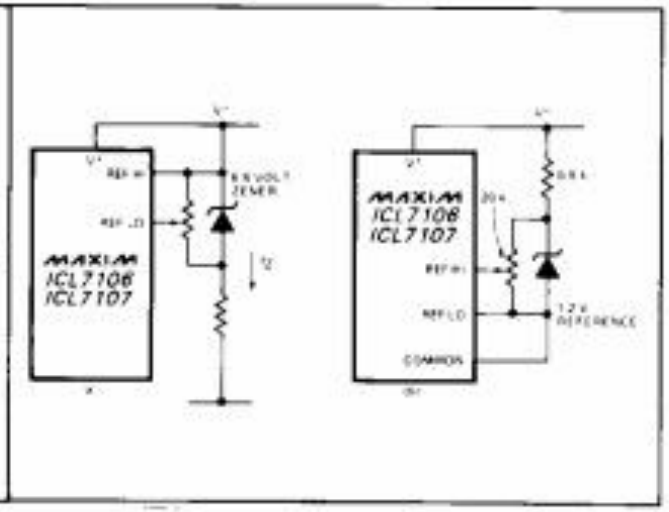


Figure 4. Using an External Reference

ICL7106/7107

ЦИФРОВАЯ ЧАСТЬ МИКРОСХЕМ АЦП ФИРМЫ MAXIM

(С выходом на жидкокристаллический индикатор)

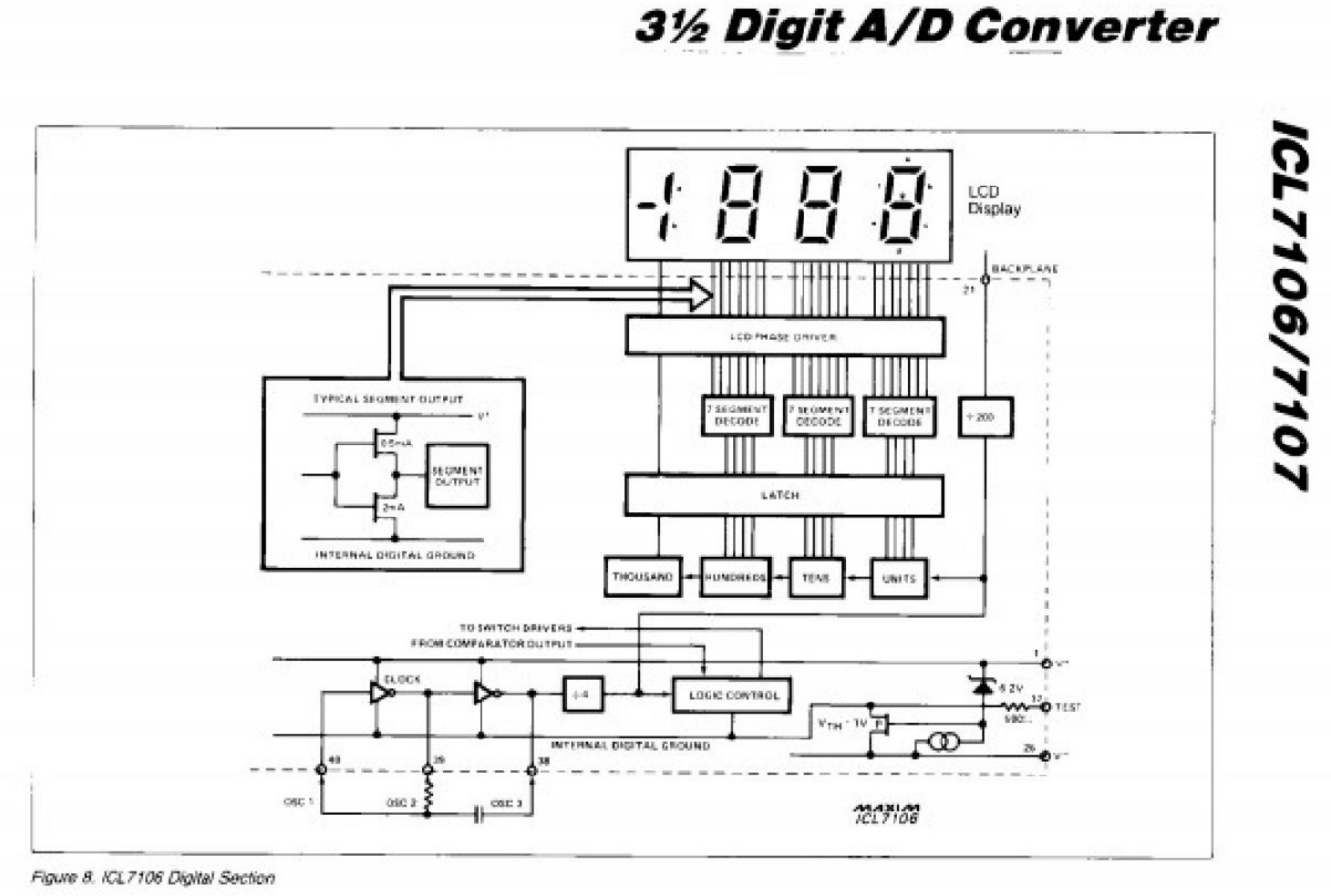


Figure 8. ICL7106 Digital Section

СХЕМЫ ВКЛЮЧЕНИЯ МИКРОСХЕМ АЦП ФИРМЫ MAXIM

ICL7106/7107

3½ Digit A/D Converter

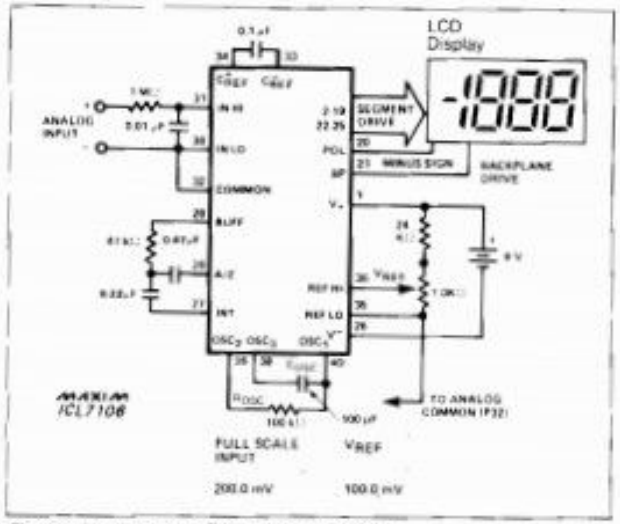


Figure 1. Maxim ICL7106 Typical Operating Circuit

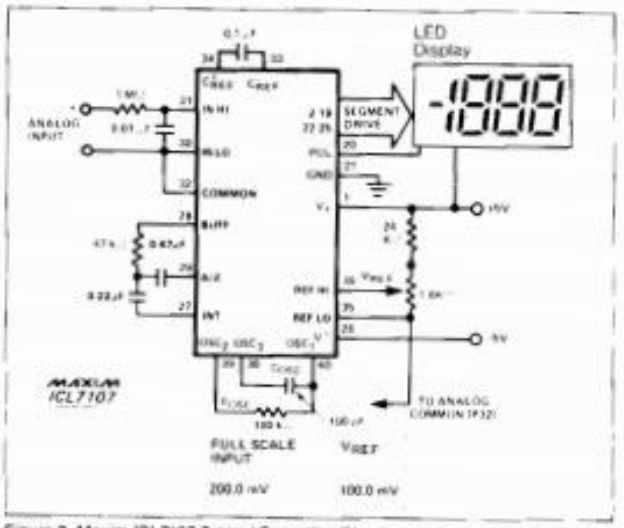


Figure 2. Maxim ICL7107 Typical Operating Circuit

Управление положением десятичной точки с помощью элементов ИСКЛЮЧАЮЩЕЕ ИЛИ

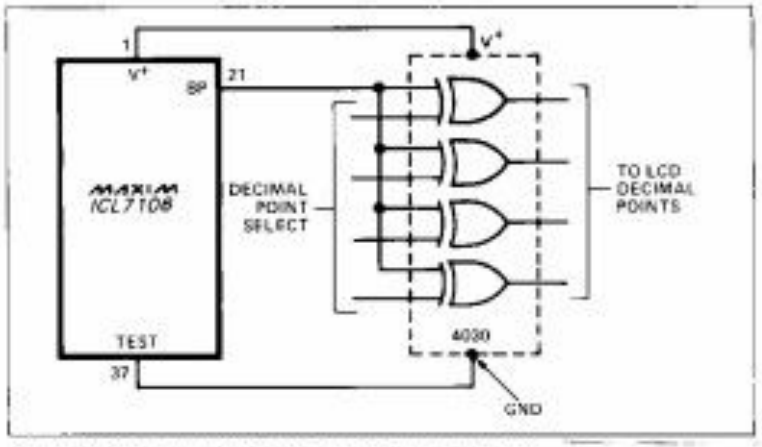


Figure 6. Exclusive "OR" Gate for Decimal Point Drive

ΣΔ-МОДУЛЯЦИЯ

Происхождение термина:

- ***Дельта-модуляцией*** было названо кодирование приращений напряжения. В каждом такте 1 или 0 означали положительное или отрицательное приращения, как в АЦП следящего уравновешивания.
- ***Сигма-дельта-модуляцией*** назвали кодирование приращений интеграла напряжения. Точно так же в каждом такте формируется 1 или 0; выходной сигнал ΣΔ-модулятора характеризуется как bit stream − поток битов.
- ΣΔ-модулятор похож на преобразователь напряжение→частота с формированием импульса обратной связи тактовым генератором, но может содержать не один, а несколько интеграторов. Сигнал обратной связи обычно биполярный: $\pm U_{REF}$.

ΣΔ-МОДУЛЯТОР И ПОСТРОЕННЫЙ НА НЁМ АЦП

Простейшая структура ΣΔ-модулятора из описания микросхемы АЦП AD7716

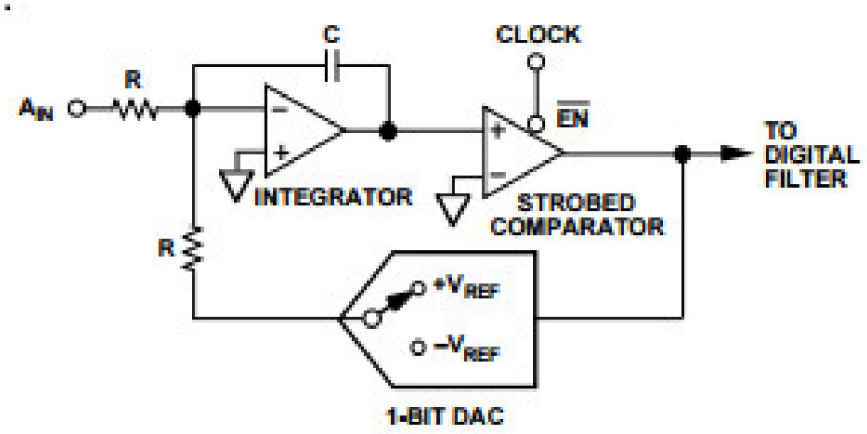


Figure 5. First Order Modulator

В действительности интегратор может быть построен на переключаемых конденсаторах

Структура канала аналого-цифрового преобразования из описания микросхемы электросчётчика ADE7953

ANALOG-TO-DIGITAL CONVERSION

The analog-to-digital conversion in the ADE7953 is performed by three second-order Σ-Δ modulators. For the sake of clarity, the block diagram in Figure 36 shows the operation of a first-order Σ-Δ modulator. The analog-to-digital conversion consists of a Σ-Δ modulator followed by a low-pass filter stage.

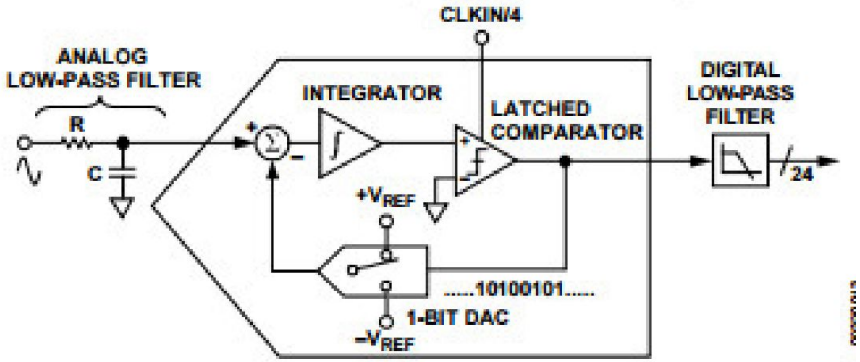


Figure 36. Σ-Δ Conversion

ДОСТОИНСТВА АЦП С ΣΔ-МОДУЛЯТОРАМИ

- Высокая разрядность, обычно 16 или 24 бита, получаемая благодаря многоступенчатой цифровой фильтрации.
- Высокая линейность характеристики: сам модулятор одноразрядный, и нет причин нелинейности.
- «Передискретизация», высокая частота обращений к входному сигналу, многократно превышающая частоту выдачи цифровых результатов.
- Возможность подавления помех определённых частот цифровым фильтром.

НОМЕНКЛАТУРА ИЗМЕРИТЕЛЬНЫХ ΣΔ-АЦП

Измерительные ΣΔ-АЦП очень разнообразны.

- Встречаются микросхемы, содержащие 4, 6 или 8 одновременно работающих измерительных каналов.
- Встречаются микросхемы с мультиплексорами на входе одного канала ΣΔ-модуляции и цифровой фильтрации.
- Встречаются микросхемы с возможностью выбора частоты преобразований, структуры входных цепей, вида характеристики (униполярная или биполярная).
- Встречаются простые одноканальные микросхемы с режимом READ ONLY, с жёстко заданной частотой преобразований.

ПРИМЕР МИКРОСХЕМЫ АЦП СРЕДНЕЙ СЛОЖНОСТИ – AD7790

ANALOG DEVICES

Low Power, 16-Bit Buffered Sigma-Delta ADC

Data Sheet **AD7790**

FEATURES

Power
- Supply: 2.5 V to 5.25 V operation
- Normal: 75 µA maximum
- Power-down: 1 µA maximum

RMS noise: 1.1 µV at 9.5 Hz update rate
16-bit p-p resolution
Integral nonlinearity: 3.5 ppm typical
Simultaneous 50 Hz and 60 Hz rejection
Internal clock oscillator
Programmable gain amplifier
Rail-to-rail input buffer
V_{DD} monitor channel
Temperature range: −40°C to +105°C
10-lead MSOP

INTERFACE

3-wire serial
SPI®, QSPI™, MICROWIRE™, and DSP compatible
Schmitt trigger on SCLK

APPLICATIONS

Smart transmitters
Battery applications
Portable instrumentation
Sensor measurement
Temperature measurement
Pressure measurement
Weigh scales
4 to 20 mA loops

FUNCTIONAL BLOCK DIAGRAM

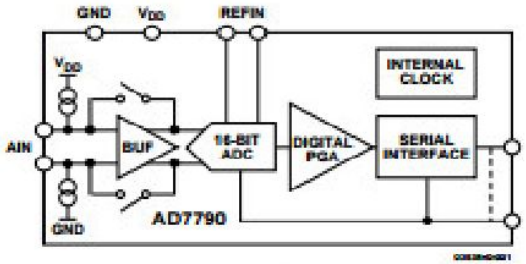


Figure 1.

GENERAL DESCRIPTION

The AD7790 is a low power, complete analog front end for low frequency measurement applications. It contains a low noise 16-bit ∑-Δ ADC with one differential input that can be buffered or unbuffered along with a digital PGA, which allows gains of 1, 2, 4, and 8.

The device operates from an internal clock. Therefore, the user does not have to supply a clock source to the device. The output data rate from the part is software programmable and can be varied from 9.5 Hz to 120 Hz, with the rms noise equal to 1.1 µV at the lower update rate. The internal clock frequency can be divided by a factor of 2, 4, or 8, which leads to a reduction in the current consumption. The update rate, cutoff frequency, and settling time will scale with the clock frequency.

The part operates with a power supply from 2.5 V to 5.25 V.

ОПИСАНИЕ ВЫВОДОВ АЦП AD7790 (НАЧАЛЬНАЯ ЧАСТЬ)

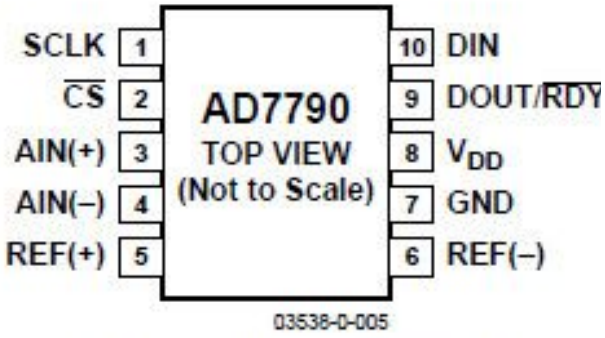


Figure 5. Pin Configuration

Обратим внимание
на детали описания:
SCLK можно подавать
непрерывно или порциями;
CS можно жёстко соединить
с общей шиной.
При проектировании нужно
внимательно проработать
описание всех выводов
микросхемы!

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	SCLK	Serial Clock Input for Data Transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data.
2	$\overline{CS}$	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device.

ВОЗМОЖНАЯ СХЕМА ВКЛЮЧЕНИЯ АЦП AD7790

(Интерфейс изображён ошибочно)

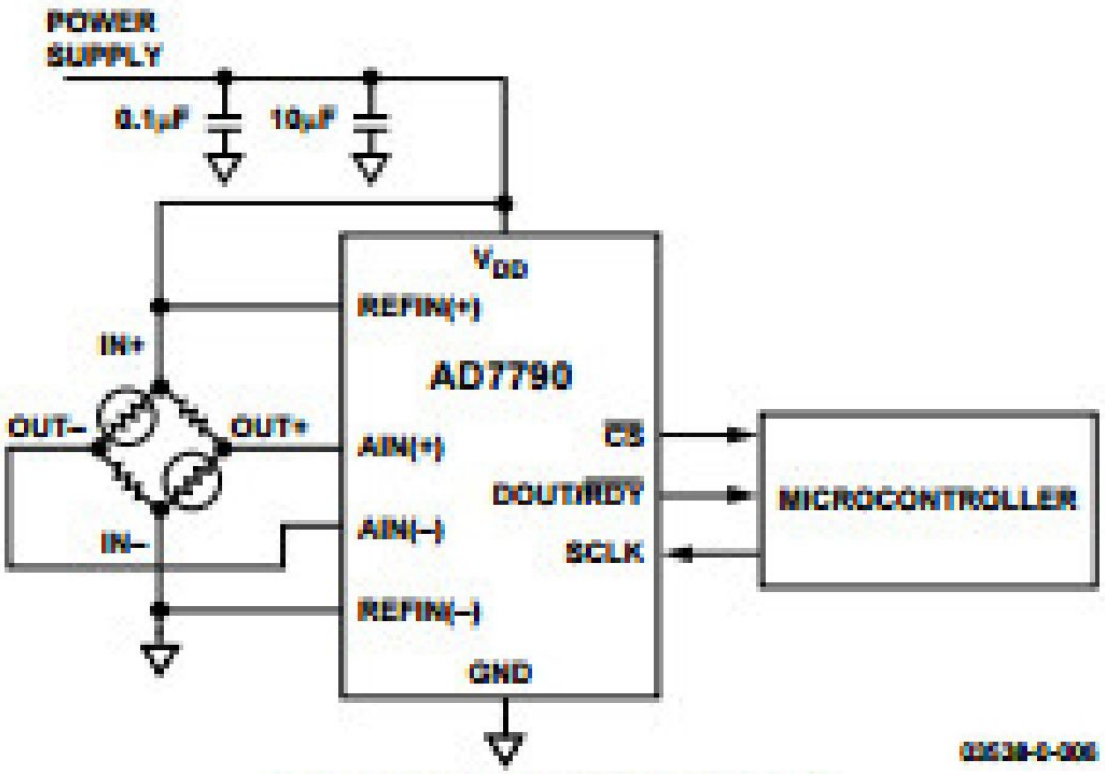


Figure 7. Basic Connection Diagram

ЧАСТОТНАЯ ХАРАКТЕРИСТИКА АЦП ПРИ ЧАСТОТЕ ВЫДАЧИ ЦИФРОВЫХ РЕЗУЛЬТАТОВ 16,6 ГЦ

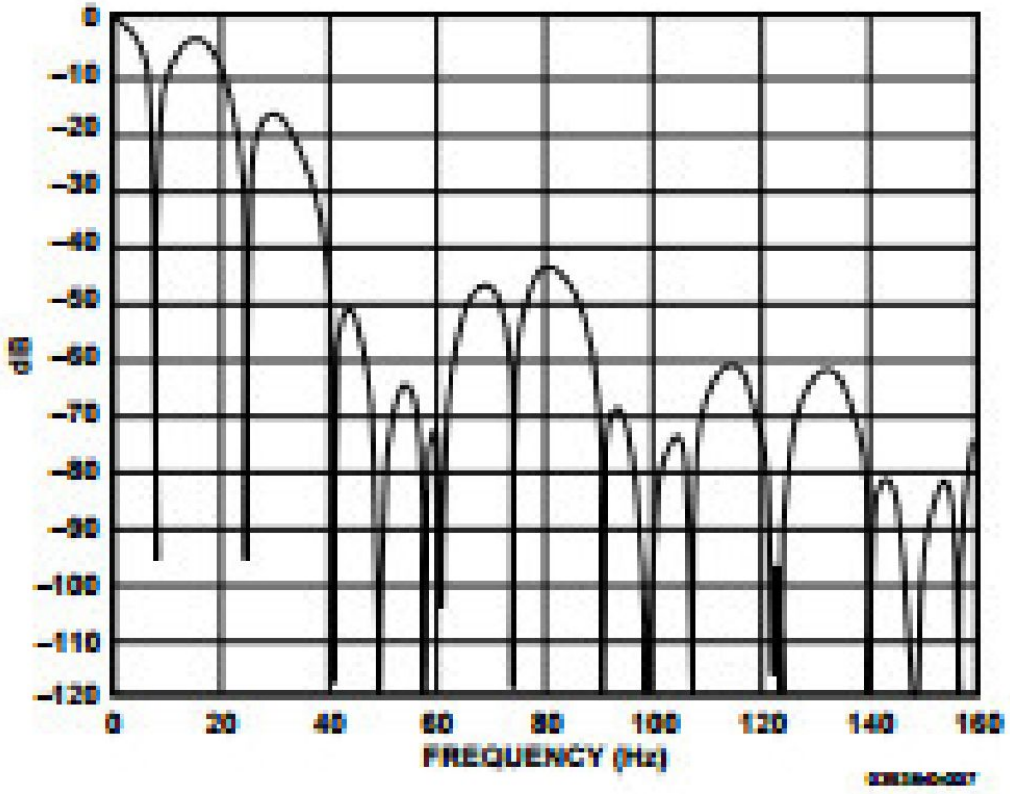


Figure 6. Frequency Response for a 16.6 Hz Update Rate

КОММУНИКАЦИОННЫЙ РЕГИСТР МИКРОСХЕМЫ AD7790

(Общение с микросхемой начинается с записи в него!)

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$(0)	0(0)	RS1(0)	RS0(0)	R/$\overline{\text{W}}$(0)	CREAD(0)	CH1(0)	CH0(0)

Table 5. Communications Register Bit Designations

Bit Location	Bit Name	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so that the write to the communications register actually occurs. If a 1 is the first bit written, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits will be loaded to the communications register.
CR6	0	This bit must be programmed to Logic 0 for correct operation.
CR5–CR4	RS1–RS0	Register Address Bits. These address bits are used to select which of the ADC's registers are being selected during this serial interface communication. See Table 6.
CR3	R/$\overline{\text{W}}$	A 0 in this bit location indicates that the next operation will be a write to a specified register. A 1 in this position indicates that the next operation will be a read from the designated register.
CR2	CREAD	Continuous Read of the Data Register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read, i.e., the contents of the data register are placed on the DOUT pin automatically when the SCLK pulses are applied. The communications register does not have to be written to for data reads. To enable continuous read mode, the instruction 001111XX must be written to the communications register. To exit the continuous read mode, the instruction 001110XX must be written to the communications register while the $\overline{\text{RDY}}$ pin is low. While in continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit continuous read mode. Additionally, a reset will occur if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.
CR1–CR0	CH1–CH0	These bits are used to select the analog input channel. The differential channel can be selected (AIN(+)/AIN(–)) or an internal short (AIN(–)/AIN(–)) can be selected. Alternatively, the power supply can be selected, i.e., the ADC can measure the voltage on the power supply, which is useful for monitoring power supply variation. The power supply voltage is divided by 5 and then applied to the modulator for conversion. The ADC uses a 1.17 V ± 5% on-chip reference as the reference source for the analog to digital conversion. Any change in channel resets the filter and a new conversion is started.

АДРЕСАЦИЯ РЕГИСТРОВ МИКРОСХЕМЫ AD7790

Table 6. Register Selection

RS1	RS0	Register	Register Size
0	0	Communications Register during a Write Operation	8-Bit
0	0	Status Register during a Read Operation	8-Bit
0	1	Mode Register	8-Bit
1	0	Filter Register	8-Bit
1	1	Data Register	16-Bit

РЕГИСТР РЕЖИМА МИКРОСХЕМЫ AD7790

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
MD1(0)	MD0(0)	G1(0)	G0(0)	BO(0)	0(0)	BUF(1)	0(0)

Table 10. Operating Modes

MD1	MD0	Mode
0	0	Continuous Conversion Mode (Default)
0	1	Reserved
1	0	Single Conversion Mode
1	1	Power-Down Mode

Table 11. Analog Input Ranges

G1	G0	Range	AD7790 LSB Size with V_{REF} = +2.5 V (μV)
0	0	$\pm V_{REF}$	76.3
0	1	$\pm V_{REF}/2$	38.14
1	0	$\pm V_{REF}/4$	19.07
1	1	$\pm V_{REF}/8$	9.54

BO − burnout current
BUF − buffer

РЕГИСТР ФИЛЬТРА МИКРОСХЕМЫ AD7790

FR7	FR6	FR5	FR4	FR3	FR2	FR1	FR0
0(0)	0(0)	CDIV1(0)	CDIV0(0)	0(0)	FS2(1)	FS1(0)	FS0(0)

Table 12. Filter Register Bit Designatins

Bit Location	Bit Name	Description
FR7–FR6	0	These bits must be programmed with a Logic 0 for correct operation.
FR5–FR4	CLKDIV1–CDIV0	These bits are used to operate the AD7790 in the lower power modes. The clock is internally divided and the power is reduced. 00 Normal Mode 01 Clock Divided by 2 10 Clock Divided by 4 11 Clock Divided by 8
FR3	0	This bit must be programmed with a Logic 0 for correct operation.
FR2–FR0	FS2–FS0	These bits set the output word rate of the ADC. The update rate influences the 50 Hz/60 Hz rejection and noise. The noise is the same for all gain settings. See Table 13 for the allowable update rates in full power mode. In the low power modes, the update rates will be reduced. (See Reduced Current Modes.)

Table 13. Update Rates

FS2	FS1	FS0	f_{ADC} (Hz)	f3dB (Hz)	RMS Noise (μV)	Rejection
0	0	0	120	28	40	25 dB @ 60 Hz
0	0	1	100	24	25	25 dB @ 50 Hz
0	1	0	33.3	8	3.36	
0	1	1	20	4.7	1.6	80 dB @ 60 Hz
1	**0**	**0**	**16.6**	**4**	**1.5**	**65 dB @ 50 Hz/60 Hz (Default Setting)**
1	0	1	16.7	4	1.5	80 dB @ 50 Hz
1	1	0	13.3	3.2	1.2	
1	1	1	9.5	2.3	1.1	62 dB @ 50/60 Hz

АЦП AD7790: ОДНОКРАТНОЕ ПРЕОБРАЗОВАНИЕ

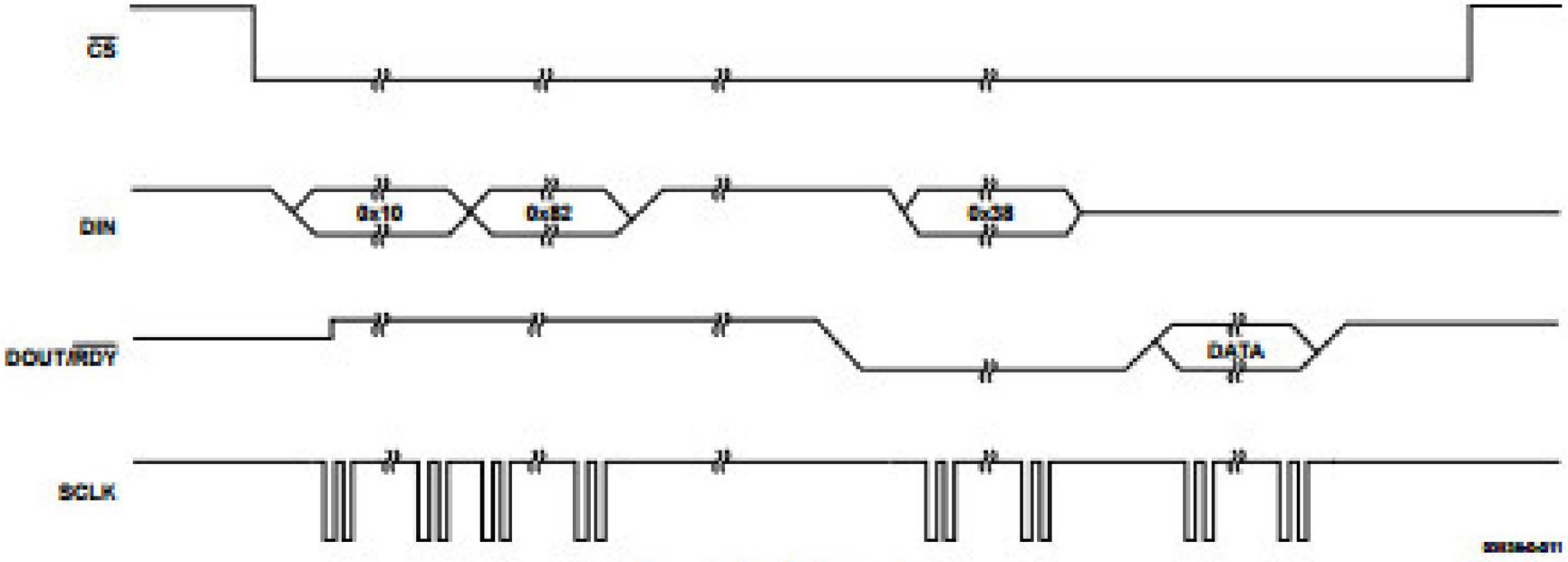


Figure 8. Single Conversion

АЦП AD7790: НЕПРЕРЫВНОЕ ПРЕОБРАЗОВАНИЕ

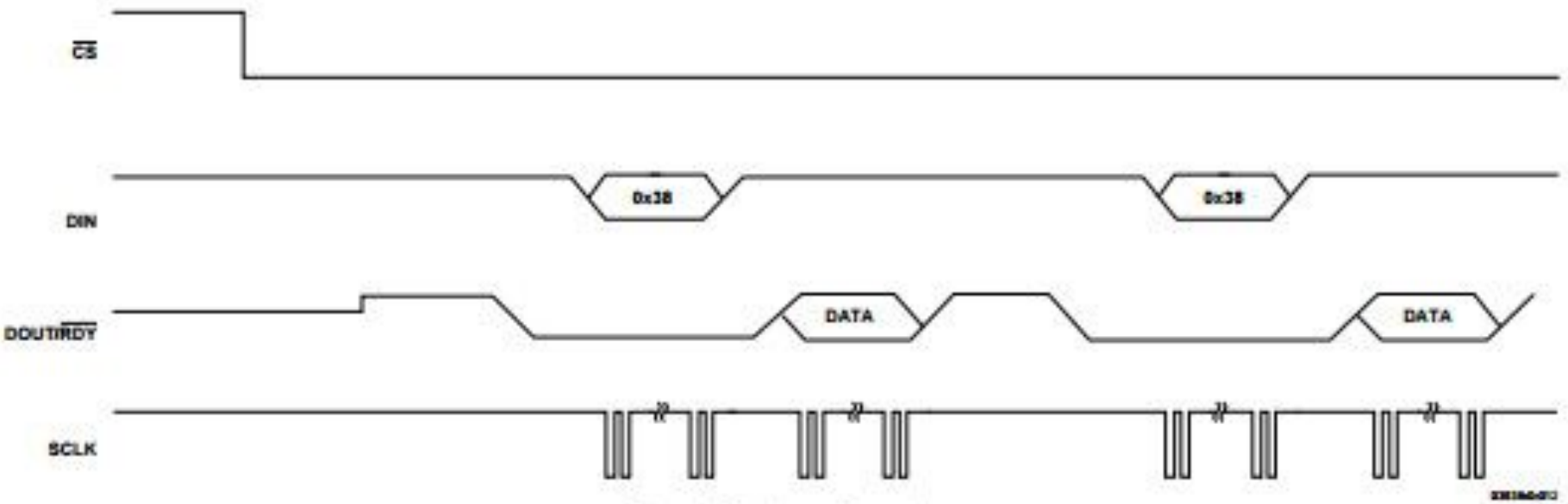


Figure 9. Continuous Conversion

АЦП AD7790: НЕПРЕРЫВНОЕ ЧТЕНИЕ

Continuous Read Mode

Rather than write to the communications register each time a conversion is complete to access the data, the AD7790 can be placed in continuous read mode. By writing 001111XX to the communications register, the user only needs to apply the appropriate number of SCLK cycles to the ADC and the 16-bit word will automatically be placed on the DOUT/$\overline{\text{RDY}}$ line when a conversion is complete.

When DOUT/$\overline{\text{RDY}}$ goes low to indicate the end of a conversion, sufficient SCLK cycles must be applied to the ADC and the data conversion will be placed on the DOUT/$\overline{\text{RDY}}$ line. When the conversion is read, DOUT/$\overline{\text{RDY}}$ will return high until the next conversion is available. In this mode, the data can be read only once. Also, the user must ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion or if insufficient serial clocks are applied to the AD7790 to read the word, the serial output register is reset when the next conversion is complete and the new conversion is placed in the output serial register.

To exit the continuous read mode, the instruction 001110XX must be written to the communications register while the $\overline{\text{RDY}}$ pin is low. While in the continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit the continuous read mode. Additionally, a reset will occur if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.

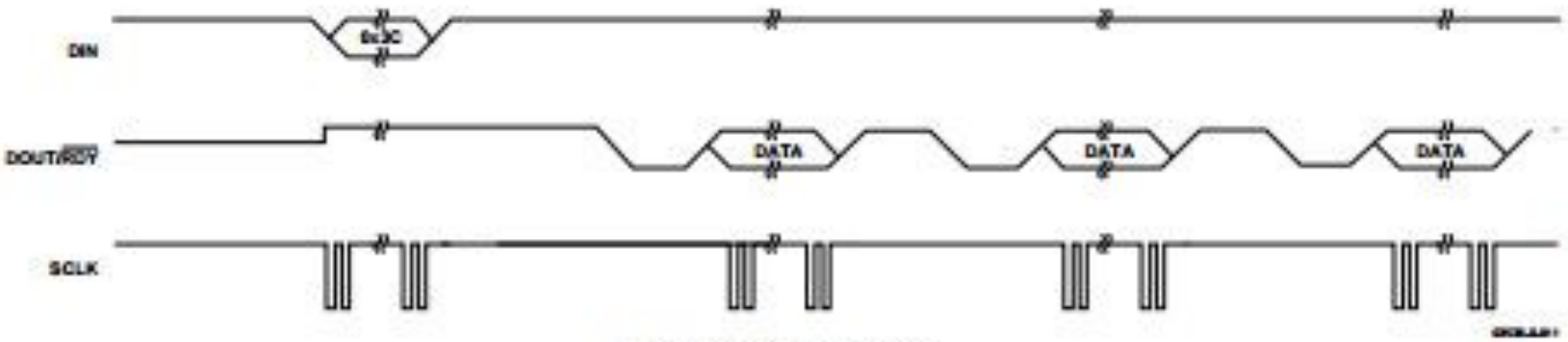


Figure 10. Continuous Read

ПРИМЕР МИКРОСХЕМЫ АЦП БЕЗ ВНУТРЕННИХ РЕГИСТРОВ – AD7171

ANALOG DEVICES

16-Bit, Low Power, Sigma-Delta ADC

Data Sheet **AD7171**

FEATURES

- Output data rate: 125 Hz
- Pin-programmable power-down and reset
- Status function
- Internal clock oscillator
- Current: 135 µA
- Power supply: 2.7 V to 5.25 V
- −40°C to +105°C temperature range
- Package: 10-lead 3 mm × 3 mm LFCSP

INTERFACE

- 2-wire serial (read-only device)
- SPI compatible
- Schmitt trigger on SCLK

APPLICATIONS

- Weigh scales
- Pressure measurement
- Industrial process control
- Portable instrumentation

FUNCTIONAL BLOCK DIAGRAM

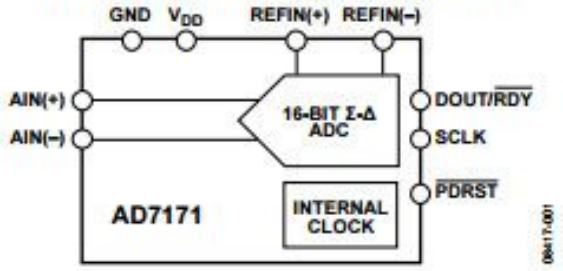


Figure 1.

Table 1.

$V_{REF} = V_{DD}$	RMS Noise	P-P Noise	P-P Resolution	ENOB
5 V	11.5 µV	76 µV	16 bits	16 bits
3 V	6.9 µV	45 µV	16 bits	16 bits

НЕБУФЕРИРОВАННЫЙ ВХОД МИКРОСХЕМЫ АЦП AD7171

ANALOG INPUT CHANNEL

The AD7171 has one differential analog input channel that is connected to the modulator; that is, the input is unbuffered. Note that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause dc gain errors, depending on the output impedance of the source that is driving the ADC input. Table 8 shows the allowable external resistance/capacitance values such that no gain error at the 16-bit level is introduced.

Table 8. External RC Combination for No Gain Error

C (pF)	R (Ω)
50	9000
100	6000
500	1500
1000	900
5000	200

The absolute input voltage range is restricted to a range between GND − 30 mV and V_{DD} + 30 mV. Care must be taken in setting up the common-mode voltage to avoid exceeding these limits. Otherwise, there is degradation in linearity and noise performance.

BIPOLAR CONFIGURATION

The AD7171 accepts a bipolar input range. A bipolar input range does not imply that the device can tolerate negative voltages with respect to system GND. Signals on the AIN(+) input are referenced to the voltage on the AIN(−) input. For example, if AIN(−) is 2.5 V, the analog input range on the AIN(+) input is 0 V to 5 V when a 2.5 V reference is used.

ФИЛЬТР $SINC^3$ МИКРОСХЕМЫ АЦП AD7171

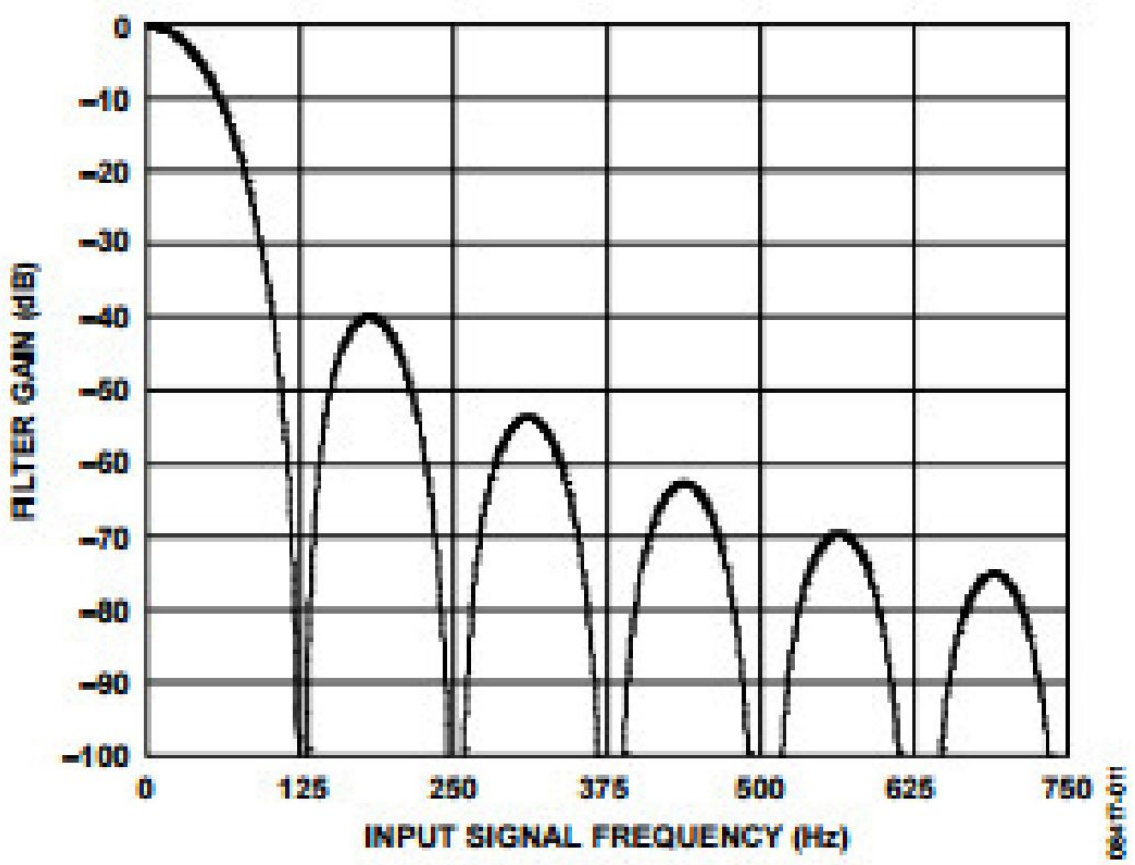


Figure 12. Filter Response

ПОДКЛЮЧЕНИЕ ТЕРМОРЕЗИСТОРА К МИКРОСХЕМЕ АЦП AD7171

TEMPERATURE SYSTEM

Figure 13 shows the AD7171 used in a temperature measurement system. The thermistor is connected in series with a precision resistor, R_{REF}, the precision resistor being used to generate the reference voltage. The value of R_{REF} is equal to the maximum resistance produced by the thermistor. The complete dynamic range of the ADC is then used, resulting in optimum performance. See Table 8 for suitable external RC combinations.

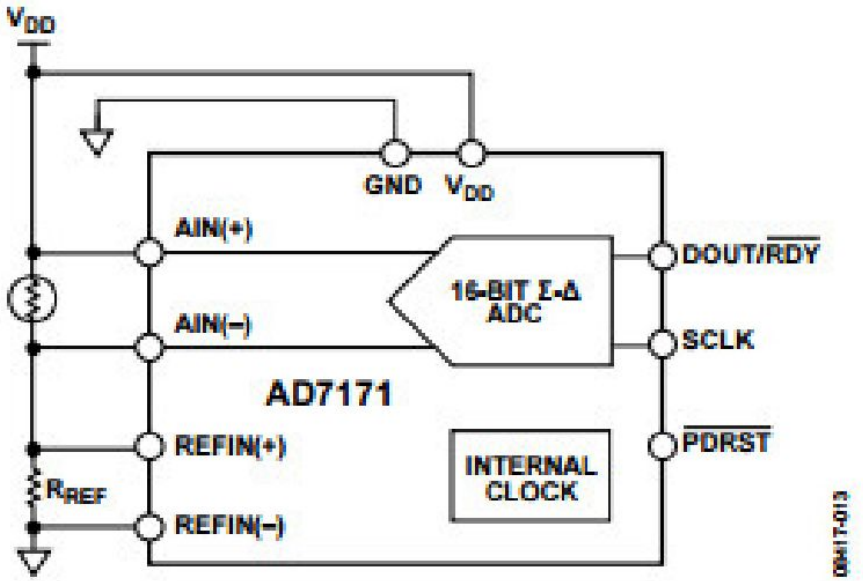


Figure 13. Temperature System Using the AD7171

ПРИМЕР МИКРОСХЕМЫ ΣΔ–АЦП С МУЛЬТИПЛЕКСОРОМ – AD7173-8

ANALOG DEVICES

Low Power, 8-/16-Channel, 31.25 kSPS, 24-Bit, Highly Integrated Sigma-Delta ADC

Data Sheet **AD7173-8**

FEATURES

- Low power, 8-/16-channel, highly integrated multiplexed analog-to-digital converter (ADC)
- Integration
  - Precision analog input buffers and reference input buffers
  - 2.5 V precision reference (3.5 ppm/°C)
  - Cross point multiplexer (enable system diagnostic)
  - 8 full differential or 16 single-ended channels
  - Clock oscillator
  - GPIO and GPO pins with automatic external mux control
- Fast and flexible output rate: 1.25 SPS to 31.25 kSPS
- Channel scan data rate: 6.21 kSPS/channel (161 µs settling)
- Performance specifications
  - 17.5 noise free bits at 31.25 kSPS
  - 24 noise free bits at 1.25 SPS
  - INL: ±3 ppm/FSR
- 85 dB rejection of 50 Hz and 60 Hz with 50 ms settling
- Operates with either 3.3 V or 5 V supply
  - Single supply
    - 3.3 V or 5 V AVDD1, 2 V to 5 V AVDD2, and 2 V to 5 V IOVDD
  - Optional split supply
    - AVDD1 and AVSS ± 2.5 V or AVDD1 and AVSS ± 1.65 V
  - Current: 1.4 mA
- 3-/4-wire serial digital interface (Schmitt trigger on SCLK)
  - CRC error checking
  - SPI, QSPI, MICROWIRE, and DSP compatible
- Package: 40-lead 6 mm × 6 mm LFCSP
- Temperature range: −40°C to +105°C

APPLICATIONS

- Process control: PLC/DCS modules
  - Voltage, current, temperature, and pressure measurement
  - Flow meters
- Medical and scientific multichannel instrumentation
- Seismic instrumentation
- Chemical analysis instrumentation: chromatography

GENERAL DESCRIPTION

Fast settling, highly accurate, low power, 8-/16-channel, multiplexed ADC for low bandwidth input signals with integrated input buffers.

Integrated precision, 2.5 V, low drift (3.5 ppm/°C), band gap reference and integrated oscillator.

Eight flexible setups with configurability for output data rate, digital filter mode, offset/gain error correction, reference selection, buffer enables and more. This per channel configurability extends to the output data rate used for each channel when using sinc5 + sinc1 filter.

Sinc5 + sinc1 filter maximizes channel scan rate, and sinc3 filter maximizes resolution and enhanced 50 Hz/60 Hz rejection, with four selectable options to maximize rejection.

Integrated diagnostic features, including CRC, register checksum, temperature sensor, crosspoint multiplexer, burnout currents, and GPIOs/GPOs.

СТРУКТУРА МИКРОСХЕМЫ AD7173-8

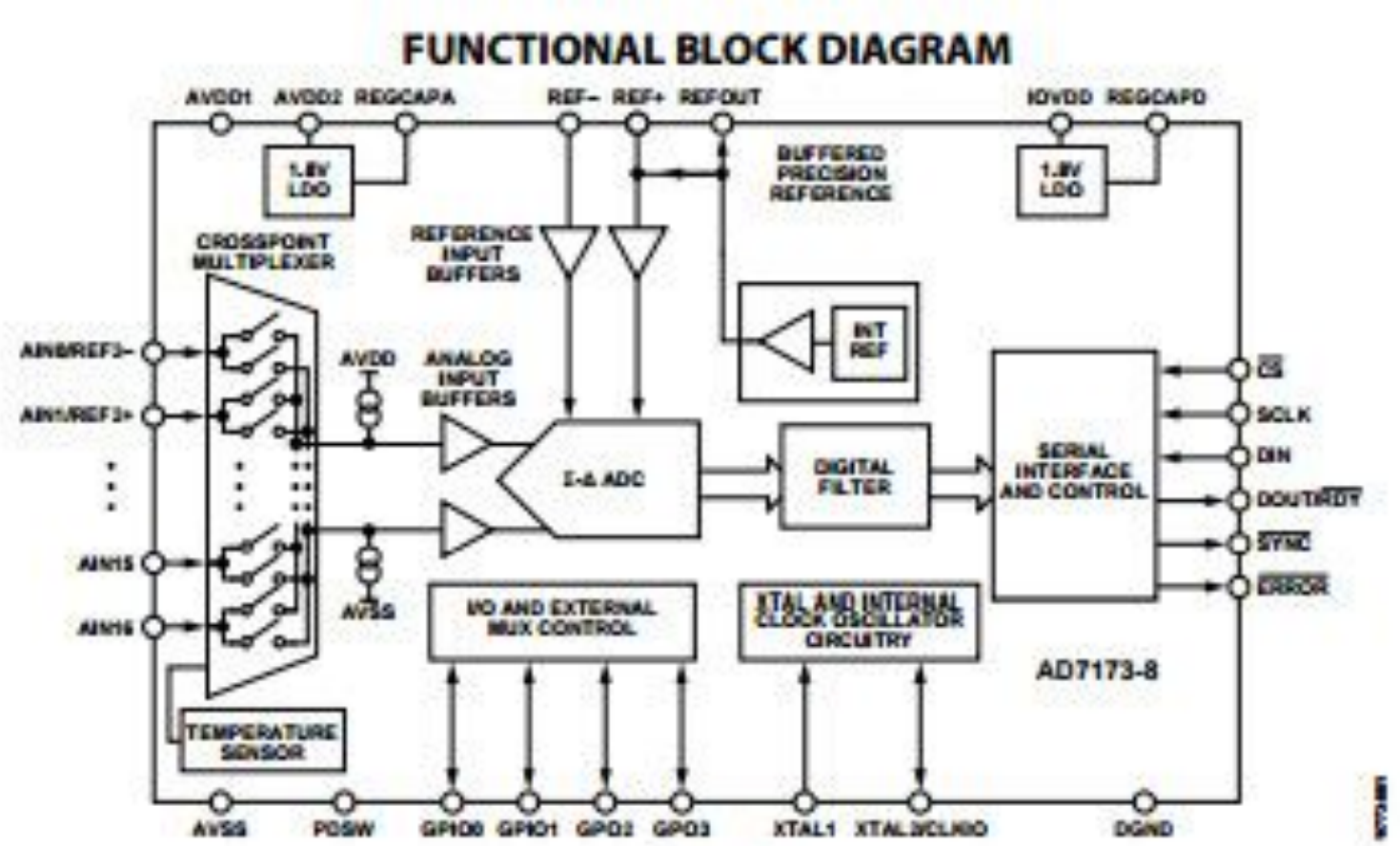


Figure 1.

СИСТЕМА ЦИФРОВЫХ ФИЛЬТРОВ МИКРОСХЕМЫ AD7173-8

DIGITAL FILTERS

The AD7173-8 provides the following three flexible filter options to allow optimization of settling time, noise, and rejection:

- Sinc5 + sinc1 filter
- Sinc3 filter
- Enhanced 50 Hz and 60 Hz rejection filters

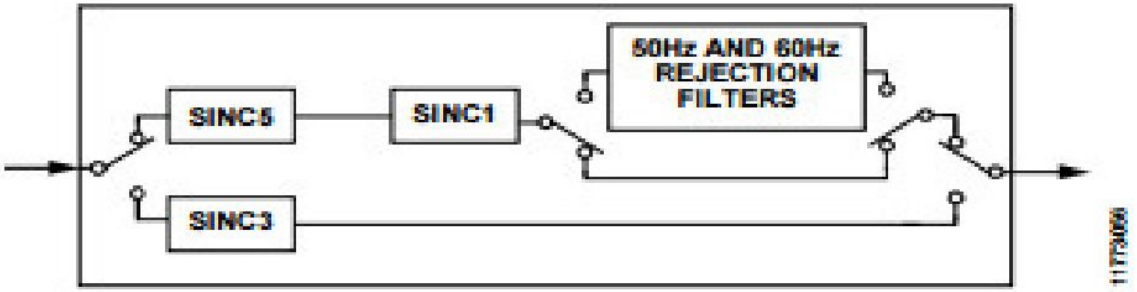


Figure 56. Digital Filter Block Diagram

The filter and output data rate are configured by setting the appropriate bits in the filter configuration register for the selected setup. When using the sinc5 + sinc1 filter, it is possible to select different output data rates per channel. When using the sinc3 filter, the user must select the sinc3 filter and use the same output data rate for all enabled channels. See the Register Details section for more information.

НА ВХОДЕ ΣΔ–АЦП МОГУТ БЫТЬ РЕЗИСТИВНЫЕ ДЕЛИТЕЛИ

ANALOG DEVICES

2-Channel, ±10 V Input Range, High Throughput, 24-Bit ∑-Δ ADC

AD7732

FEATURES

- High resolution ADC
  - 24 bits no missing codes
  - ±0.0015% nonlinearity
- Optimized for fast channel switching
  - 18-bit p-p resolution (21 bits effective) at 500 Hz
  - 16-bit p-p resolution (19 bits effective) at 2 kHz
  - 14-bit p-p resolution (18 bits effective) at 15 kHz
  - On-chip per channel system calibration
- 2 fully differential analog inputs
  - Input ranges +5 V, ±5 V, +10 V, ±10 V
  - Overvoltage tolerant
  - Up to ±16.5 V not affecting adjacent channel
  - Up to ±50 V absolute maximum
- 3-wire serial interface
  - SPI™, QSPI™, MICROWIRE™, and DSP compatible
  - Schmitt trigger on logic inputs
- Single-supply operation
  - 5 V analog supply
  - 3 V or 5 V digital supply
- Package: 28-lead TSSOP

FUNCTIONAL BLOCK DIAGRAM

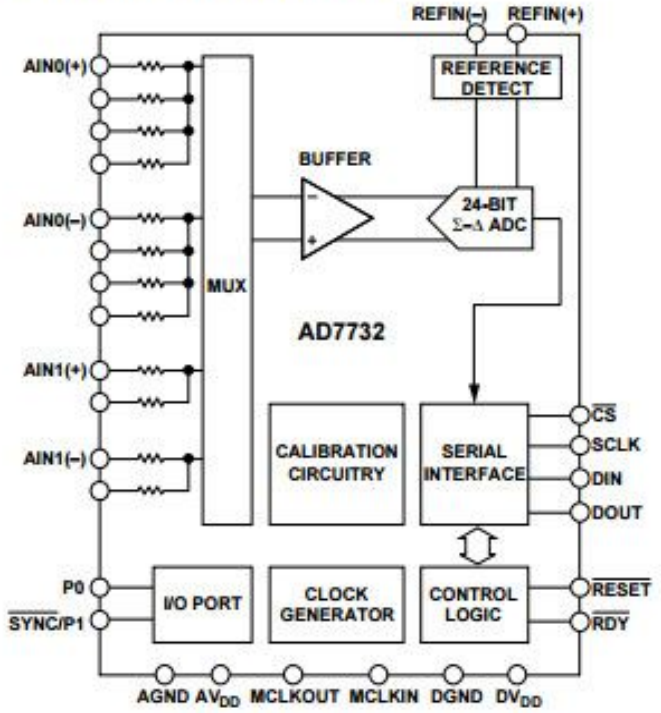


Figure 1.

СПЕЦИАЛИЗИРОВАННЫЕ МИКРОСХЕМЫ ΣΔ–АЦП

- «Слабая специализация»
  - Микросхемы АЦП для мостовых датчиков
  - Многоканальные АЦП для медицинской аппаратуры
- «Сильная специализация»
  - Микросхемы цифровых термометров
  - Преобразователи ёмкость→код
  - Микросхемы для электроэнергетики, в частности, для электросчётчиков

ПРИМЕР МИКРОСХЕМЫ АЦП ДЛЯ МОСТОВЫХ ДАТЧИКОВ – AD7730

ANALOG DEVICES

Bridge Transducer ADC

AD7730/AD7730L

KEY FEATURES
Resolution of 230,000 Counts (Peak-to-Peak)
Offset Drift: 5 nV/°C
Gain Drift: 2 ppm/°C
Line Frequency Rejection: >150 dB
Buffered Differential Inputs
Programmable Filter Cutoffs
Specified for Drift Over Time
Operates with Reference Voltages of 1 V to 5 V

ADDITIONAL FEATURES
Two-Channel Programmable Gain Front End
On-Chip DAC for Offset/TARE Removal
*FAST*Step™ Mode
AC or DC Excitation
Single Supply Operation

APPLICATIONS
Weigh Scales
Pressure Measurement

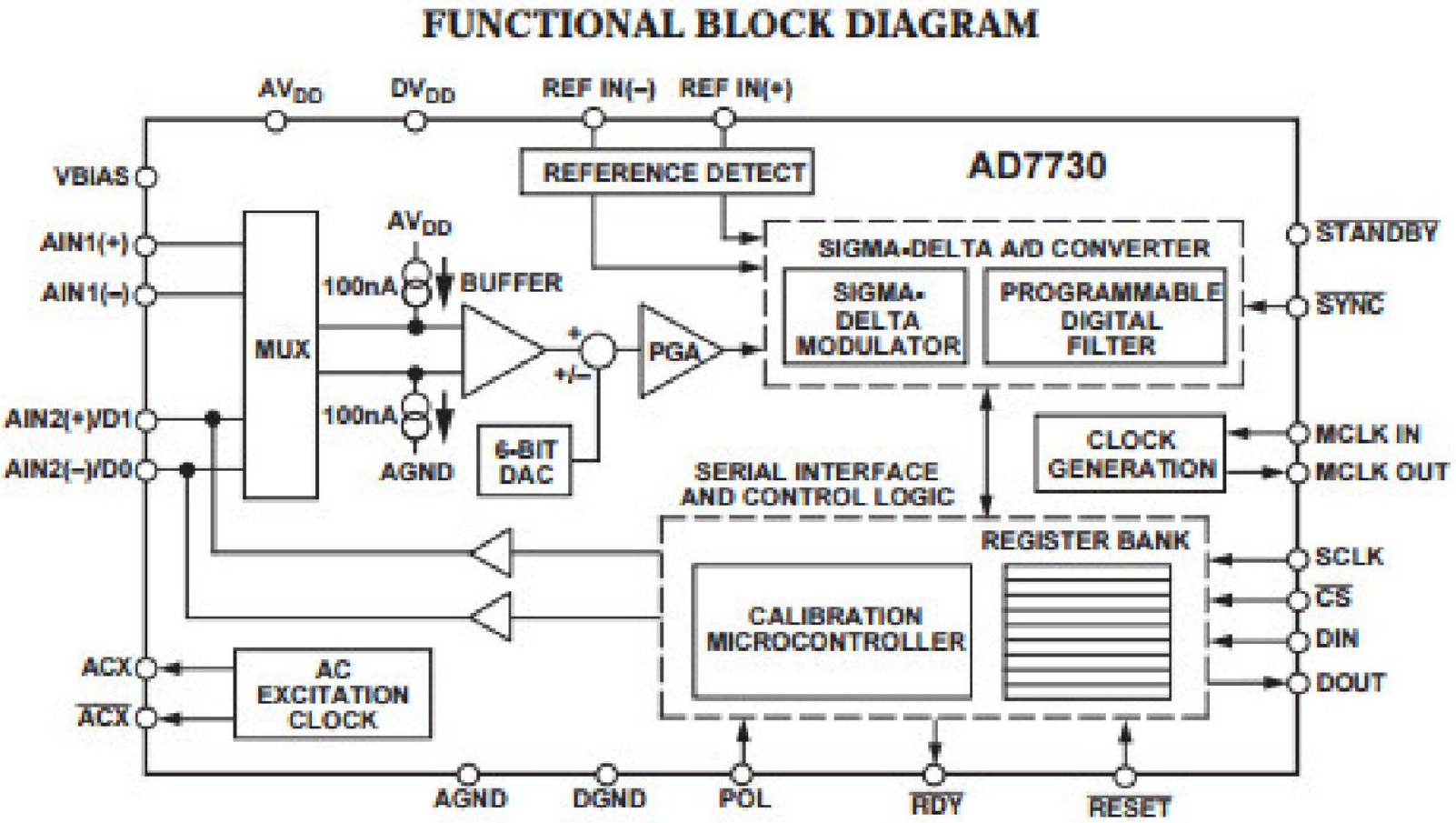
The modulator output is processed by a low pass programmable digital filter, allowing adjustment of filter cutoff, output rate and settling time.

The part features two buffered differential programmable gain analog inputs as well as a differential reference input. The part operates from a single +5 V supply. It accepts four unipolar analog input ranges: 0 mV to +10 mV, +20 mV, +40 mV and +80 mV and four bipolar ranges: ±10 mV, ±20 mV, ±40 mV and ±80 mV. The peak-to-peak resolution achievable directly from the part is 1 in 230,000 counts. An on-chip 6-bit DAC allows the removal of TARE voltages. Clock signals for synchronizing ac excitation of the bridge are also provided.

The serial interface on the part can be configured for three-wire operation and is compatible with microcontrollers and digital signal processors. The AD7730 contains self-calibration and system calibration options, and features an offset drift of less than 5 nV/°C and a gain drift of less than 2 ppm/°C.

The AD7730 is available in a 24-pin plastic DIP, a 24-lead SOIC and 24-lead TSSOP package. The AD7730L is available in a 24-lead SOIC and 24-lead TSSOP package.

СТРУКТУРА МИКРОСХЕМЫ AD7730



СОЕДИНЕНИЕ АЦП AD7730 С МОСТОВЫМ ДАТЧИКОМ

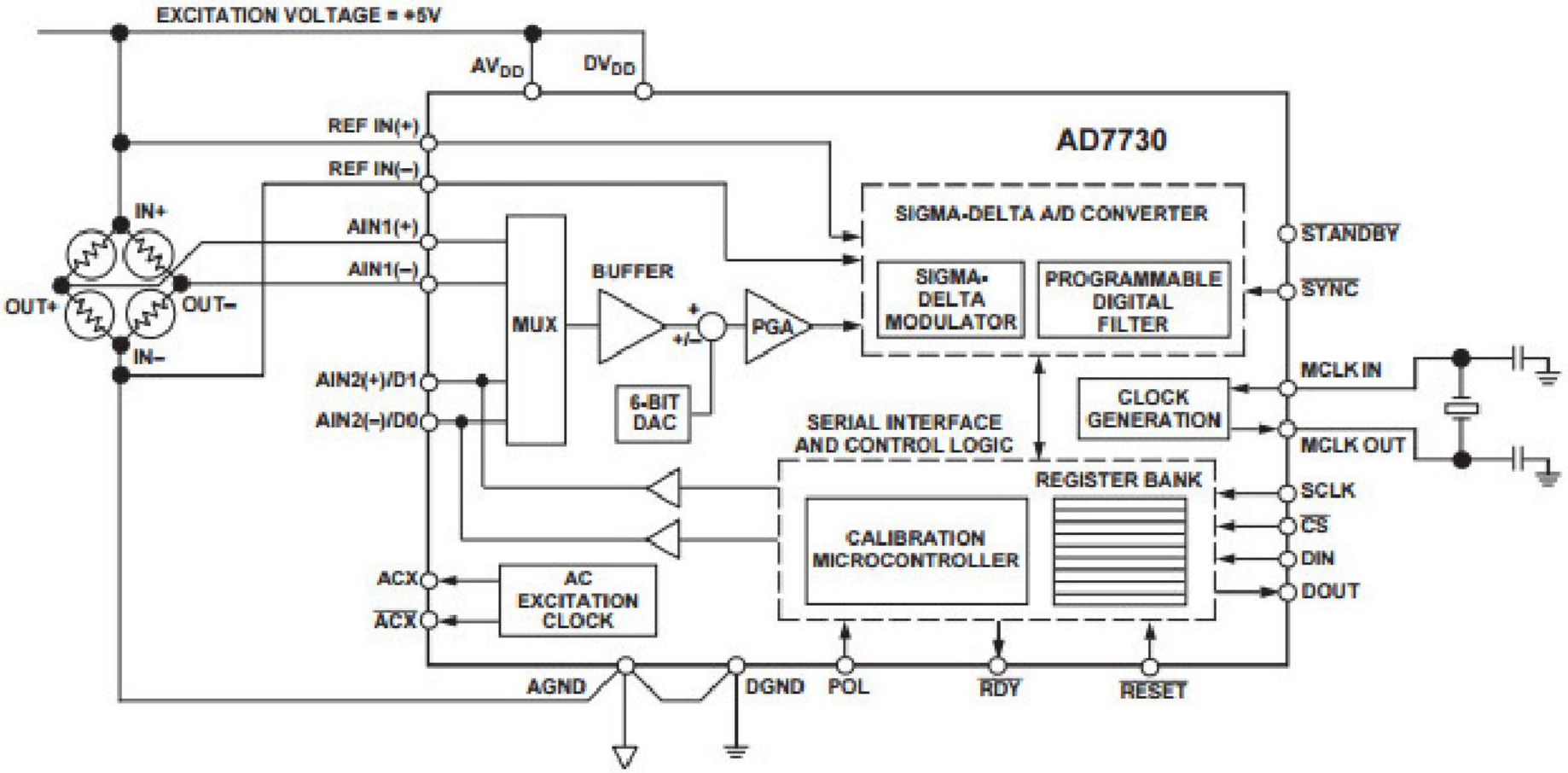


Figure 23. Typical Connections for DC-Excited Bridge Application

ПИТАНИЕ МОСТОВОГО ДАТЧИКА ПЕРЕМЕННЫМ НАПРЯЖЕНИЕМ ОТ АЦП AD7730

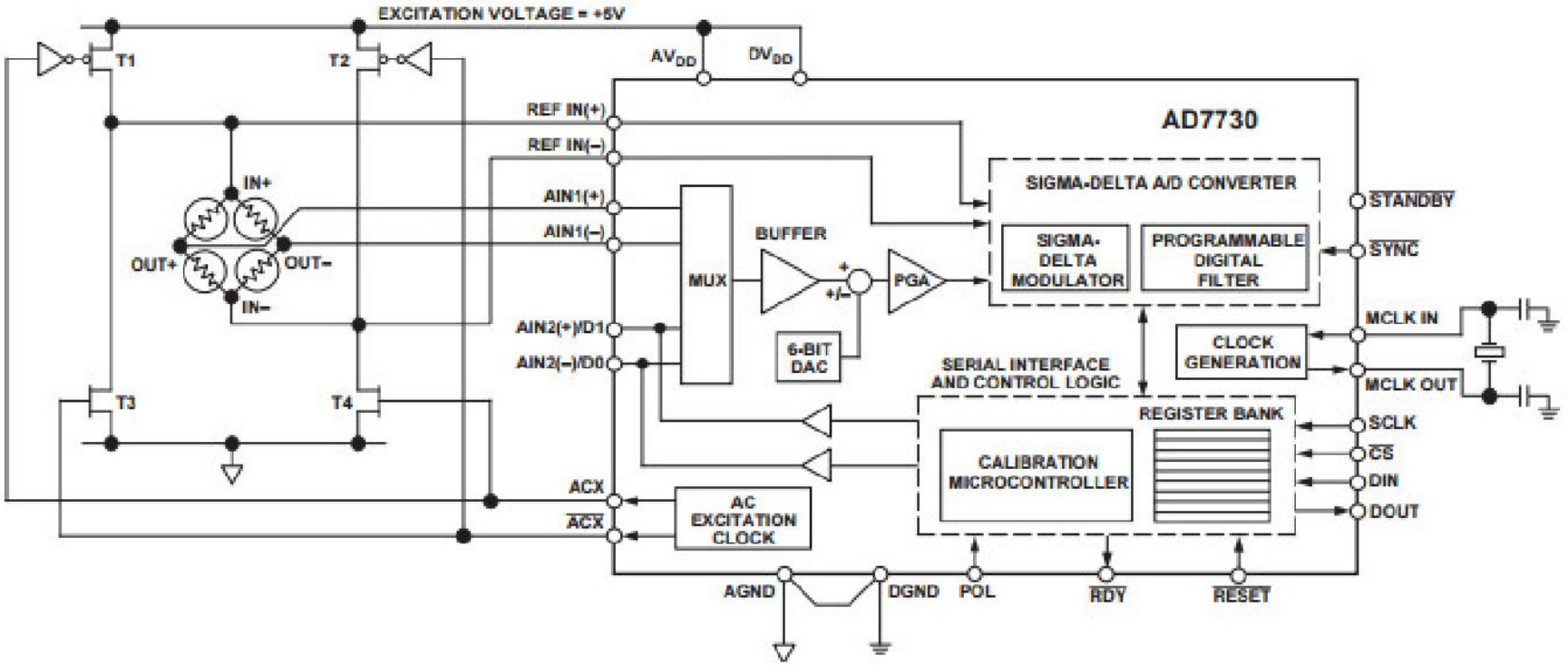


Figure 24. Typical Connections for AC-Excited Bridge Application

БОЛЕЕ НОВЫЕ МИКРОСХЕМЫ АЦП ДЛЯ МОСТОВЫХ ДАТЧИКОВ – AD7796/AD7797

ANALOG DEVICES

Low Power, 16-/24-Bit Sigma-Delta ADC for Bridge Sensors Low Power, 16-/24-Bit

Data Sheet **AD7796/AD7797**

FEATURES

- RMS noise: 65 nV
- Instrumentation amp
- Temperature sensor
- Internal clock oscillator
- Simultaneous 50 Hz/60 Hz rejection
- Update rate range: 4.17 Hz to 123 Hz
- Current: 250 µA typ
- Power-down: 1 µA
- Power supply range: 2.7 V to 5.25 V
- –40°C to +85°C temperature range
- Independent interface power supply
- 16-lead TSSOP

FUNCTIONAL BLOCK DIAGRAM

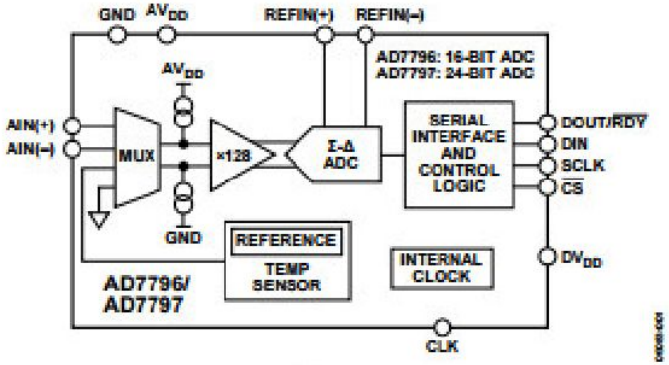


Figure 1.

ШУМОВЫЕ ХАРАКТЕРИСТИКИ МИКРОСХЕМ АЦП AD7796/AD7797

RMS NOISE AND RESOLUTION SPECIFICATIONS

Table 6 shows the rms noise of the AD7796/AD7797 for some of the update rates. The numbers given are for the bipolar input range with an external 2.5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 7 and Table 8 show the effective resolution, while the output peak-to-peak (p-p) resolution is shown in parentheses. It is important to note that the effective resolution is calculated using the rms noise, while the p-p resolution is based on the p-p noise. The p-p resolution represents the resolution for which there is no code flicker. These numbers are typical and are rounded to the nearest 0.5 LSB.

Table 6. RMS Noise (μV) vs. Output Update Rate for the AD7796/AD7797 Using a 2.5 V Reference

Update Rate (Hz)	RMS Noise (μV)
4.17	0.065
6.25	0.07
8.33	0.08
10	0.09
12.5	0.1
16.7	0.12
33.2	0.17
50	0.21
62	0.23
123	0.43

Table 7. Typical Resolution (Bits) vs. Output Update Rate for the AD7797 Using a 2.5 V Reference

Update Rate (Hz)	Effective Bits (p-p)
4.17	19 (16.5)
6.25	19 (16.5)
8.33	19 (16)
10	18.5 (16)
12.5	18.5 (16)
16.7	18.5 (15.5)
33.2	18 (15)
50	17.5 (15)
62	17.5 (14.5)
123	16.5 (13.5)

Table 8. Typical Resolution (Bits) vs. Output Update Rate for the AD7796 Using a 2.5 V Reference

Update Rate (Hz)	Effective Bits (p-p)
4.17	16 (16)
6.25	16 (16)
8.33	16 (16)
10	16 (16)
12.5	16 (16)
16.7	16 (15.5)
33.2	16 (15)
50	16 (15)
62	16 (14.5)
123	16 (13.5)

МИКРОСХЕМЫ АЦП AD7796/AD7797 В ЦИФРОВЫХ ТЕНЗОМЕТРИЧЕСКИХ ВЕСАХ

The AD7796/AD7797 offer a high resolution analog-to-digital function. Because the analog-to-digital function is provided by a Σ-Δ architecture, the devices are more immune to noisy environments, making them ideal for use in sensor measurement, and industrial and process-control applications.

WEIGH SCALES

Figure 17 shows the AD7796/AD7797 being used in a weigh scale application. The load cell is arranged in a bridge network and gives a differential output voltage between its OUT+ and OUT– terminals. Assuming a 5 V excitation voltage, the full-scale output range from the transducer is 10 mV when the sensitivity is 2 mV/V. The excitation voltage for the bridge can be used to directly provide the reference for the ADC because the reference input range includes the supply voltage. This allows a ratiometric measurement. Therefore, variations of the excitation voltage do not affect the measurement.

The on-chip temperature sensor can be used for temperature compensation of the bridge so the variation of the sensor resistance with temperature drift can be monitored and the conversions from the bridge can be compensated.

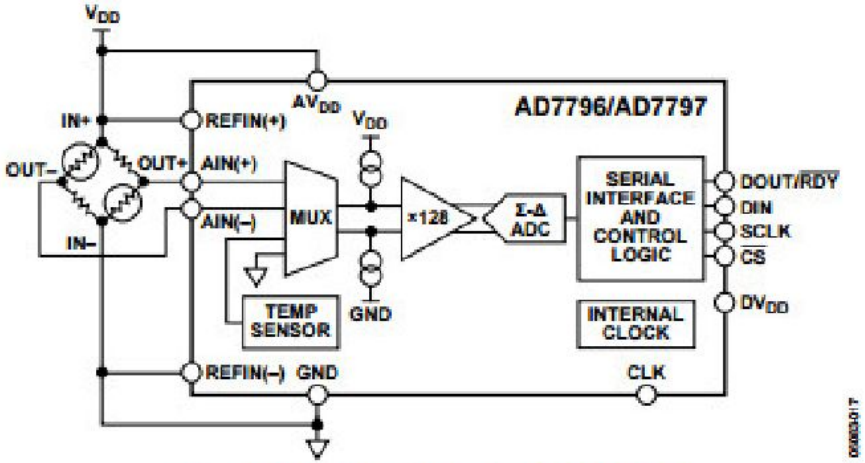


Figure 17. Weigh Scales Using the AD7796/AD7797

ТРЁХКАНАЛЬНЫЕ МИКРОСХЕМЫ АЦП ДЛЯ МОСТОВЫХ ДАТЧИКОВ

ANALOG DEVICES

3-Channel, Low Noise, Low Power, 16-/24-Bit, Σ-Δ ADC with On-Chip In-Amp

Data Sheet **AD7798/AD7799**

FEATURES

RMS noise:
- 27 nV at 4.17 Hz (AD7799)
- 65 nV at 16.7 Hz (AD7799)
- 40 nV at 4.17 Hz (AD7798)
- 85 nV at 16.7 Hz (AD7798)

Current: 380 µA typical
Power-down: 1 µA maximum
Low noise, programmable gain, instrumentation amp
Update rate: 4.17 Hz to 470 Hz
3 differential inputs
Internal clock oscillator
Simultaneous 50 Hz/60 Hz rejection
Reference detect
Low-side power switch
Programmable digital outputs
Burnout currents
Power supply: 2.7 V to 5.25 V
−40°C to +105°C temperature range
Independent interface power supply
16-lead TSSOP package

INTERFACE

3-wire serial
SPI®, QSPI™, MICROWIRE™, and DSP compatible
Schmitt trigger on SCLK

APPLICATIONS

Weigh scales
Pressure measurement
Strain gauge transducers
Gas analysis
Industrial process control
Instrumentation
Portable instrumentation
Blood analysis
Smart transmitters
Liquid/gas chromotography
6-digit DVM

FUNCTIONAL BLOCK DIAGRAM

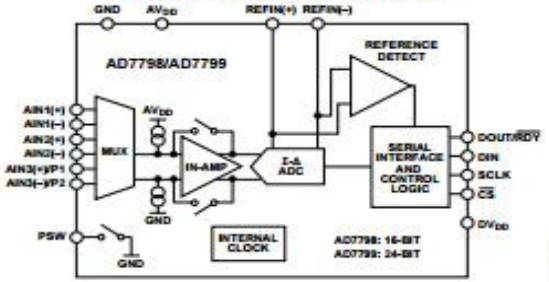


Figure 1.

GENERAL DESCRIPTION

The AD7798/AD7799 are low power, low noise, complete analog front ends for high precision measurement applications. The AD7798/AD7799 contains a low noise, 16-/24-bit Σ-Δ ADC with three differential analog inputs. The on-chip, low noise instrumentation amplifier means that signals of small amplitude can be interfaced directly to the ADC. With a gain setting of 64, the rms noise is 27 nV for the AD7799 and 40 nV for the AD7798 when the update rate equals 4.17 Hz.

On-chip features include a low-side power switch, reference detect, programmable digital output pins, burnout currents, and an internal clock oscillator. The output data rate from the part is software-programmable and can be varied from 4.17 Hz to 470 Hz.

The part operates with a power supply from 2.7 V to 5.25 V. The AD7798 consumes a current of 300 µA typical, whereas the AD7799 consumes 380 µA typical. Both devices are housed in a 16-lead TSSOP package.

ШУМОВЫЕ ХАРАКТЕРИСТИКИ АЦП AD7798

OUTPUT NOISE AND RESOLUTION SPECIFICATIONS

AD7798

Table 5 shows the AD7798 output rms noise for some update rates and gain settings. The numbers given are for the bipolar input range with a 2.5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 6 shows the effective resolution, and the output peak-to-peak resolution is shown in parentheses. It is important to note that the effective resolution is calculated using the rms noise, whereas the peak-to-peak resolution is based on the peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker. These numbers are typical and are rounded to the nearest LSB.

Table 5. Output RMS Noise (μV) vs. Gain and Output Update Rate for the AD7798 Using a 2.5 V Reference

Update Rate	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17 Hz	0.64	0.6	0.29	0.22	0.1	0.065	0.039	0.041
8.33 Hz	1.04	0.96	0.38	0.26	0.13	0.078	0.057	0.055
16.7 Hz	1.55	1.45	0.54	0.36	0.18	0.11	0.087	0.086
33.2 Hz	2.3	2.13	0.74	0.5	0.23	0.17	0.124	0.118
62 Hz	2.95	2.85	0.92	0.58	0.29	0.2	0.153	0.144
123 Hz	4.89	4.74	1.49	1	0.48	0.32	0.265	0.283
242 Hz	11.76	9.5	4.02	1.96	0.88	0.45	0.379	0.397
470 Hz	11.33	9.44	3.07	1.79	0.99	0.63	0.568	0.593

Table 6. Typical Resolution (Bits) vs. Gain and Output Update Rate for the AD7798 Using a 2.5 V Reference

Update Rate	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17 Hz	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
8.33 Hz	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
16.7 Hz	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
33.2 Hz	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
62 Hz	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)
123 Hz	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)	16 (14.5)
242 Hz	16 (16)	16 (15.5)	16 (15.5)	16 (15.5)	16 (16)	16 (16)	16 (15)	16 (14)
470 Hz	16 (16)	16 (15.5)	16 (16)	16 (16)	16 (15.5)	16 (15.5)	16 (14.5)	15.5 (13.5)

ШУМОВЫЕ ХАРАКТЕРИСТИКИ АЦП AD7799

AD7799

Table 7 shows the AD7799 output rms noise for some update rates and gain settings. The numbers given are for the bipolar input range with a 2.5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 8 shows the effective resolution, and the output peak-to-peak resolution is given in parentheses. Note that the effective resolution is calculated using the rms noise, whereas the peak-to-peak resolution is based on peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker. These numbers are typical and are rounded to the nearest LSB.

Table 7. Output RMS Noise (μV) vs. Gain and Output Update Rate for the AD7799 Using a 2.5 V Reference

Update Rate	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17 Hz	0.64	0.6	0.185	0.097	0.075	0.035	0.027	0.027
8.33 Hz	1.04	0.96	0.269	0.165	0.108	0.048	0.037	0.040
16.7 Hz	1.55	1.45	0.433	0.258	0.176	0.085	0.065	0.065
33.2 Hz	2.3	2.13	0.647	0.364	0.24	0.118	0.097	0.094
62 Hz	2.95	2.85	0.952	0.586	0.361	0.178	0.133	0.134
123 Hz	4.89	4.74	1.356	0.785	0.521	0.265	0.192	0.192
242 Hz	11.76	9.5	3.797	2.054	1.027	0.476	0.326	0.308
470 Hz	11.33	9.44	3.132	1.773	1.107	0.5	0.413	0.374

Table 8. Typical Resolution (Bits) vs. Gain and Output Update Rate for the AD7799 Using a 2.5 V Reference

Update Rate	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17 Hz	23 (20.5)	22 (19.5)	22.5 (20)	22.5 (20)	22 (19.5)	22 (19.5)	21.5 (19)	20.5 (18)
8.33 Hz	22 (19.5)	21.5 (19)	22 (19.5)	22 (19.5)	21.5 (19)	21.5 (19)	21 (18.5)	20 (17.5)
16.7 Hz	21.5 (19)	20.5 (18)	21.5 (19)	21 (18.5)	21 (18.5)	21 (18.5)	20 (17.5)	19 (16.5)
33.3 Hz	21 (18.5)	20 (17.5)	21 (18.5)	20.5 (18)	20.5 (18)	20.5 (18)	19.5 (17)	18.5 (16)
62 Hz	20.5 (18)	19.5 (17)	20.5 (18)	20 (17.5)	19.5 (17)	19.5 (17)	19 (16.5)	18 (15.5)
123 Hz	20 (17.5)	19 (16.5)	20 (17.5)	19.5 (17)	19 (16.5)	19 (16.5)	18.5 (16)	17.5 (15)
242 Hz	18.5 (16)	18 (15.5)	18.5 (16)	18 (15.5)	18 (15.5)	18.5 (16)	18 (15.5)	17 (14.5)
470 Hz	18.5 (16)	18 (15.5)	18.5 (16)	18.5 (16)	18 (15.5)	18.5 (16)	17.5 (15)	16.5 (14)

МИКРОСХЕМЫ АЦП AD7798/AD7799 В ЦИФРОВЫХ ТЕНЗОМЕТРИЧЕСКИХ ВЕСАХ

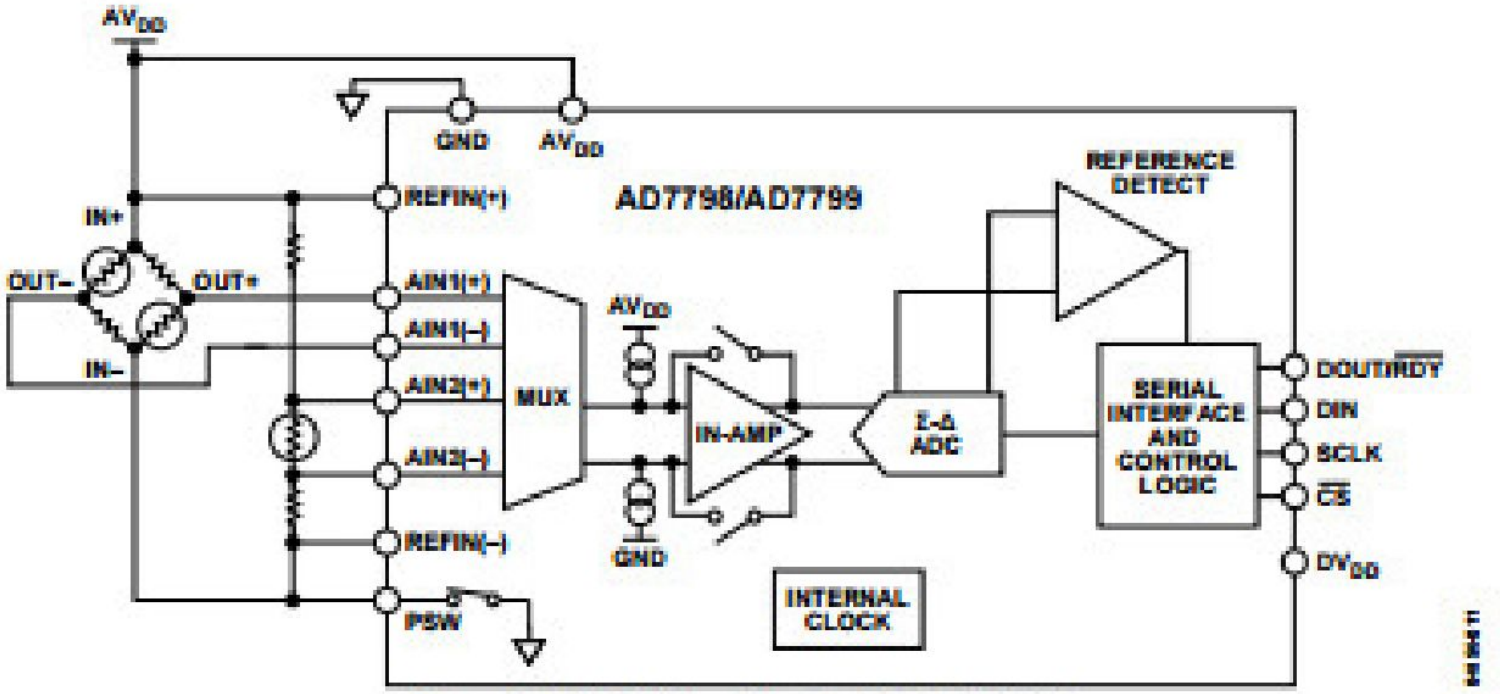


Figure 19. Weigh Scales Using the AD7798/AD7799

Обратим внимание на ключ (левый нижний вывод микросхемы)!

ПРИМЕР МНОГОКАНАЛЬНОГО АЦП ДЛЯ КАРДИОГРАФОВ И ЭНЦЕФАЛОГРАФОВ – AD7716

ANALOG DEVICES

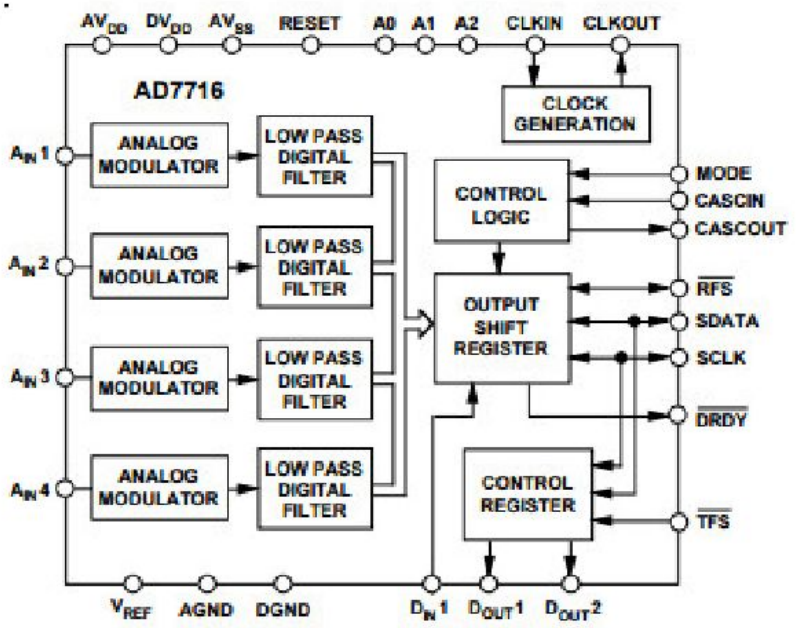
LC²MOS
22-Bit Data Acquisition System

AD7716

FEATURES
- 22-Bit Sigma-Delta ADC
  - Dynamic Range of 105 dB (146 Hz Input)
  - ±0.003% Integral Nonlinearity
- On-Chip Low-Pass Digital Filter
  - Cutoff Programmable from 584 Hz to 36.5 Hz
  - Linear Phase Response
- Five Line Serial I/O
- Twos Complement Coding
- Easy Interface to DSPs and Microcomputers
- Software Control of Filter Cutoff
- ±5 V Supply
- Low Power Operation: 50 mW

APPLICATIONS
- Biomedical Data Acquisition
  - ECG Machines
  - EEG Machines
- Process Control
- High Accuracy Instrumentation
- Seismic Systems

FUNCTIONAL BLOCK DIAGRAM



КАСКАДНОЕ СОЕДИНЕНИЕ МИКРОСХЕМ АЦП AD7716

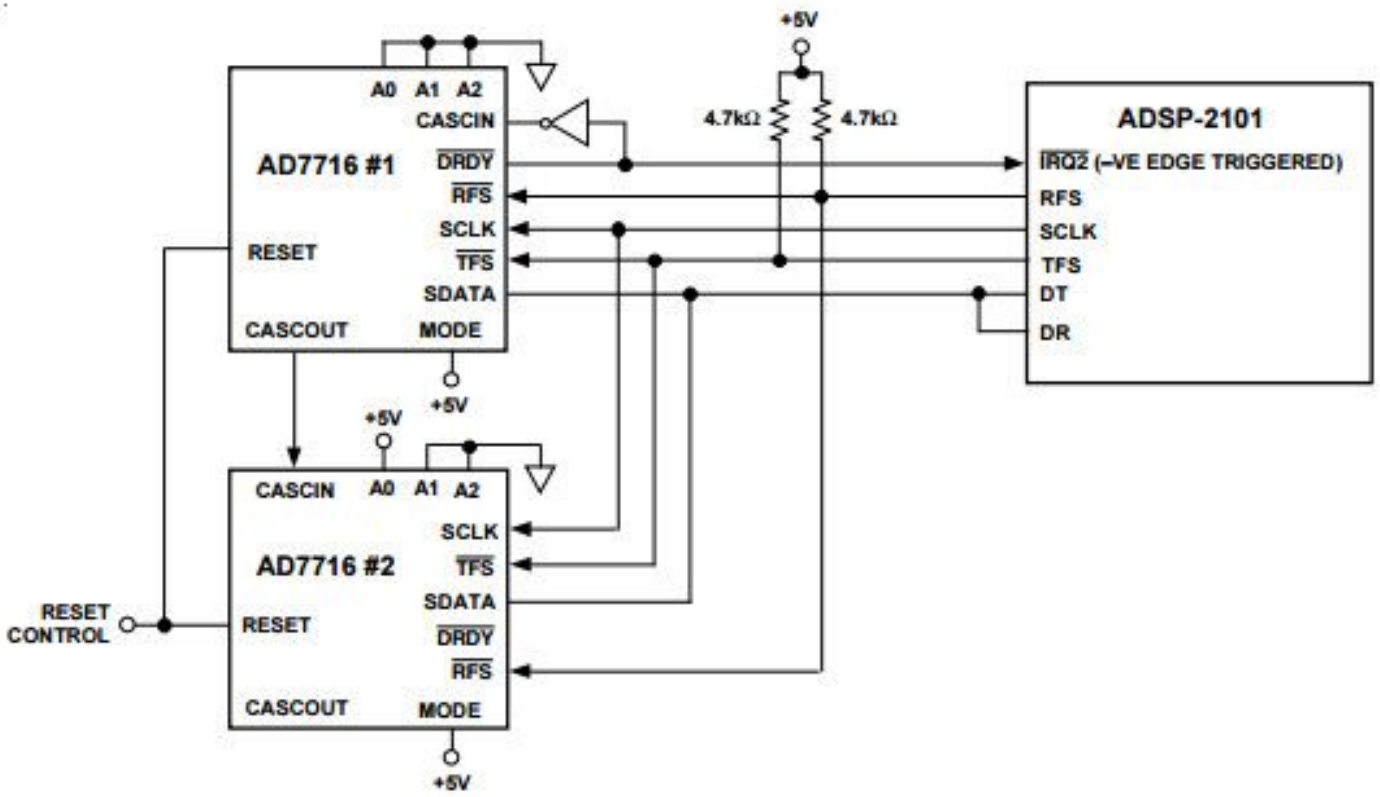


Figure 8. 8-Channel Data Acquisition System Using the ADSP-2101 Digital Signal Processor

АЦП AD7716 В РЕЖИМЕ ВЕДУЩЕГО (MASTER)

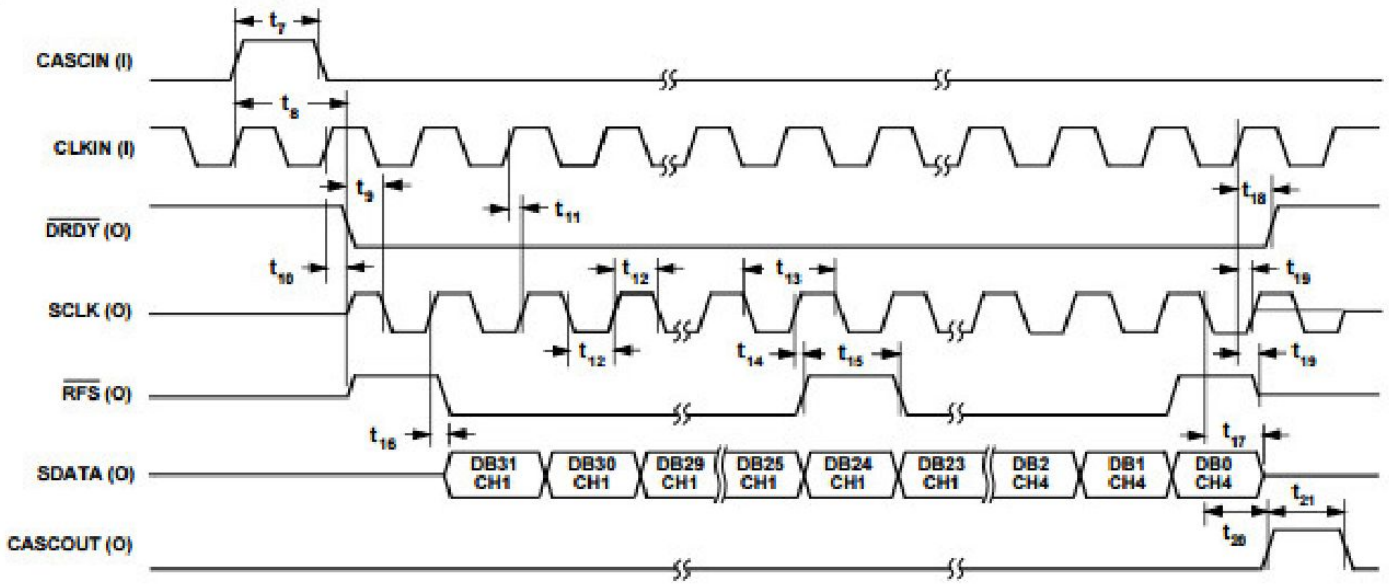


Figure 3. Master Mode Timing Diagram

АЦП AD7716 В РЕЖИМЕ ВЕДОМОГО (SLAVE)

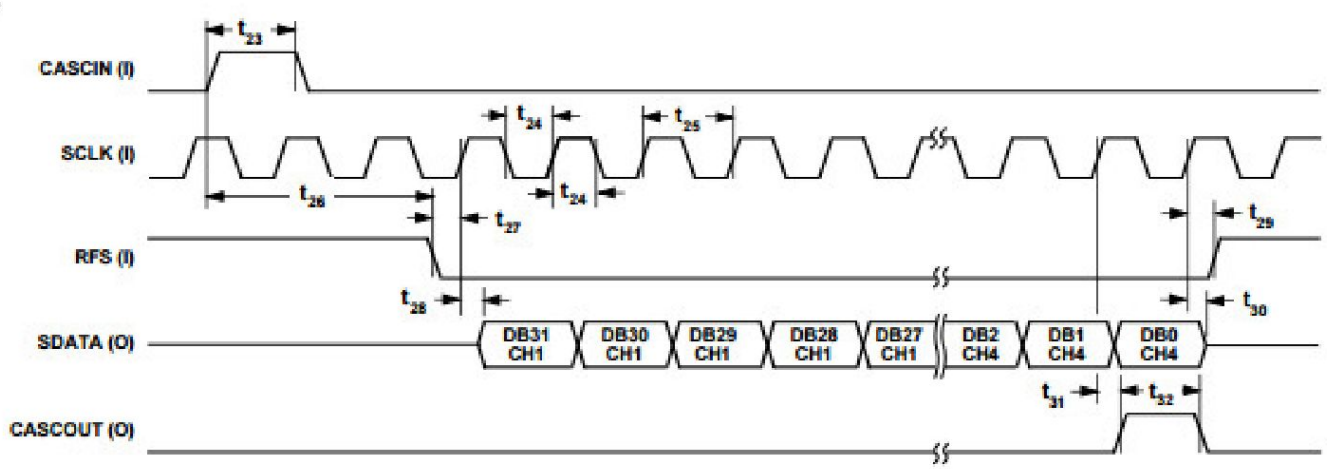


Figure 4. Slave Mode Timing Diagram

ПРИМЕР МИКРОСХЕМЫ АЦП ДЛЯ ЦИФРОВОГО ТЕРМОМЕТРА – ADT7410

ANALOG DEVICES

±0.5°C Accurate, 16-Bit Digital I²C Temperature Sensor

Data Sheet **ADT7410**

FEATURES

- High performance
  - Temperature accuracy
    - ±0.5°C from −40°C to +105°C (2.7 V to 3.6 V)
    - ±0.4°C from −40°C to +105°C (3.0 V)
  - 16-bit temperature resolution: 0.0078°C
  - Fast first temperature conversion on power-up of 6 ms
- Easy implementation
  - No temperature calibration/correction required by user
  - No linearity correction required
- Low power
  - Power saving 1 sample per second (SPS) mode
  - 700 µW typical at 3.3 V in normal mode
  - 7 µW typical at 3.3 V in shutdown mode
- Wide operating ranges
  - Temperature range: −55°C to +150°C
  - Voltage range: 2.7 V to 5.5 V
- Programmable interrupts
  - Critical overtemperature interrupt
  - Overtemperature/undertemperature interrupt
- I²C-compatible interface
- 8-lead narrow SOIC RoHS-compliant package

APPLICATIONS

- Medical equipment
- Environmental control systems
- Computer thermal monitoring
- Thermal protection
- Industrial process control
- Power system monitors
- Hand-held applications

GENERAL DESCRIPTION

The ADT7410 is a high accuracy digital temperature sensor in a narrow SOIC package. It contains a band gap temperature reference and a 13-bit ADC to monitor and digitize the temperature to a 0.0625°C resolution. The ADC resolution, by default, is set to 13 bits (0.0625°C). This can be changed to 16 bits (0.0078°C) by setting Bit 7 in the configuration register (Register Address 0x03).

The ADT7410 is guaranteed to operate over supply voltages from 2.7 V to 5.5 V. Operating at 3.3 V, the average supply current is typically 210 µA. The ADT7410 has a shutdown mode that powers down the device and offers a shutdown current of typically 2 µA. The ADT7410 is rated for operation over the −55°C to +150°C temperature range.

Pin A0 and Pin A1 are available for address selection, giving the ADT7410 four possible I²C addresses. The CT pin is an open-drain output that becomes active when the temperature exceeds a programmable critical temperature limit. The default critical temperature limit is 147°C. The INT pin is also an open-drain output that becomes active when the temperature exceeds a programmable limit. The INT and CT pins can operate in either comparator or interrupt mode.

СТРУКТУРА МИКРОСХЕМЫ ADT7410

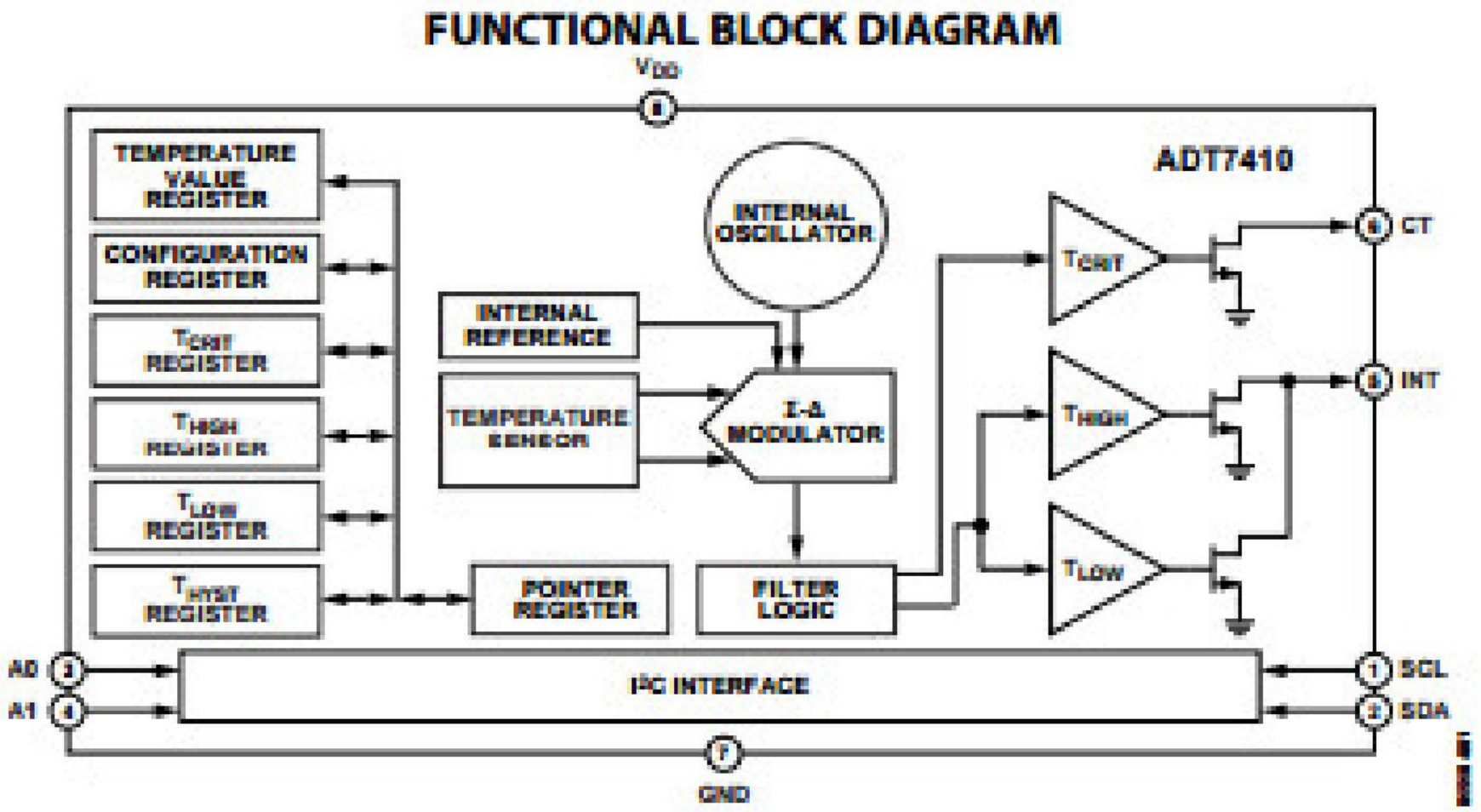


Figure 1.

ПРИМЕР ПРЕОБРАЗОВАТЕЛЯ ЁМКОСТЬ→КОД – AD7150

ANALOG DEVICES

Ultra-Low Power, 2-Channel, Capacitance Converter for Proximity Sensing

AD7150

FEATURES

- Ultra-low power
  - 2.7 V to 3.6 V, 100 µA
- Response time: 10 ms
- Adaptive environmental compensation
- 2 independent capacitance input channels
  - Sensor capacitance (C_{SENS}) 0 pF up to 13 pF
  - Sensitivity to 1 fF
- EMC tested
- 2 modes of operation
  - Standalone with fixed settings
  - Interfaced to a microcontroller for user-defined settings
- 2 proximity detection output flags
- 2-wire serial interface (I^2C compatible)
- Operating temperature
  - −40°C to +85°C
- 10-lead MSOP package

APPLICATIONS

- Proximity sensing
- Contactless switching
- Position detection
- Level detection

GENERAL DESCRIPTION

The AD7150 delivers a complete signal processing solution for capacitive proximity sensors, featuring an ultra-low power converter with fast response time. The AD7151 is a single-channel, lower power alternative to the AD7150.

The AD7150 uses Analog Devices, Inc., capacitance-to-digital converter (CDC) technology, which combines features important for interfacing to real sensors, such as high input sensitivity and high tolerance of both input parasitic ground capacitance and leakage current.

The integrated adaptive threshold algorithm compensates for any variations in the sensor capacitance due to environmental factors like humidity and temperature or due to changes in the dielectric material over time.

By default, the AD7150 operates in standalone mode using the fixed power-up settings and indicates detection on two digital outputs. Alternatively, the AD7150 can be interfaced to a microcontroller via the serial interface, the internal registers can be programmed with user-defined settings, and the data and status can be read from the part.

The AD7150 operates with a 2.7 V to 3.6 V power supply. It is specified over the temperature range of −40°C to +85°C.

СТРУКТУРА МИКРОСХЕМЫ AD7150

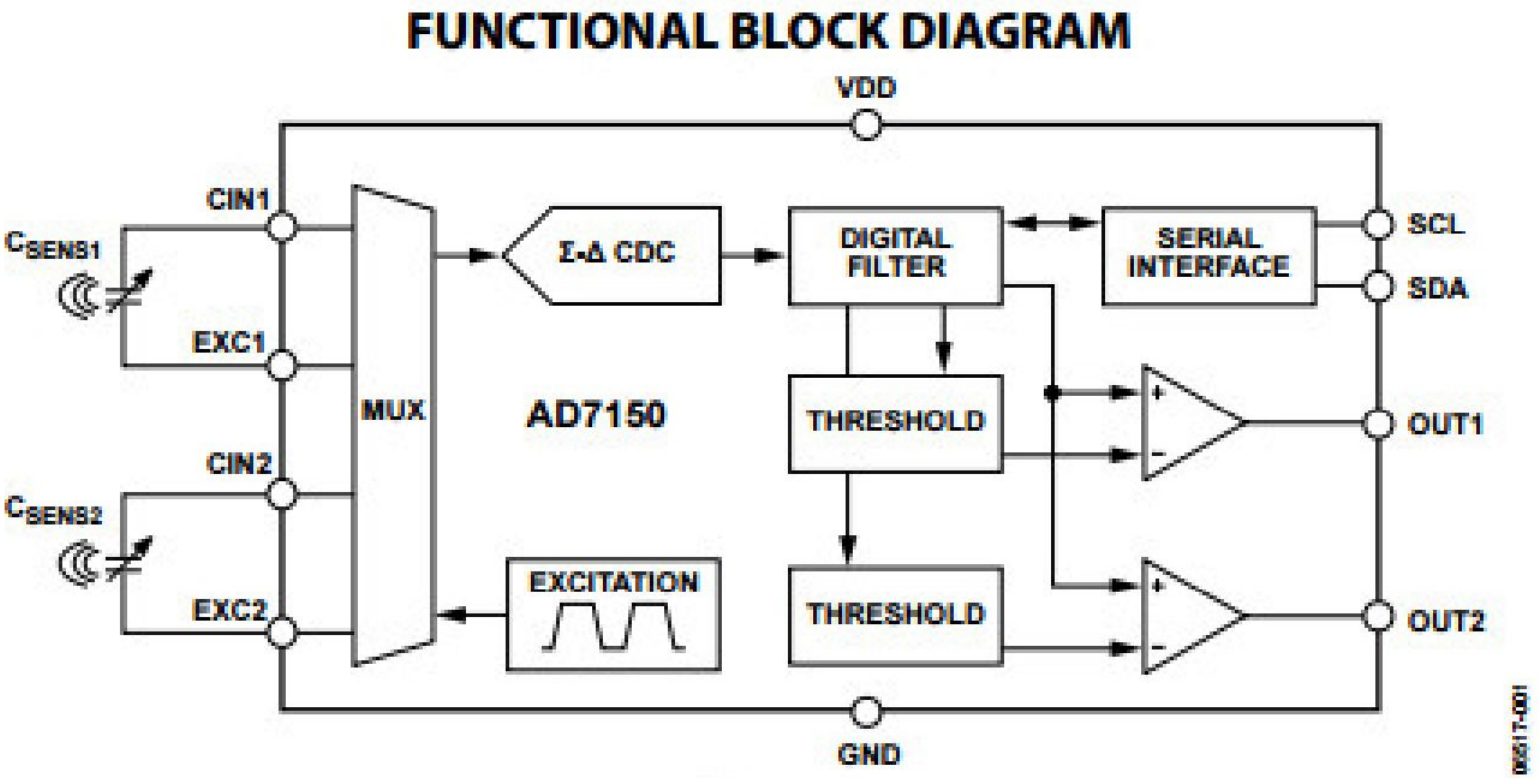


Figure 1.

ВАРИАНТЫ ВКЛЮЧЕНИЯ МИКРОСХЕМЫ AD7150

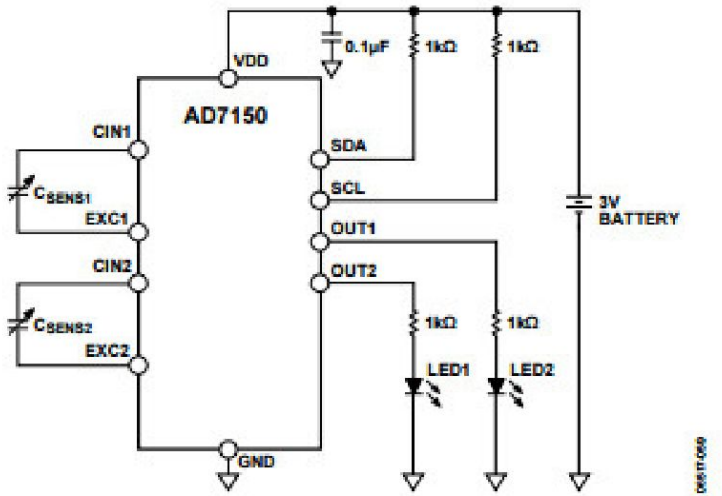


Figure 51. AD7150 Standalone Operation Application Diagram

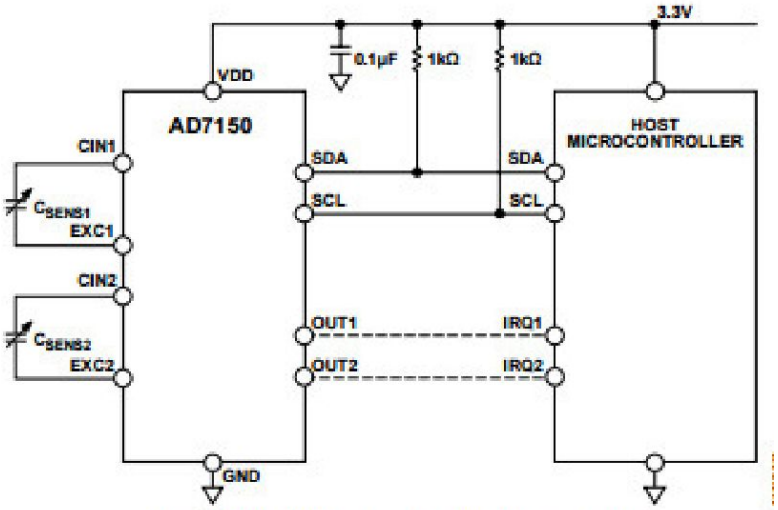


Figure 52. AD7150 Interfaced to a Host Microcontroller

ПРИМЕР МИКРОСХЕМЫ ДЛЯ ОДНОФАЗНОГО ЭЛЕКТРОСЧЁТЧИКА

ANALOG DEVICES

ИС счетчика электроэнергии с импульсным выходом

ADE7755*

ОСОБЕННОСТИ

- Высокая точность; счетчик поддерживает стандарт 50 Гц/60 Гц IEC 687/1036
- Ошибка менее 0,1% при динамическом диапазоне 500:1
- ИС ADE7755 выдает значение средней активной мощности на частотных выходах F1 и F2
- Высокочастотный выход CF предназначен для калибровки и выдает значение мгновенной активной мощности
- Совместимость по выводам с микросхемой AD7755 с синхронными выходами CF и F1/F2
- Логический выход REVP можно использовать для индикации возможного неправильного подключения к сети (отрицательной мощности)
- Прямое управление электромеханическими счетными механизмами и двухфазными шаговыми двигателями (выходы F1 и F2)
- Усилитель с программируемым коэффициентом усиления в канале измерения тока позволяет использовать шунт с малой величиной сопротивления
- Собственные встроенные АЦП и цифровой сигнальный процессор обеспечивают высокую точность в широком диапазоне условий и долговременную стабильность
- Встроенный контроль напряжения источника питания
- Встроенная защита от самохода счетчика (имеется порог мощности нагрузки, начиная с которого счетчик работает)
- Встроенный источник опорного напряжения 2,5 В±8% (типичный дрейф составляет 30·10⁻⁶/°C) с возможностью подключения внешнего источника опорного напряжения
- Один источник питания 5 В, низкая потребляемая мощность (типичное значение 15 мВт)
- Недорогая КМОП технология

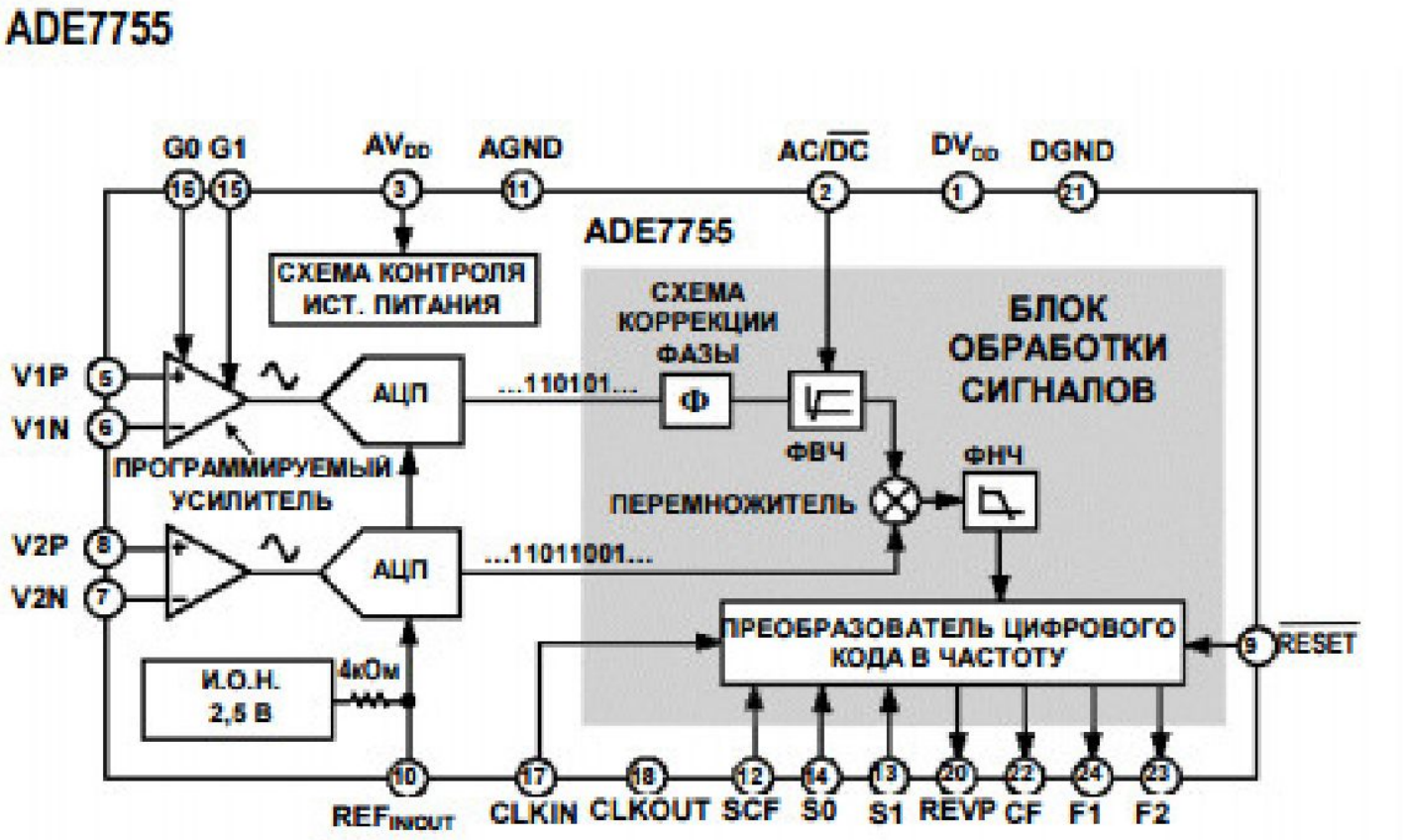
Микросхема ADE7755 – высокоточная ИС, предназначенная для счетчиков потребления электрической энергии. Технические характеристики этой ИС превосходят требования по точности, предъявляемые стандартом IEC1036. См. руководство по применению фирмы Analog Devices AN-559 с описанием конструкции счетчика электроэнергии стандарта IEC1036 на базе ИС AD7755.

Аналоговая часть микросхемы ADE7755 включает лишь АЦП и источник опорного напряжения. Все дальнейшие преобразования сигнала, такие как перемножение и фильтрация, происходят с сигналом в цифровом виде. Такой подход обеспечивает очень высокую стабильность и точность при предельных значениях параметров окружающей среды и в течение длительного времени.

Микросхема ADE7755 выдает информацию о средней активной мощности на низкочастотных выходах F1 и F2. Эти импульсные выходы могут быть использованы непосредственно для управления электромеханическим счетным механизмом или могут подключаться к микроконтроллеру. Импульсный выход CF дает информацию о мгновенной активной мощности. Этот выход предназначен для калибровки или для подключения к микроконтроллеру.

ИС ADE7755 включает в себя схему контроля напряжения питания на выводе AVDD. Микросхема ADE7755 остается в состоянии сброса до тех пор, пока напряжение источника питания не достигнет 4 В. Если напряжение источника питания падает ниже 4 В, ИС ADE7755 также переходит в состояние сброса, при этом импульсы на выходах F1, F2 и CF отсутствуют.

СТРУКТУРА МИКРОСХЕМЫ ДЛЯ ОДНОФАЗНОГО ЭЛЕКТРОСЧЁТЧИКА – ADE7755



ПРИМЕР МНОГОФУНКЦИОНАЛЬНОЙ ИЗМЕРИТЕЛЬНОЙ МИКРОСХЕМЫ ДЛЯ ЭЛЕКТРОЭНЕРГЕТИКИ – ADE7953

ANALOG DEVICES

Single Phase, Multifunction Metering IC with Neutral Current Measurement

Data Sheet **ADE7953**

FEATURES

- Highly accurate; supports EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-21, IEC 62053-22, and IEC 62053-23 standards
- Measures active, reactive, and apparent energy; sampled waveform; current and voltage rms
- Provides a second current input for neutral current measurement
- Less than 0.1% error in active and reactive energy measurements over a dynamic range of 3000:1
- Less than 0.2% error in instantaneous IRMS measurement over a dynamic range of 1000:1
- Provides apparent energy measurement and instantaneous power readings
- 1.23 kHz bandwidth operation
- Flexible PGA gain stage (up to ×22)
- Includes internal integrators for use with Rogowski coil sensors
- SPI, I^2C, or UART communication

GENERAL DESCRIPTION

The ADE7953 is a high accuracy electrical energy measurement IC intended for single phase applications. It measures line voltage and current and calculates active, reactive, and apparent energy, as well as instantaneous rms voltage and current.

The device incorporates three Σ-Δ ADCs with a high accuracy energy measurement core. The second input channel simultaneously measures neutral current and enables tamper detection and neutral current billing. The additional channel incorporates a complete signal path that allows a full range of measurements. Each input channel supports independent and flexible gain stages, making the device suitable for use with a variety of current sensors such as current transformers (CTs) and low value shunt resistors. Two on-chip integrators facilitate the use of Rogowski coil sensors.

The ADE7953 provides access to on-chip meter registers via a variety of communication interfaces including SPI, I^2C, and UART. Two configurable low jitter pulse output pins provide outputs that are proportional to active, reactive, or apparent energy, as well as current and voltage rms. A full range of power quality information such as overcurrent, overvoltage, peak, and sag detection are accessible via the external $\overline{\text{IRQ}}$ pin. Independent active, reactive, and apparent no-load detections are included to prevent "meter creep." Dedicated reverse power ($\overline{\text{REVP}}$), zero-crossing voltage (ZX), and zero-crossing current (ZX_I) pins are also provided. The ADE7953 energy metering IC operates from a 3.3 V supply voltage and is available in a 28-lead LFCSP package.

СТРУКТУРА МНОГОФУНКЦИОНАЛЬНОЙ ИЗМЕРИТЕЛЬНОЙ МИКРОСХЕМЫ ДЛЯ ЭЛЕКТРОЭНЕРГЕТИКИ – ADE7953

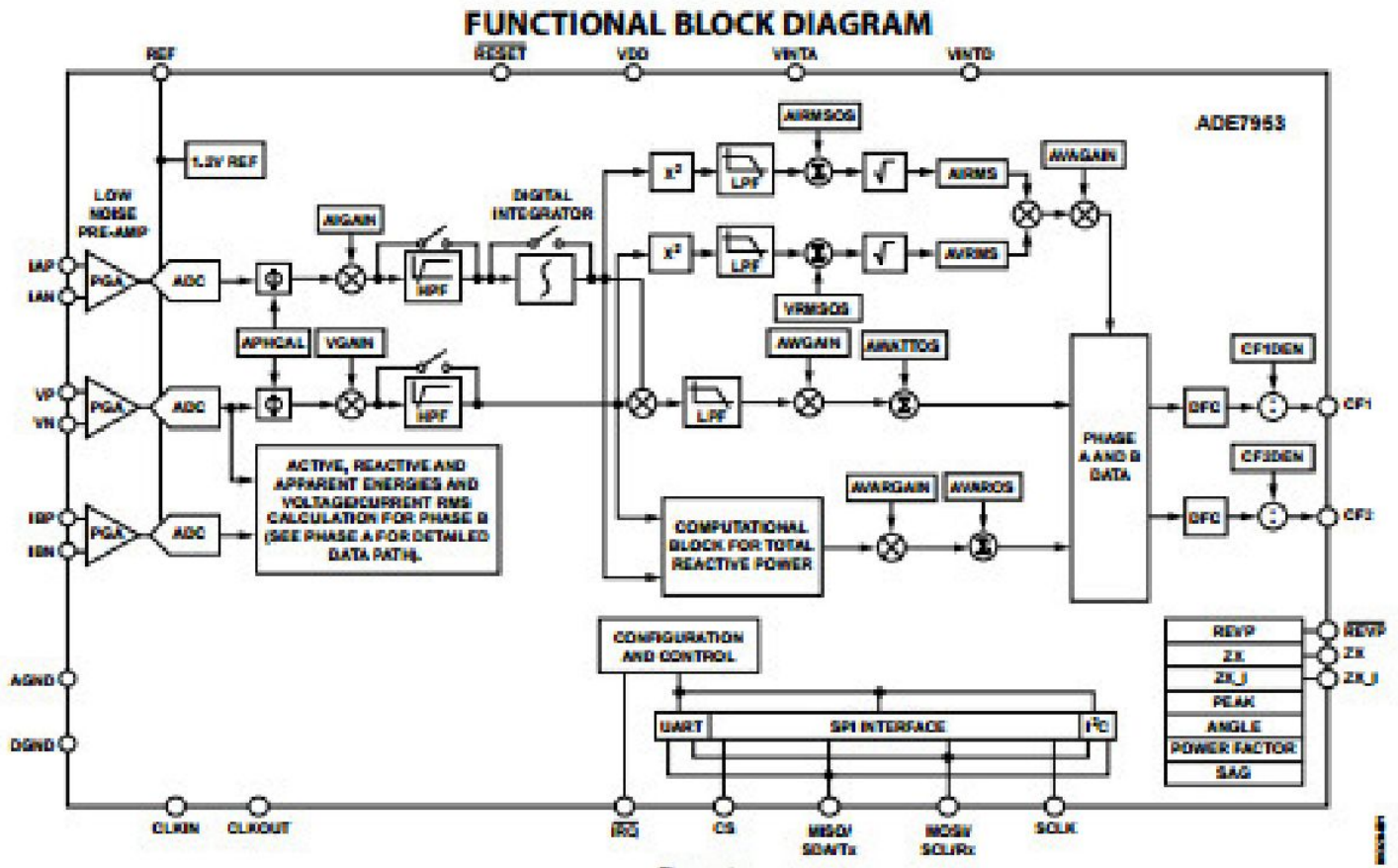


Figure 1.

ΣΔ–АЦП В МИКРОКОНВЕРТЕРЕ

ANALOG DEVICES

Low Power, Precision Analog Microcontroller with Dual Sigma-Delta ADCs, ARM Cortex-M3

Data Sheet **ADuCM360/ADuCM361**

FEATURES

- Analog input/output
  - Dual 24-bit ADCs (ADuCM360)
  - Single 24-bit ADC (ADuCM361)
  - Programmable ADC output rate (3.5 Hz to 3.906 kHz)
  - Simultaneous 50 Hz/60 Hz noise rejection
    - At 50 SPS continuous conversion mode
    - At 16.67 SPS single conversion mode
  - Flexible input mux for input channel selection to both ADCs
  - Two 24-bit multichannel ADCs (ADC0 and ADC1)
    - 6 differential or 11 single-ended input channels
    - 4 internal channels for monitoring DAC, temperature sensor, IOVDD/4, and AVDD/4 (ADC1 only)
    - Programmable gain (1 to 128)
    - RMS noise: 52 nV at 3.53 Hz, 200 nV at 50 Hz
  - Programmable sensor excitation current sources
  - On-chip precision voltage reference
  - Single 12-bit voltage output DAC
    - NPN mode for 4 mA to 20 mA loop applications
- Microcontroller
  - ARM Cortex-M3 32-bit processor
  - Serial wire download and debug
  - Internal watch crystal for wake-up timer
  - 16 MHz oscillator with 8-way programmable divider
- Memory
  - 128 kB Flash/EE memory, 8 kB SRAM
  - In-circuit debug/download via serial wire and UART
- Power supply range: 1.8 V to 3.6 V (maximum)
- Power consumption, MCU active mode
  - Core consumes 290 µA/MHz
  - Overall system current consumption of 1.0 mA with core operating at 500 kHz (both ADCs on, input buffers off, PGA gain of 4, one SPI port on, and all timers on)
- Power consumption, power-down mode: 4 µA (wake-up timer active)
- On-chip peripherals
  - UART, I²C, and 2 × SPI serial I/O
  - 16-bit PWM controller
  - 19-pin multifunction GPIO port
  - 2 general-purpose timers
  - Wake-up timer/watchdog timer
  - Multichannel DMA and interrupt controller
- Package and temperature range
  - 48-lead, 7 mm × 7 mm LFCSP
  - Specified for –40°C to +125°C operation
- Development tools
  - Low cost QuickStart Development System
  - Third-party compiler and emulator tool support
- Multiple functional safety features for improved diagnostics

APPLICATIONS

- Industrial automation and process control
- Intelligent precision sensing systems
- 4 mA to 20 mA loop-powered smart sensor systems
- Medical devices, patient monitoring

СТРУКТУРА МИКРОКОНВЕРТЕРА ADuCM360 С ДВУМЯ АЦП

ADuCM360/ADuCM361 Data Sheet

FUNCTIONAL BLOCK DIAGRAMS

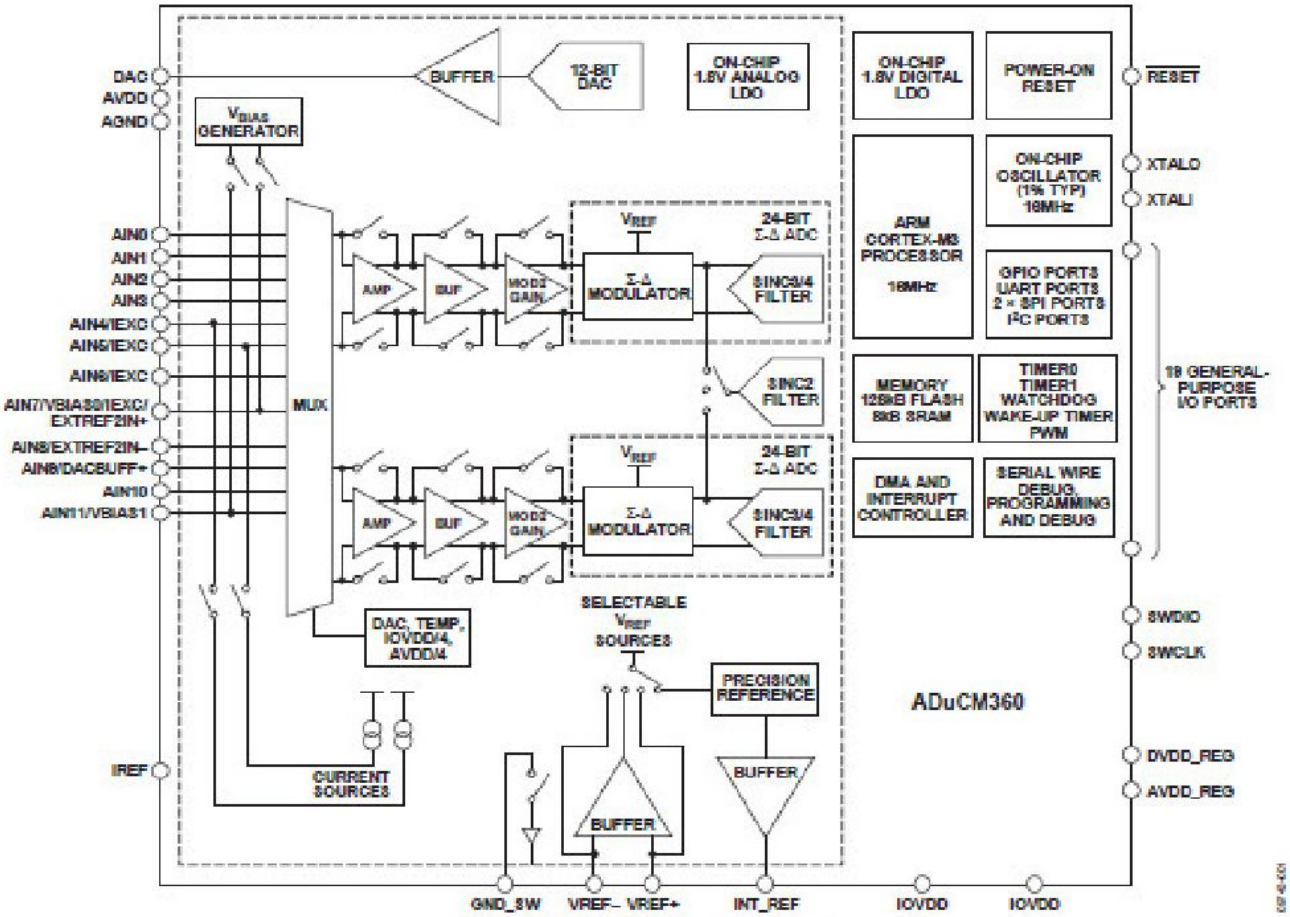


Figure 1. ADuCM360 Functional Block Diagram