Мікропроцесорна техніка

(лекція 4)
Благітко Б.Я.
2019 р.

PSoC Creator 4.2
Designing with PSoC 3/5

PSoC@3/5 Interrupts

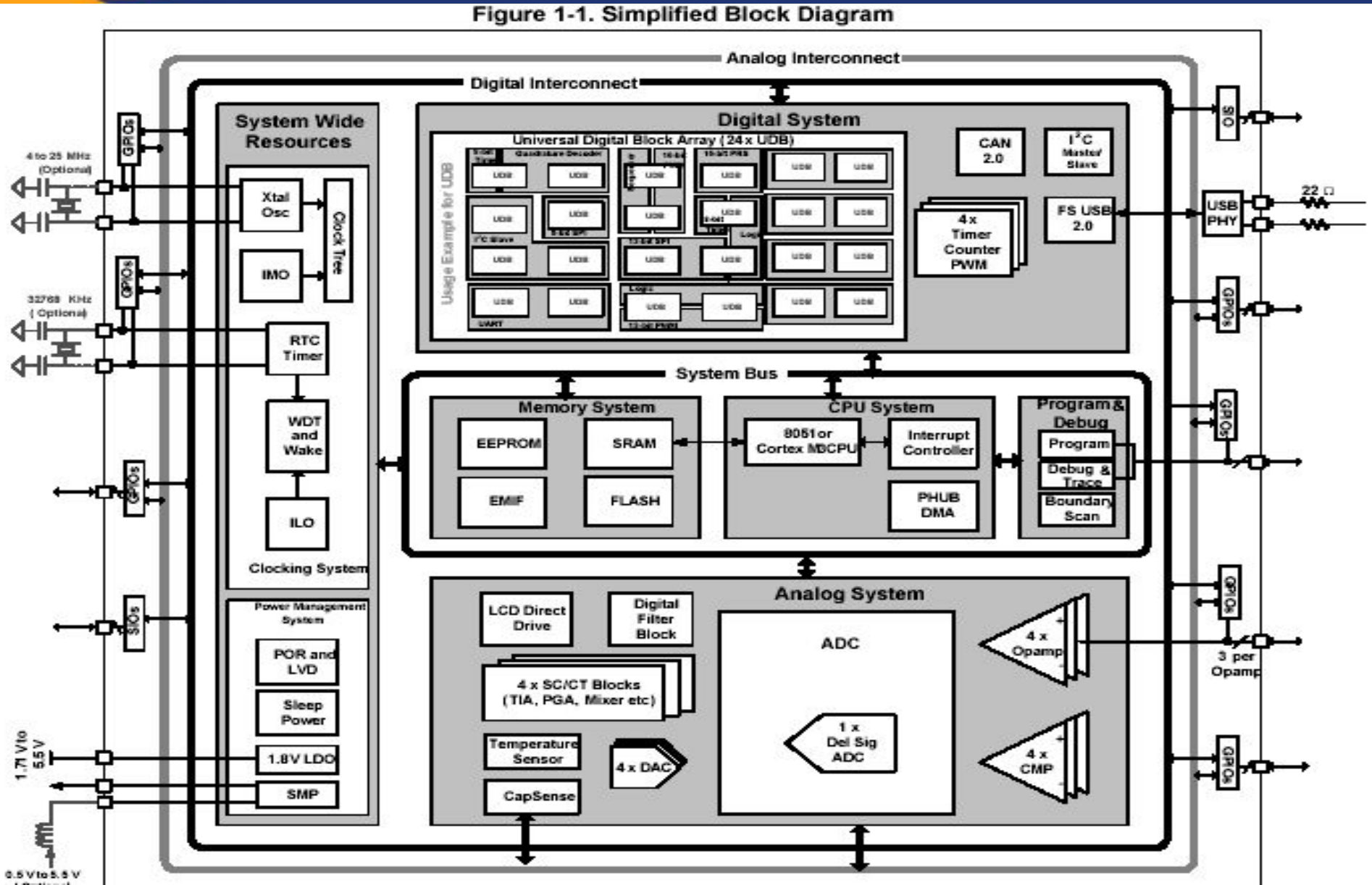
PSoC Creator 4.2
Designing with PSoC 3/5

Interrupts

Project Objective

- Generate interrupt for rising edge signal on pin
- Set a Flag in Interrupt Service routine (ISR)
- Increment Count variable in main code if Flag is set
- Clear the Flag in main code

Модулі PSoC@3/5



Цифрові модулі

Figure 7-3. Component Catalog

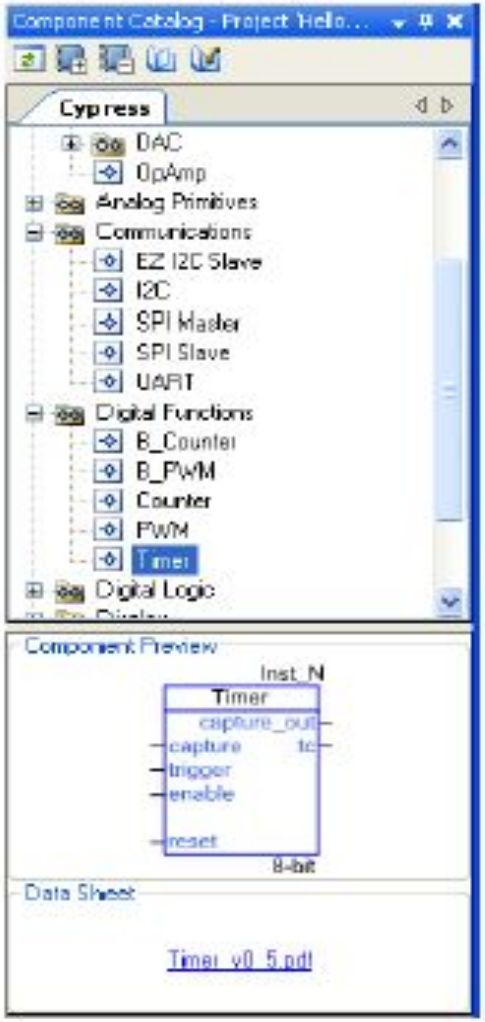
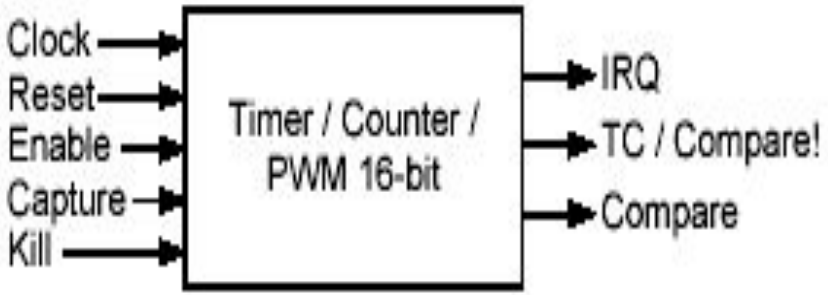
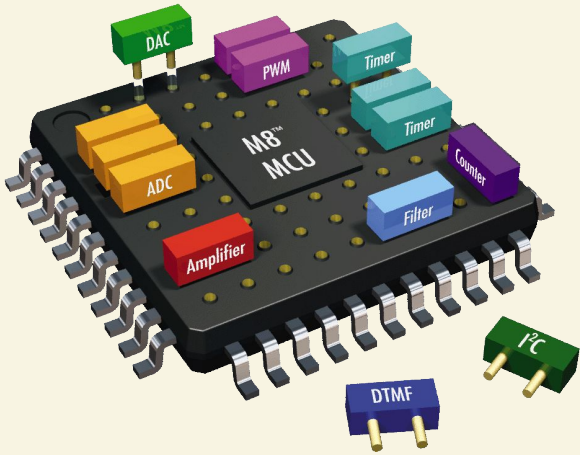


Figure 7-21. Timer/Counter/PWM





PWMs, Timers and Counters

PWMs, **Timer**s and **Counter**s share many capabilities but each provides specific capabilities.

When to Use a PWM

The most common use of the **PWM** is to generate periodic waveforms with adjustable duty cycles. The PWM also provides optimized features for power control, motor control, switching regulators and lighting control. The PWM can also be used as a clock divider by driving a clock into the clock input and using the terminal count or a PWM output as the divided clock output.

When to Use a Counter

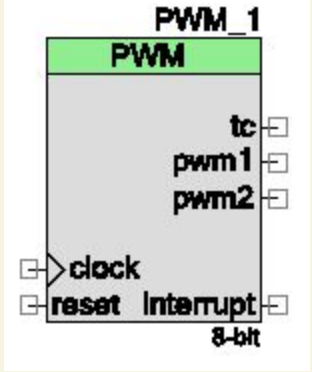
A **Counter** component is better used in situations that require the counting of a number of events but also provides rising edge capture input as well as a compare output.

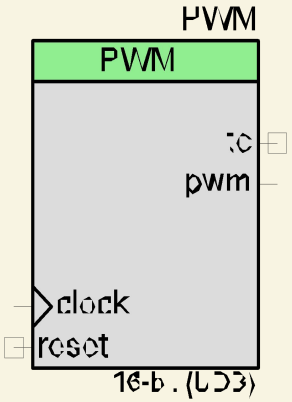
When to Use a Timer

A **Timer** component is better used in situations focused on timing the length of events, measuring the interval of multiple rising and/or falling edges, or for multiple capture events.

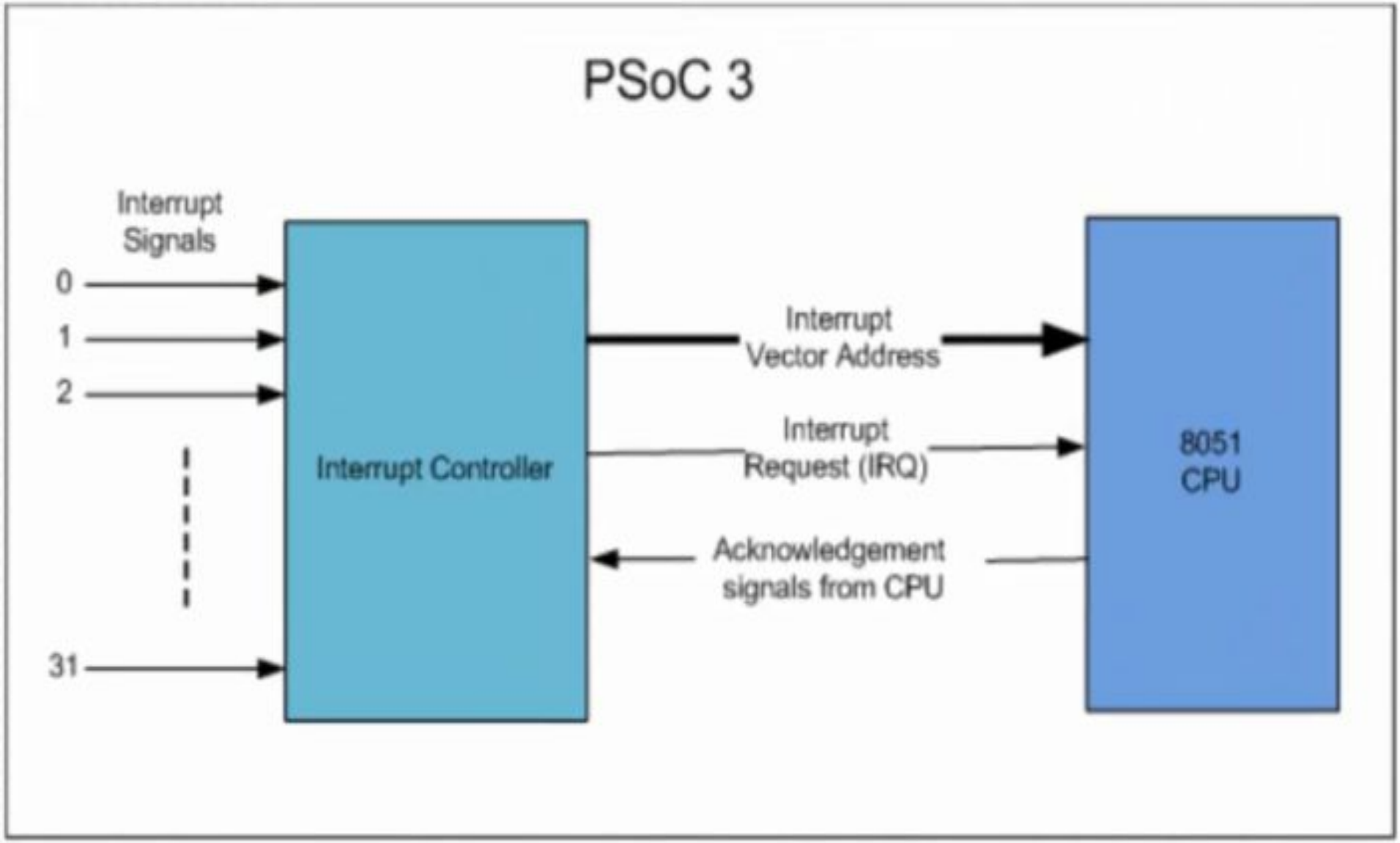
PWM

Output	May Be Hidden	Description
tc	N	The terminal count output is '1' when the period counter is equal to zero. In normal operation this output will be '1' for a single cycle where the counter is reloaded with period. If the PWM is stopped with the period counter equal to zero then this signal will remain high until the period counter is no longer zero. This output is synchronized to the block clock input of the component.
interrupt	Y	The interrupt output is the logical OR of the group of possible interrupt sources. This signal will go high while any of the enabled interrupt sources are true. The interrupt output shall remain asserted until the Status Register is read out by the software. In order to receive subsequent interrupts, the interrupt shall be cleared by reading the Status Register using the PWM_ReadStatusRegister() API. The interrupt output is not visible if the Use Interrupt parameter is not set. This allows the status register to be removed for resource optimization as necessary.
pwm/pwm1	Y	The pwm or pwm1 output is the first or only pulse width modulated output. This signal is defined by PWM Mode, compare modes(s), and compare value(s) as indicated in waveforms in the Configure dialog. When the instance is configured in one output, Dual Edged, Hardware Select, Center Aligned, or Dither PWM Modes, then the output "pwm" is visible. Otherwise the output "pwm1" is visible with "pwm2" the other pulse width signal. This output is synchronized to the block clock input of the component.

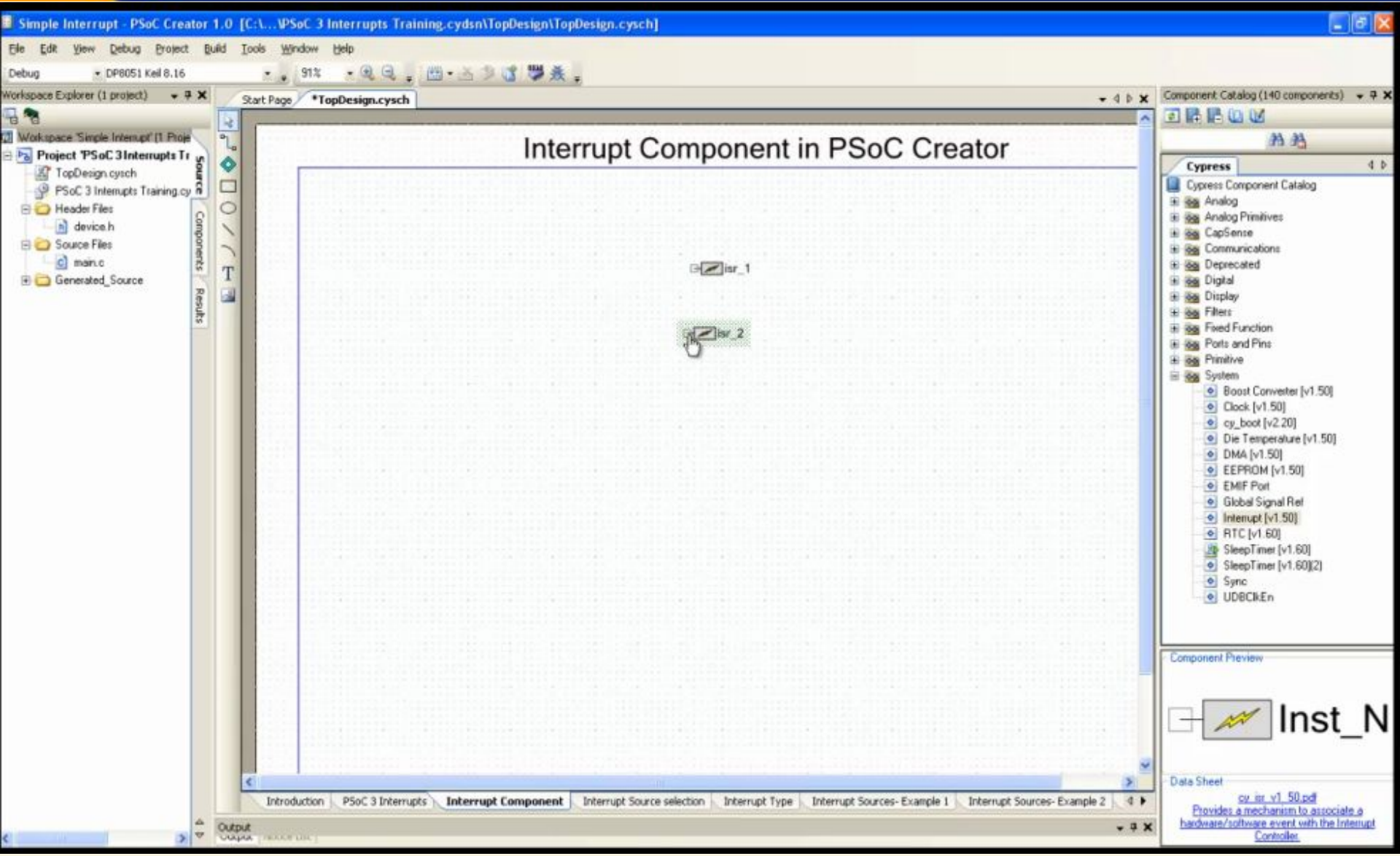




Interrupts


PSoC 3
Interrupt Signals
0
1
2
31
Interrupt Controller
Interrupt Vector Address
Interrupt Request (IRQ)
Acknowledgement signals from CPU
8051 CPU

Interrupts


Simple Interrupt - PSoC Creator 1.0 [C:\...\PSoC 3 Interrupts Training.cydsn\TopDesign\TopDesign.cysch]
File Edit View Debug Project Build Tools Window Help
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Workspace Explorer (1 project)
Workspace 'Simple Interrupt' (1 Proje
Project 'PSoC 3 Interrupts Tr
TopDesign.cysch
PSoC 3 Interrupts Training.cy
Header Files
device.h
Source Files
main.c
Generated_Source
Source
Components
Results
Start Page
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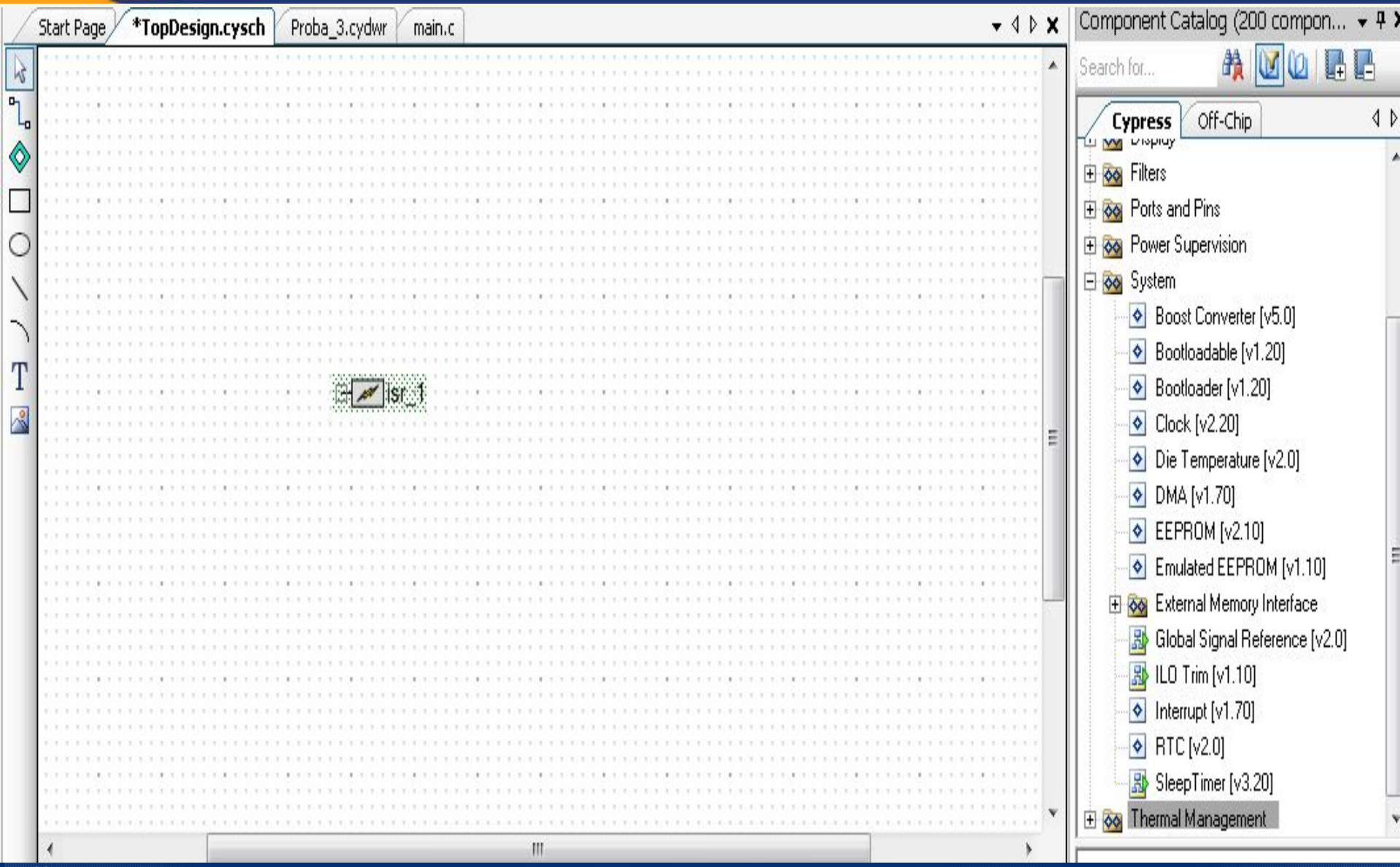
Interrupt Component in PSoC Creator
isr_1
isr_2
Introduction
PSoC 3 Interrupts
Interrupt Component
Interrupt Source selection
Interrupt Type
Interrupt Sources- Example 1
Interrupt Sources- Example 2
Output
Component Catalog (140 components)
Cypress
Cypress Component Catalog
Analog
Analog Primitives
CapSense
Communications
Deprecated
Digital
Display
Filters
Fixed Function
Ports and Pins
Primitive
System
Boost Converter [v1.50]
Clock [v1.50]
cy_boot [v2.20]
Die Temperature [v1.50]
DMA [v1.50]
EEPROM [v1.50]
EMIF Port
Global Signal Rel
Interrupt [v1.50]
RTC [v1.60]
SleepTimer [v1.60]
SleepTimer [v1.60](2)
Sync
UDBClkEn
Component Preview
Inst_N
Data Sheet
cy_isr_v1_50.pdf
Provides a mechanism to associate a hardware/software event with the Interrupt Controller.

Interrupts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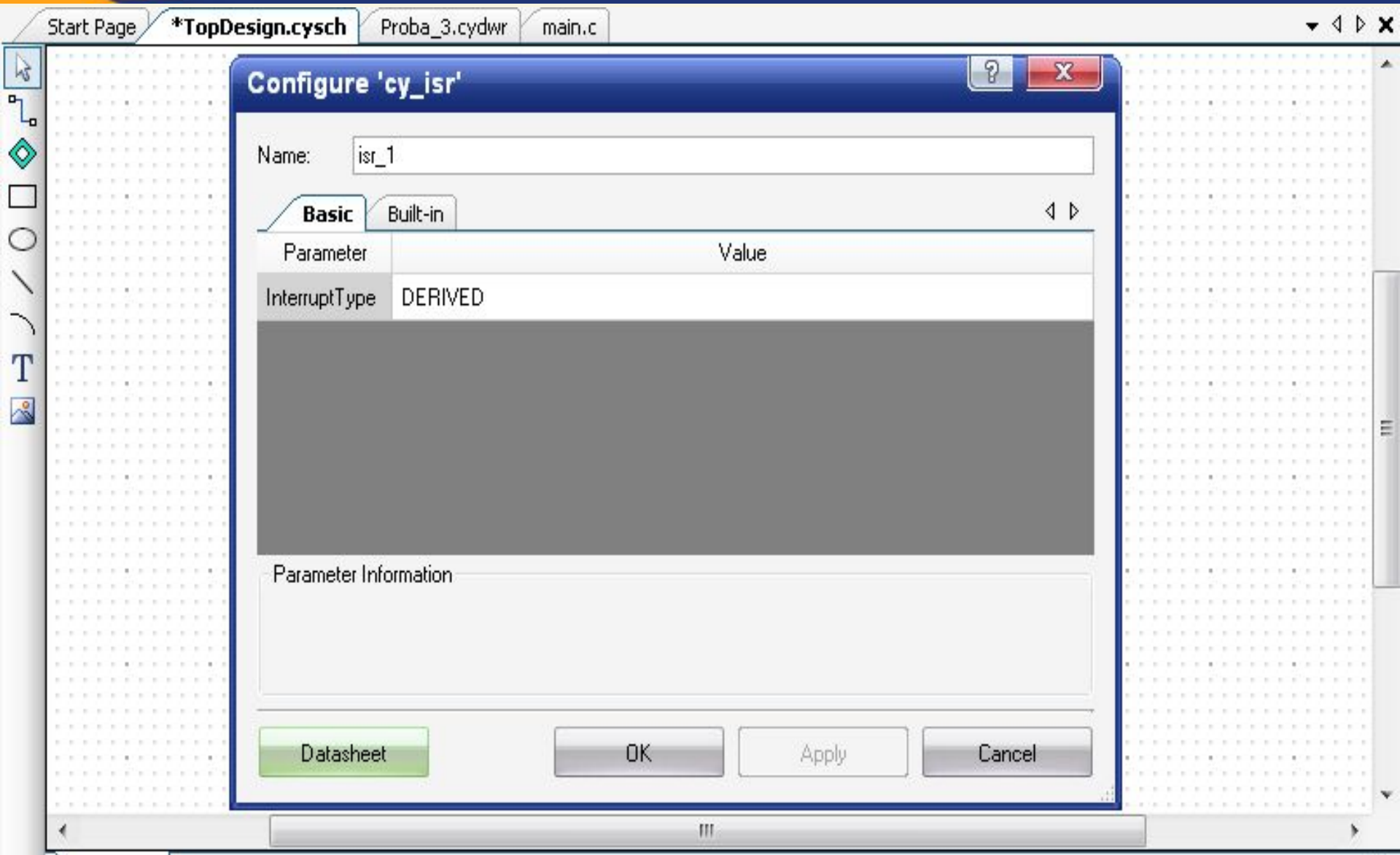
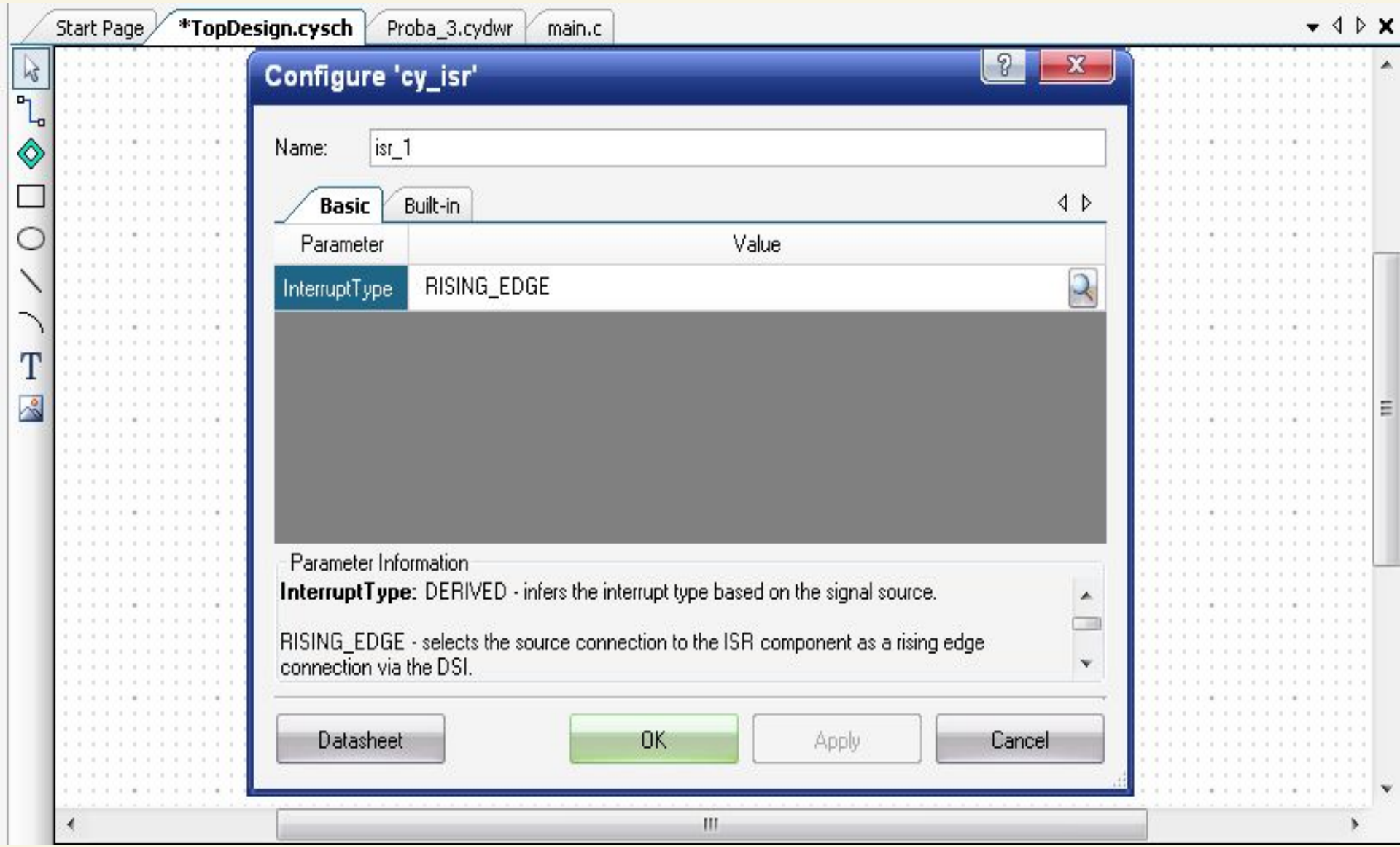
main.c
isr_1
Component Catalog (200 compon...
Search for...
Cypress
Off-Chip
Filters
Ports and Pins
Power Supervision
System
Boost Converter [v5.0]
Bootloadable [v1.20]
Bootloader [v1.20]
Clock [v2.20]
Die Temperature [v2.0]
DMA [v1.70]
EEPROM [v2.10]
Emulated EEPROM [v1.10]
External Memory Interface
Global Signal Reference [v2.0]
ILO Trim [v1.10]
Interrupt [v1.70]
RTC [v2.0]
SleepTimer [v3.20]
Thermal Management

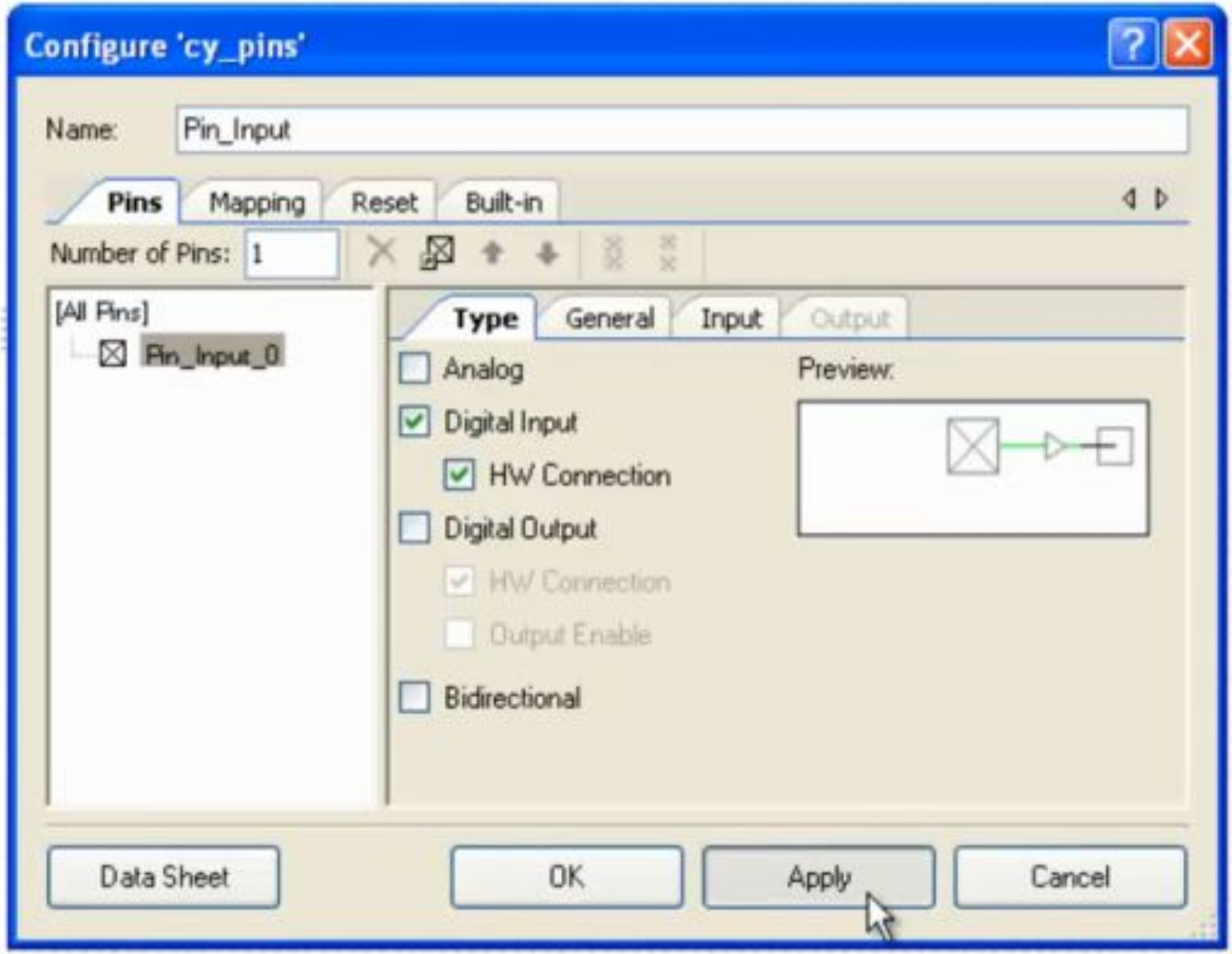
Interrupts


Start Page
*TopDesign.cysch
Proba_3.cydwr
main.c
Configure 'cy_isr'
Name:
isr_1
Basic
Built-in
Parameter
Value
InterruptType
DERIVED
Parameter Information
Datasheet
OK
Apply
Cancel

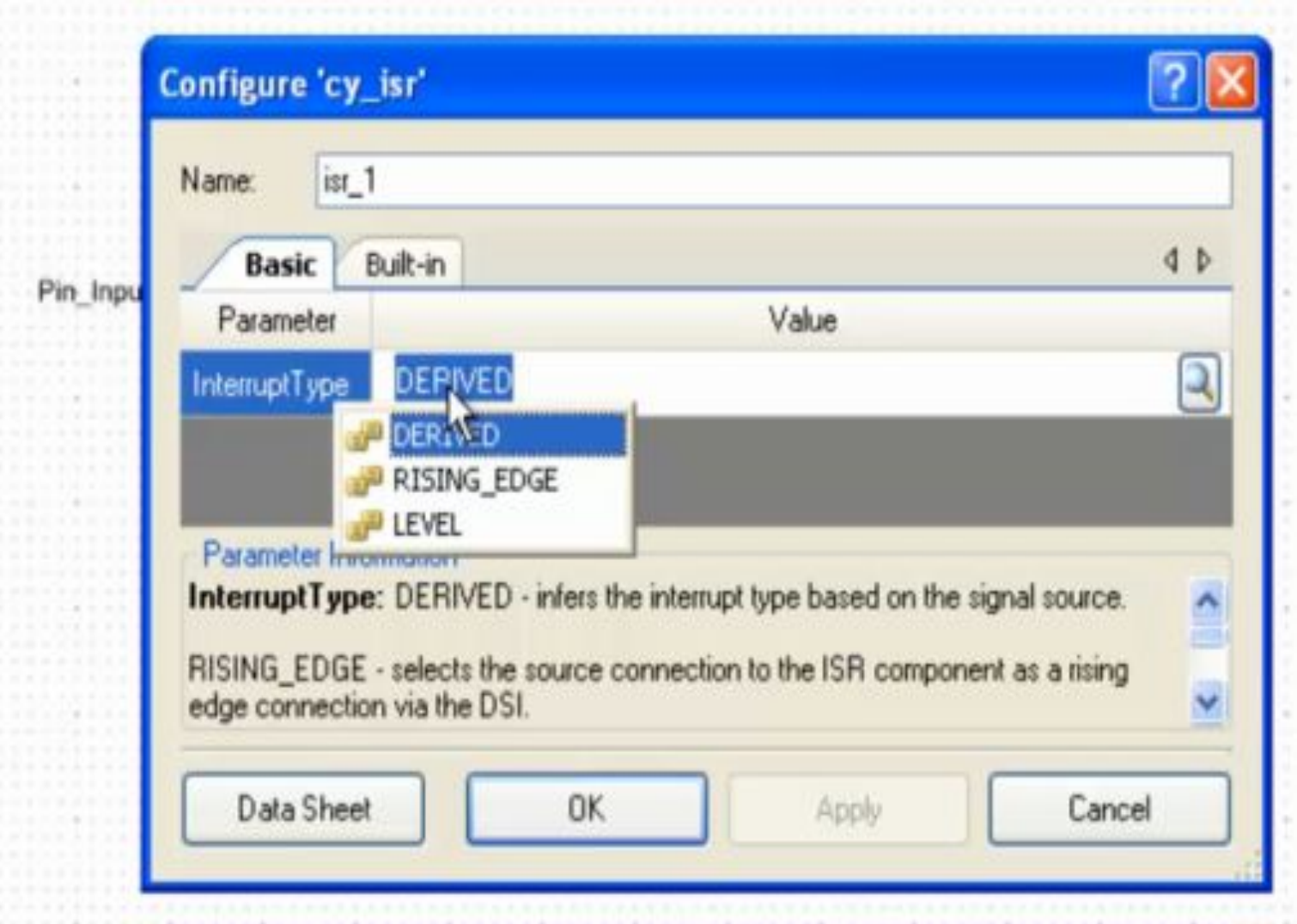
Interrupts


Start Page
*TopDesign.cysch
Proba_3.cydwr
main.c
Configure 'cy_isr'
Name:
isr_1
Basic
Built-in
Parameter
Value
InterruptType
RISING_EDGE
Parameter Information
InterruptType: DERIVED - infers the interrupt type based on the signal source.
RISING_EDGE - selects the source connection to the ISR component as a rising edge connection via the DSI.
Datasheet
OK
Apply
Cancel

Interrupts


Configure 'cy_pins'
Name:
Pin_Input
Pins
Mapping
Reset
Built-in
Number of Pins:
1
[All Pins]
Pin_Input_0
Type
General
Input
Output
Analog
Digital Input
HW Connection
Digital Output
HW Connection
Output Enable
Bidirectional
Preview:
Data Sheet
OK
Apply
Cancel

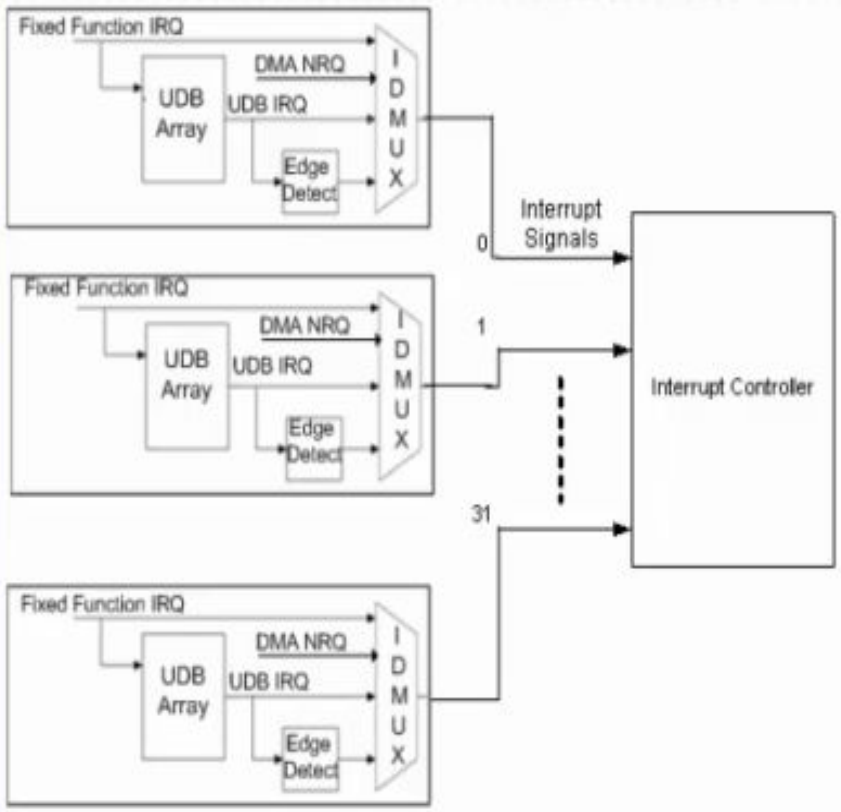
Interrupts


Configure 'cy_isr'
Name:
isr_1
Basic
Built-in
Parameter
Value
InterruptType
DERIVED
DERIVED
RISING_EDGE
LEVEL
InterruptType: DERIVED - infers the interrupt type based on the signal source.
RISING_EDGE - selects the source connection to the ISR component as a rising edge connection via the DSI.
Data Sheet
OK
Apply
Cancel

Interrupts

Interrupts

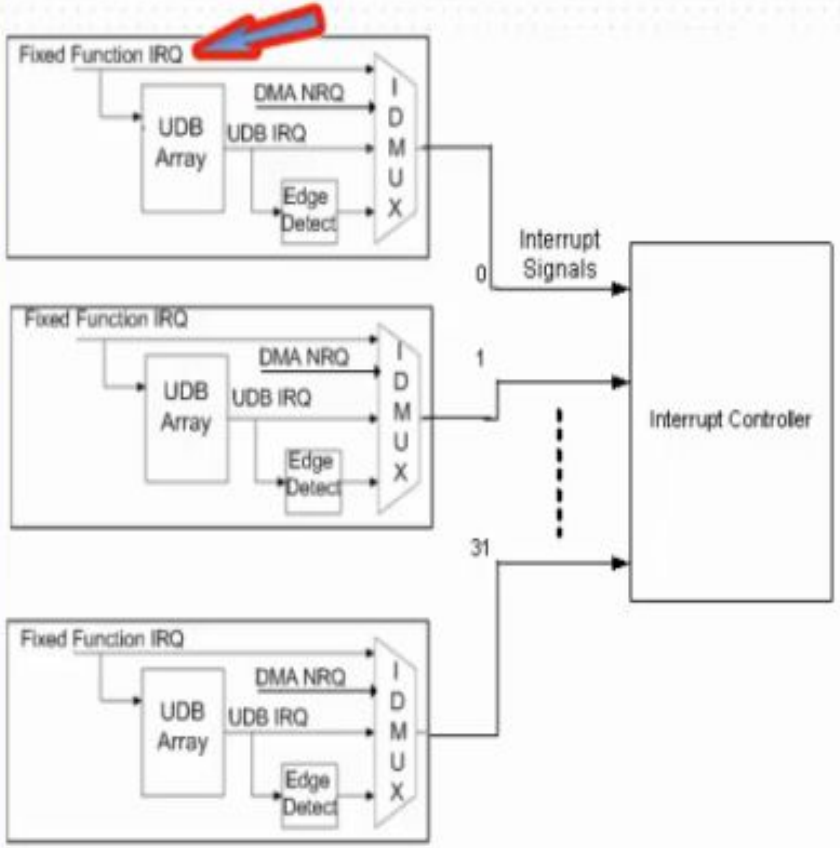
Interrupt Sources



Interrupt Request Source (IRQ) Type	Examples
Fixed function IRQ's	ADC End of Conversion (EoC), Fixed Function Timer, Counter Interrupts, Port Interrupt Control Unit (PICU), Sleep Timer, Low Voltage Detect (LVD)
Universal Digital Block (UDB) array IRQ's	Any digital output signal on chip, UART, SPI component interrupts, UDB based Timer, Counter, PWM interrupts, Fixed function IRQ's can also be UDB IRQ's
Direct Memory Access (DMA) NRQ's	DMA channel Transfer complete (NRQ) signals

Interrupts

Interrupt Sources



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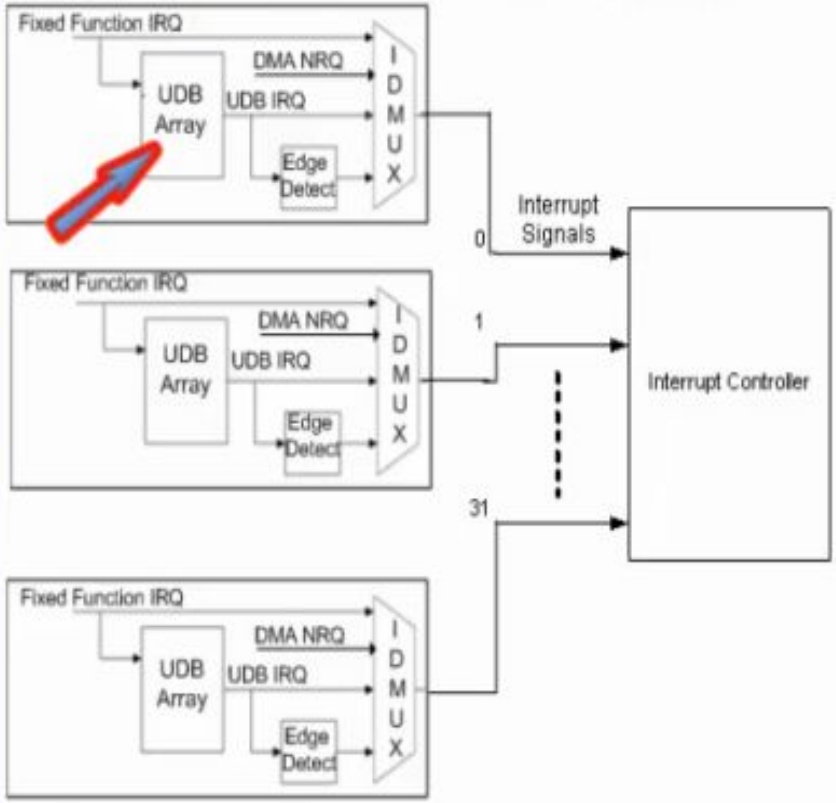
Interrupts

Interrupt Sources



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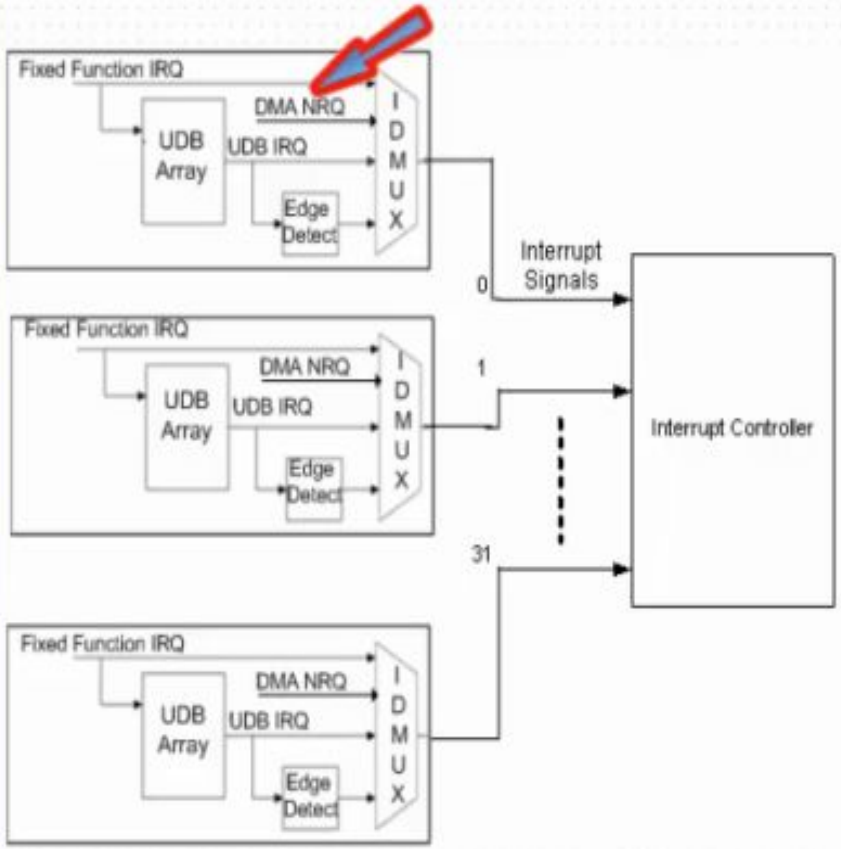
Interrupts

Interrupt Sources



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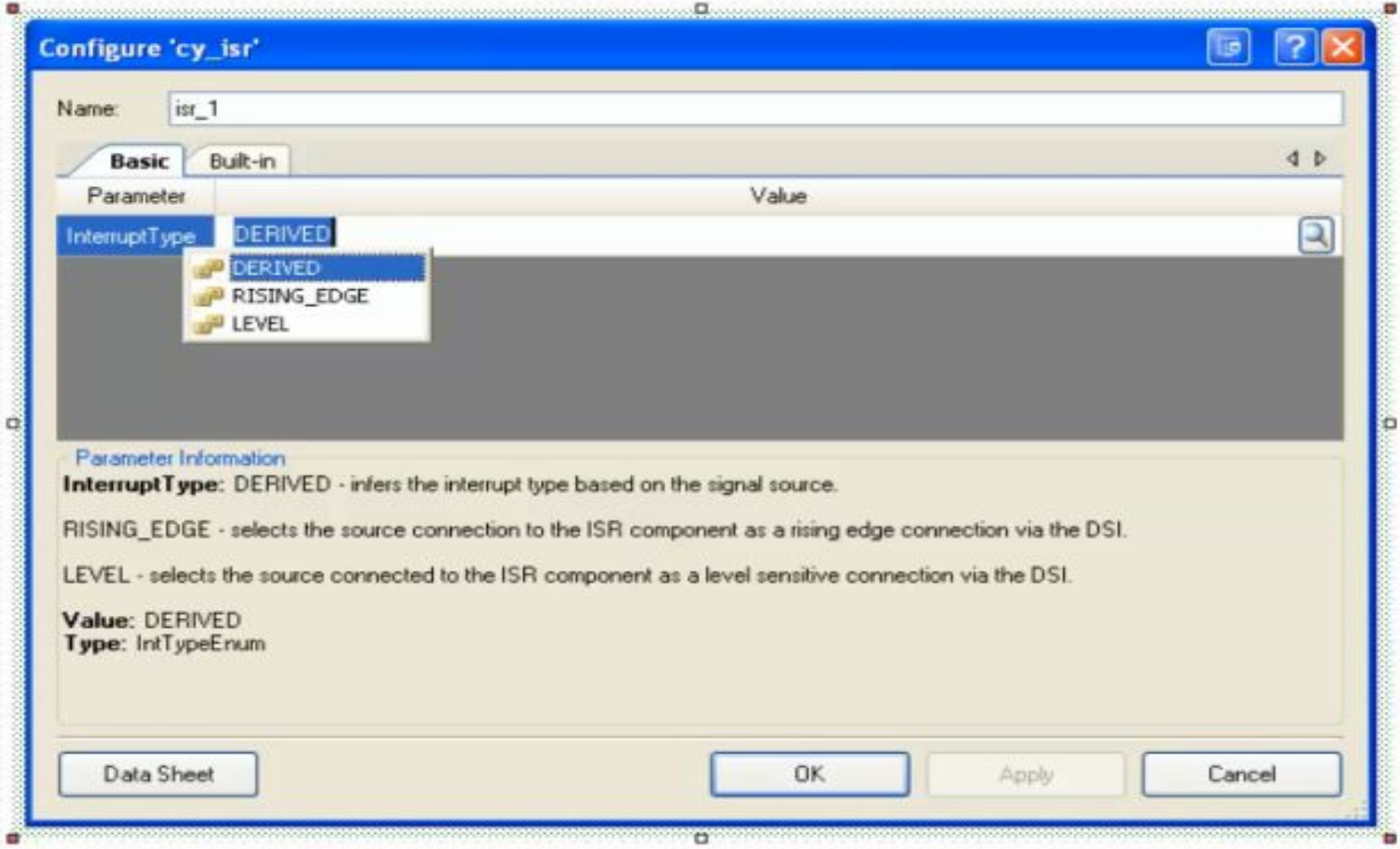
Direct Memory Access (DMA) NRQ's	DMA channel Transfer complete (NRQ) signals

Interrupts

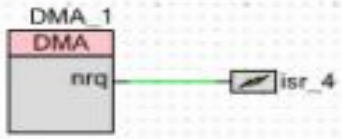
Interrupt Type selection



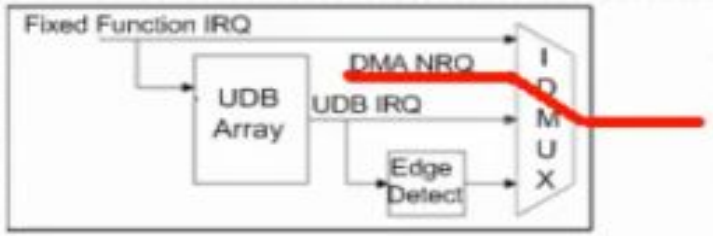
Interrupts

Interrupt Sources

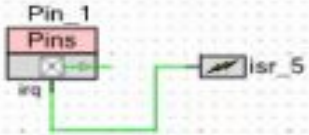
1.) DMA nrq Interrupt



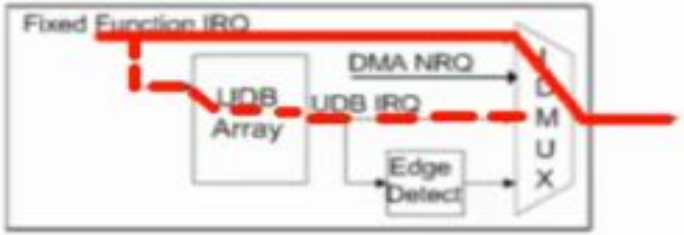
Derived

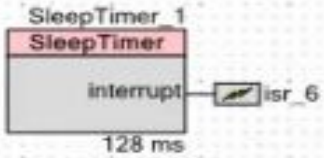


2.) Fixed Function Interrupts



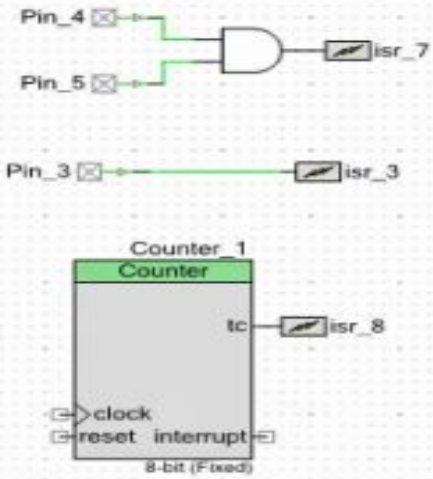
Derived



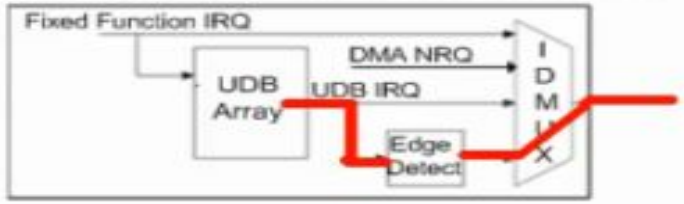


Interrupts

3.) Edge Triggered Interrupts

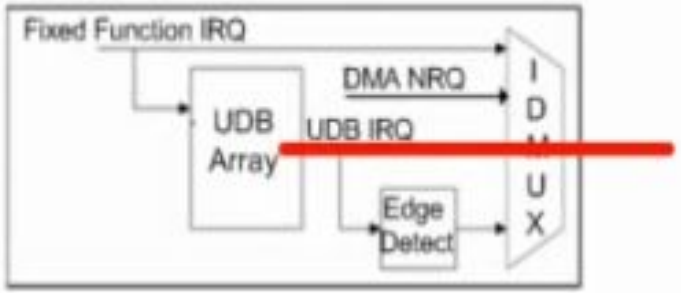


Derived (or) Rising Edge

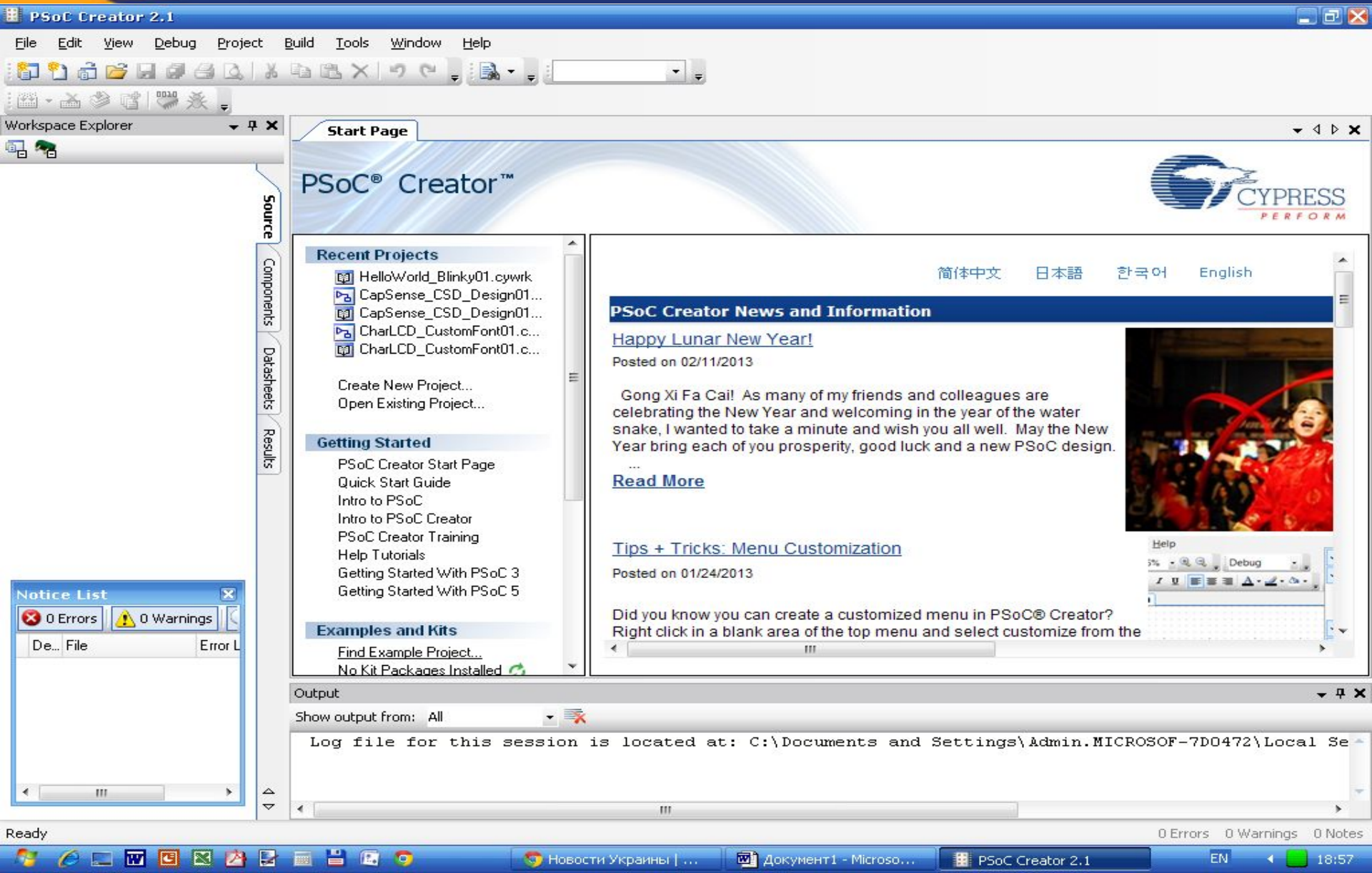


4.) Level Interrupt

Level



Creator


PSoC Creator 2.1
File Edit View Debug Project Build Tools Window Help
Workspace Explorer
Source
Components
Datasheets
Results
Start Page
PSoC® Creator™
CYPRESS PERFORM
Recent Projects
HelloWorld_Blinky01.cywrk
CapSense_CSD_Design01...
CapSense_CSD_Design01...
CharLCD_CustomFont01.c...
CharLCD_CustomFont01.c...
Create New Project...
Open Existing Project...
Getting Started
PSoC Creator Start Page
Quick Start Guide
Intro to PSoC
Intro to PSoC Creator
PSoC Creator Training
Help Tutorials
Getting Started With PSoC 3
Getting Started With PSoC 5
Examples and Kits
Find Example Project...
No Kit Packages Installed
简体中文 日本語 한국어 English
PSoC Creator News and Information
Happy Lunar New Year!
Posted on 02/11/2013
Gong Xi Fa Cai! As many of my friends and colleagues are celebrating the New Year and welcoming in the year of the water snake, I wanted to take a minute and wish you all well. May the New Year bring each of you prosperity, good luck and a new PSoC design.
...
Read More
Tips + Tricks: Menu Customization
Posted on 01/24/2013
Did you know you can create a customized menu in PSoC® Creator? Right click in a blank area of the top menu and select customize from the
Notice List
0 Errors
0 Warnings
De... File Error L
Output
Show output from: All
Log file for this session is located at: C:\Documents and Settings\Admin.MICROSOF-7D0472\Local Se
Ready
0 Errors 0 Warnings 0 Notes
Новости Украины | ...
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PSoC Creator 2.1
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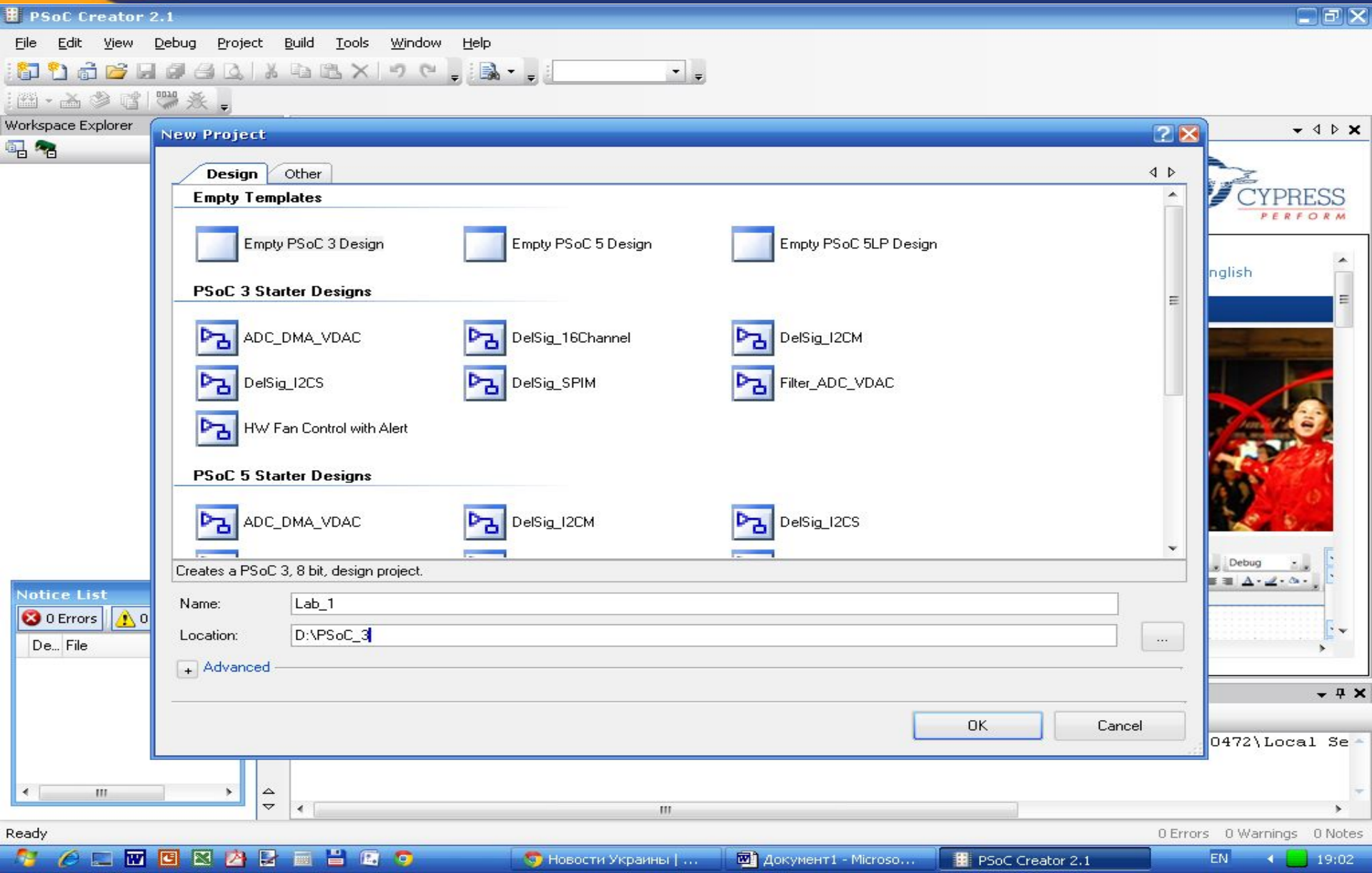
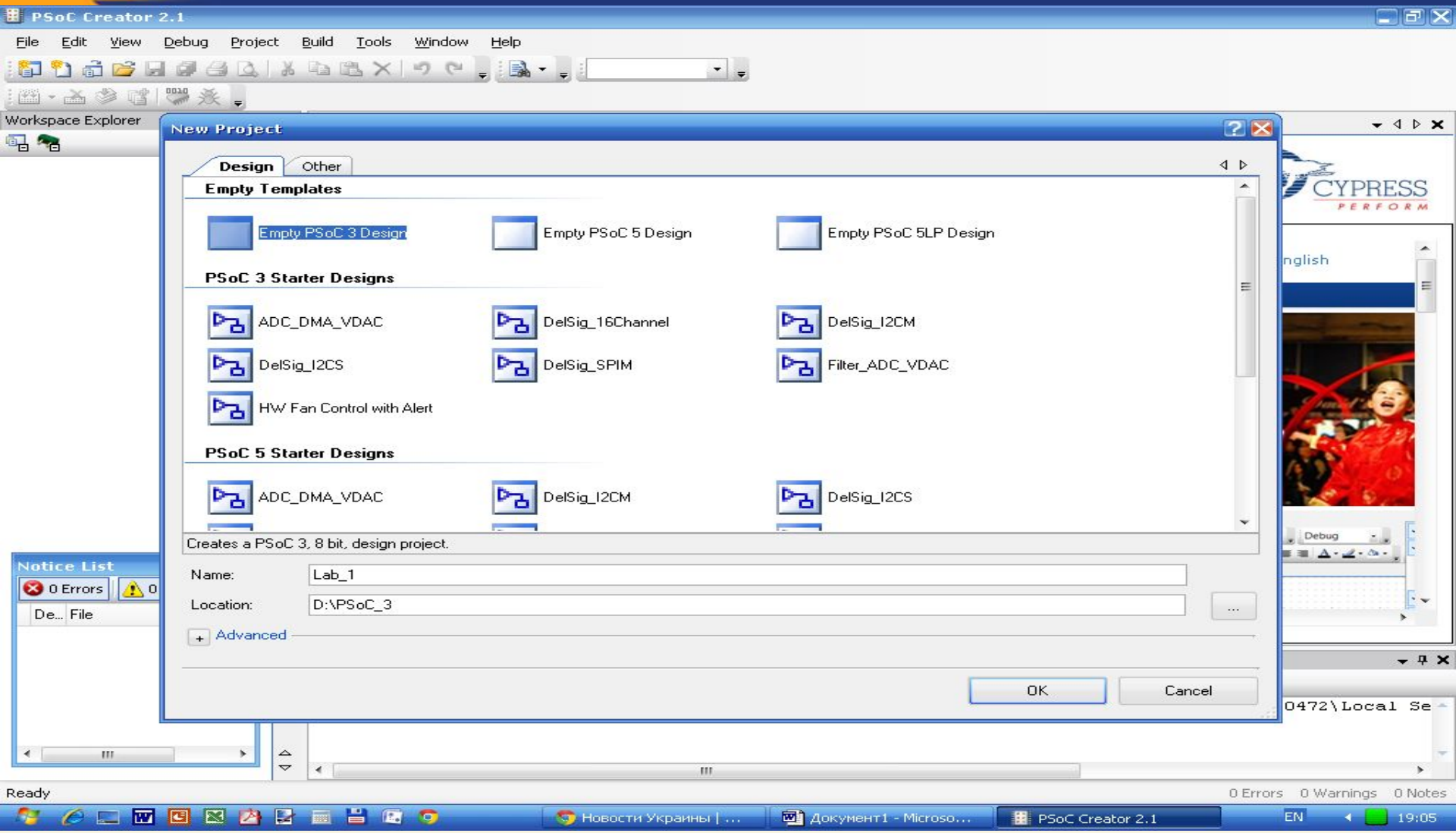
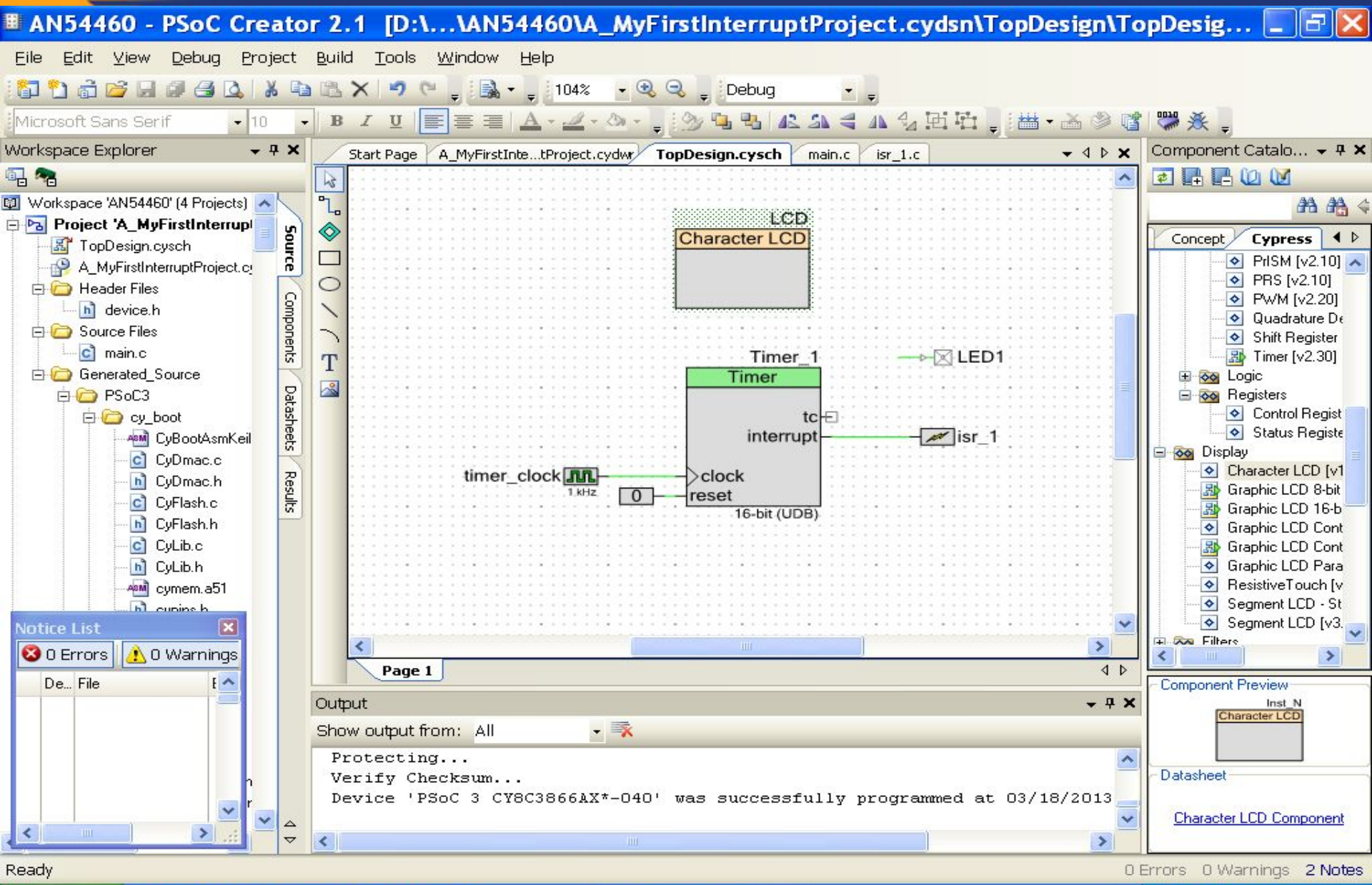
File – New - Projekt



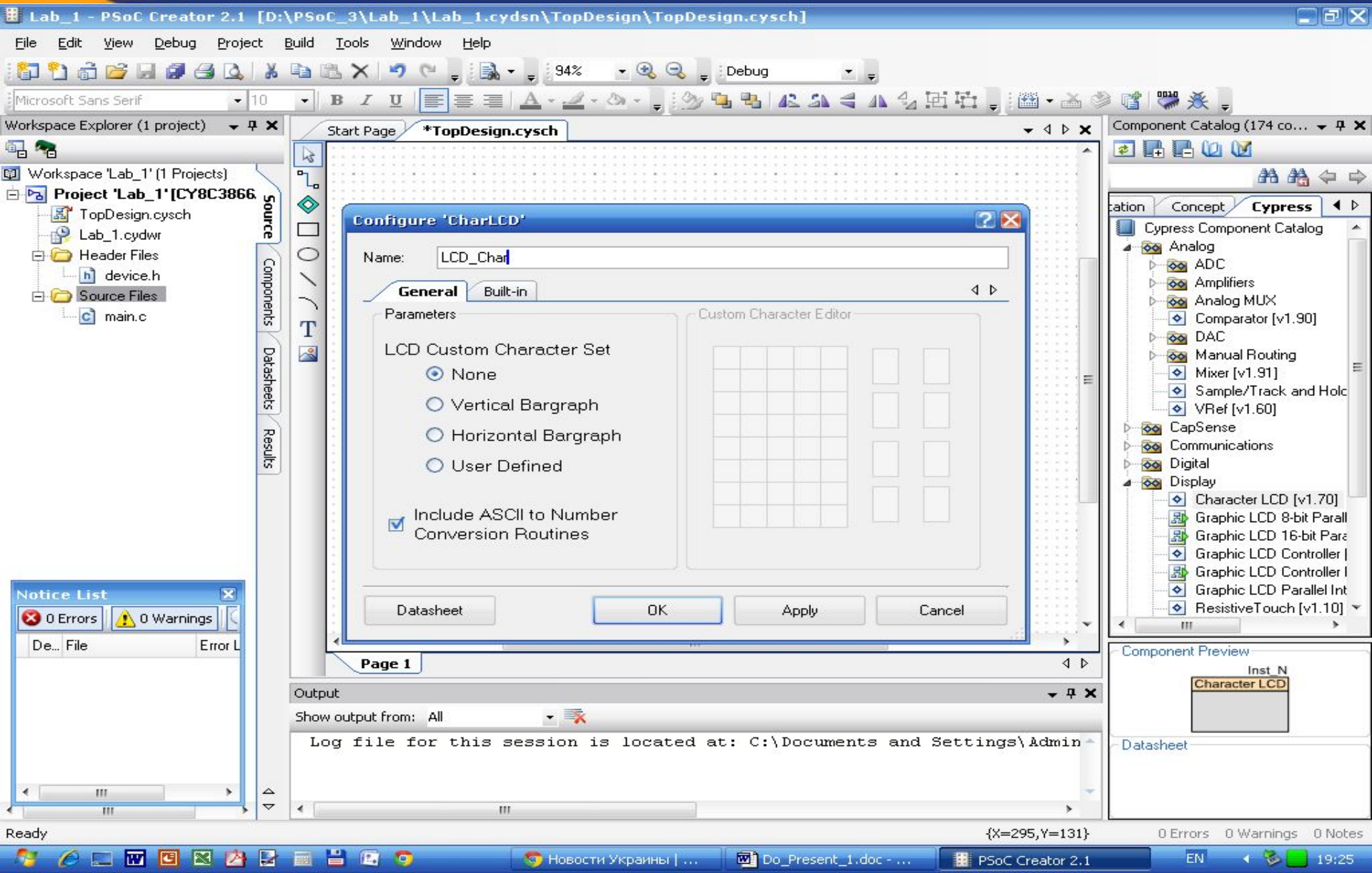
Empty PSoC 3 Design



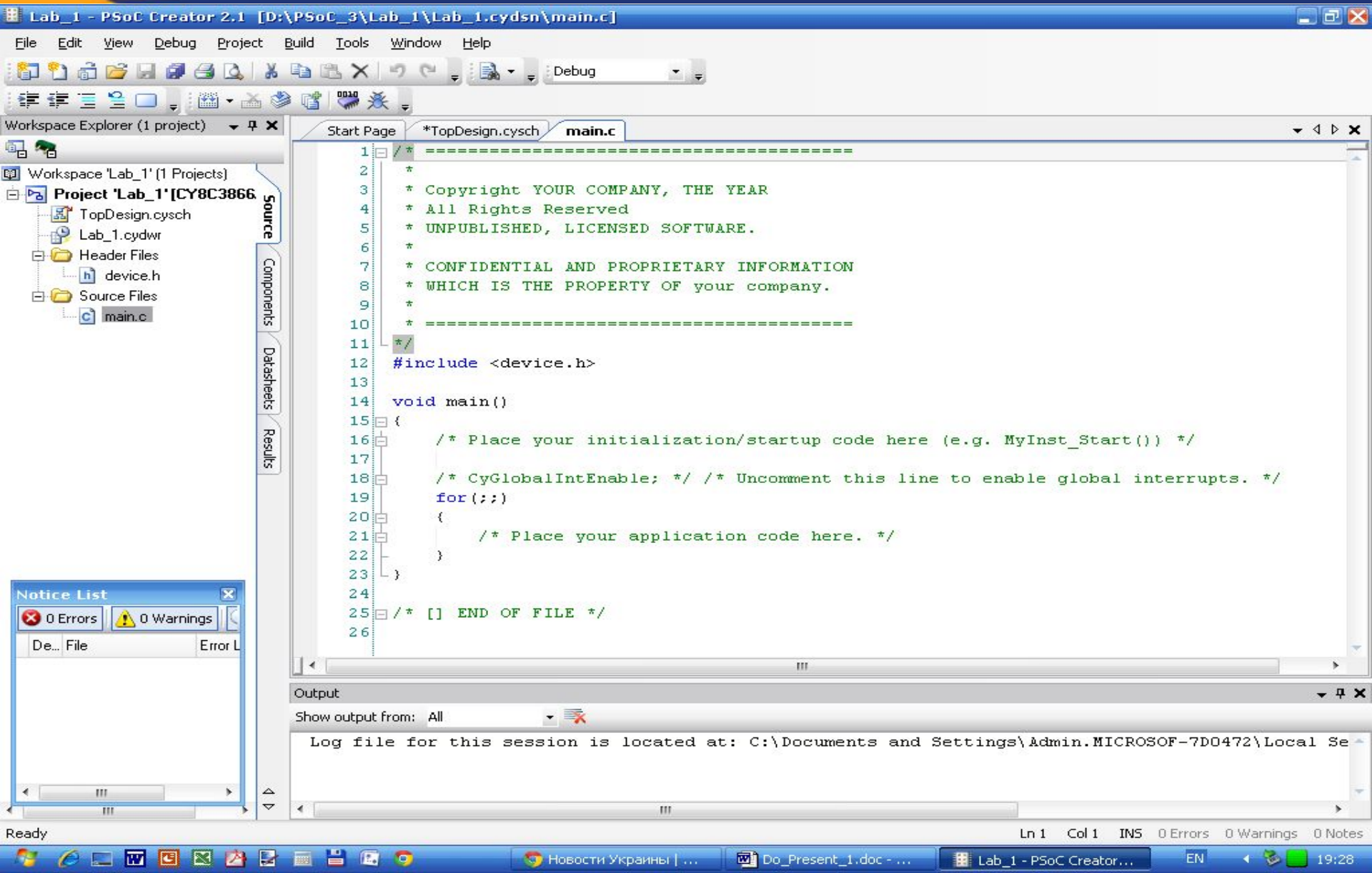
Lab_4 Interrupts



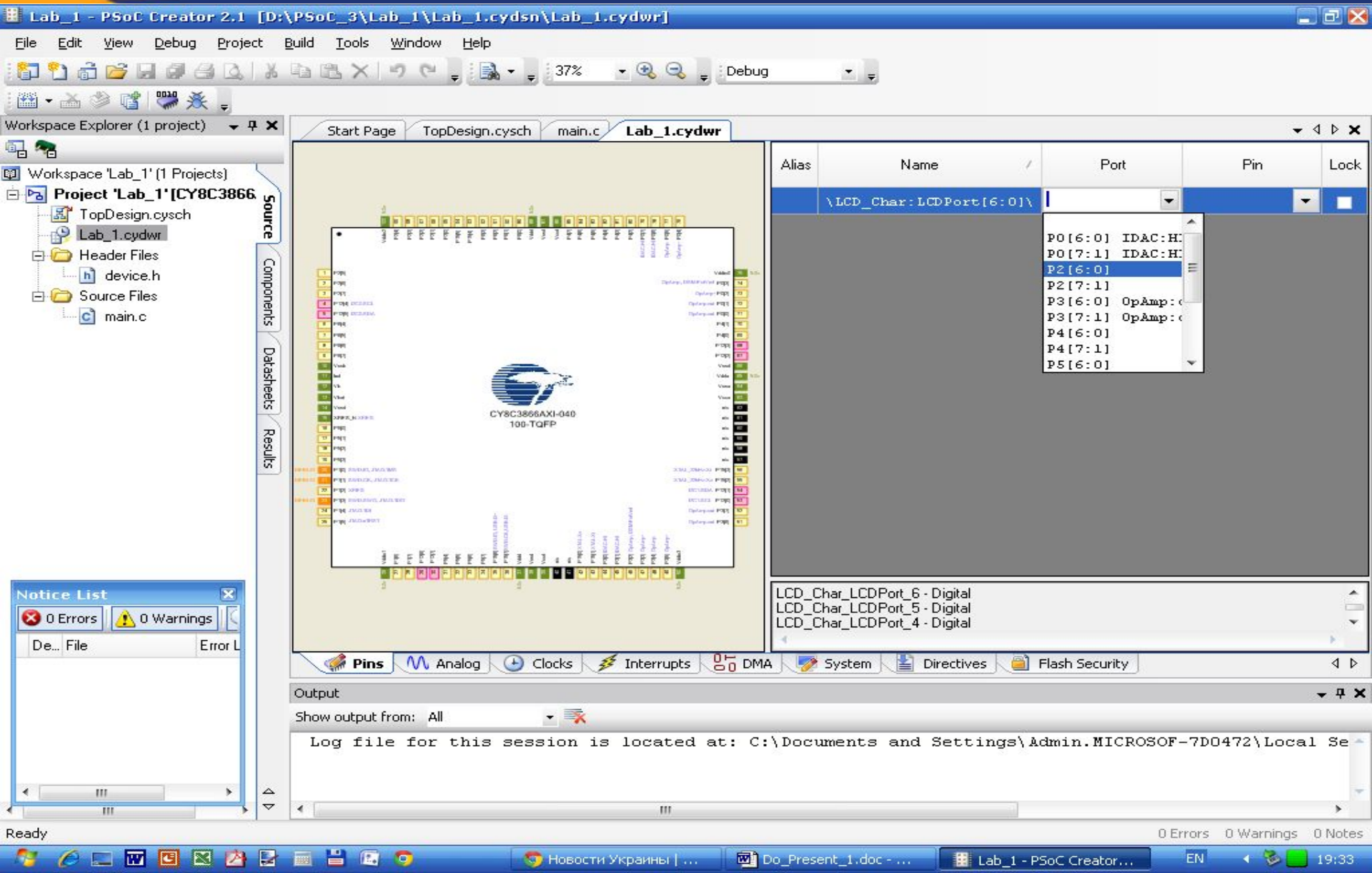
Configure LCD



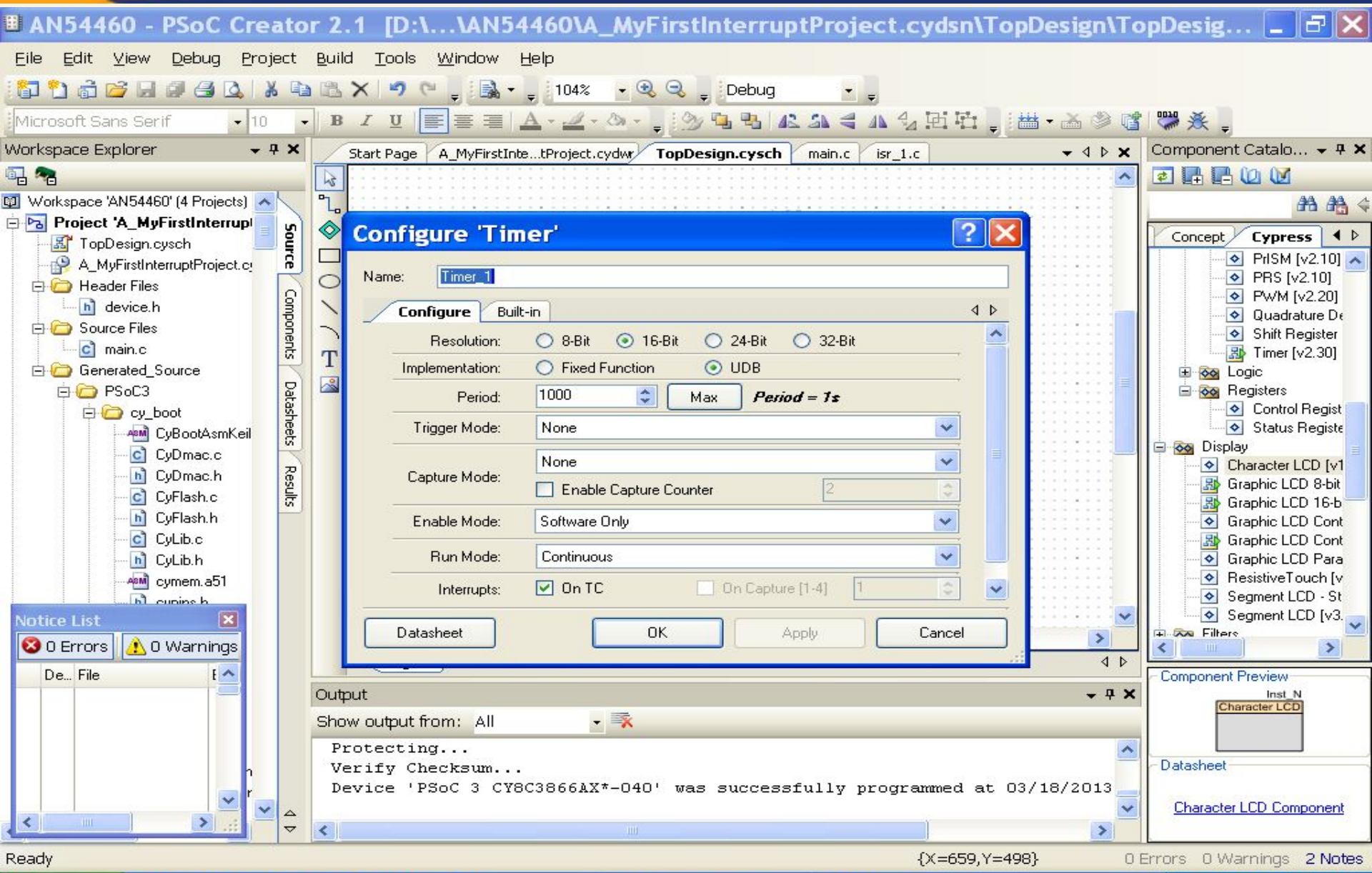
Main.c


Lab_1 - PSoC Creator 2.1 [D:\PSoC_3\Lab_1\Lab_1.cydsn\main.c]
File Edit View Debug Project Build Tools Window Help
Debug
Workspace Explorer (1 project)
Workspace 'Lab_1' (1 Projects)
Project 'Lab_1' [CY8C3866
TopDesign.cysch
Lab_1.cydwr
Header Files
device.h
Source Files
main.c
Source
Components
Datasheets
Results
Start Page
*TopDesign.cysch
main.c
1 /* ==
2 *
3 * Copyright YOUR COMPANY, THE YEAR
4 * All Rights Reserved
5 * UNPUBLISHED, LICENSED SOFTWARE.
6 *
7 * CONFIDENTIAL AND PROPRIETARY INFORMATION
8 * WHICH IS THE PROPERTY OF your company.
9 *
10 * ==
11 */
12 #include <device.h>
13
14 void main()
15 {
16 /* Place your initialization/startup code here (e.g. MyInst_Start()) */
17
18 /* CyGlobalIntEnable; */ /* Uncomment this line to enable global interrupts. */
19 for(;;)
20 {
21 /* Place your application code here. */
22 }
23 }
24
25 /* [] END OF FILE */
26
Notice List
0 Errors
0 Warnings
De... File Error L
Output
Show output from: All
Log file for this session is located at: C:\Documents and Settings\Admin.MICROSOF-7D0472\Local Se
Ready
Ln 1 Col 1 INS 0 Errors 0 Warnings 0 Notes
Новости Украины | ...
Do_Present_1.doc - ...
Lab_1 - PSoC Creator...
EN
19:28

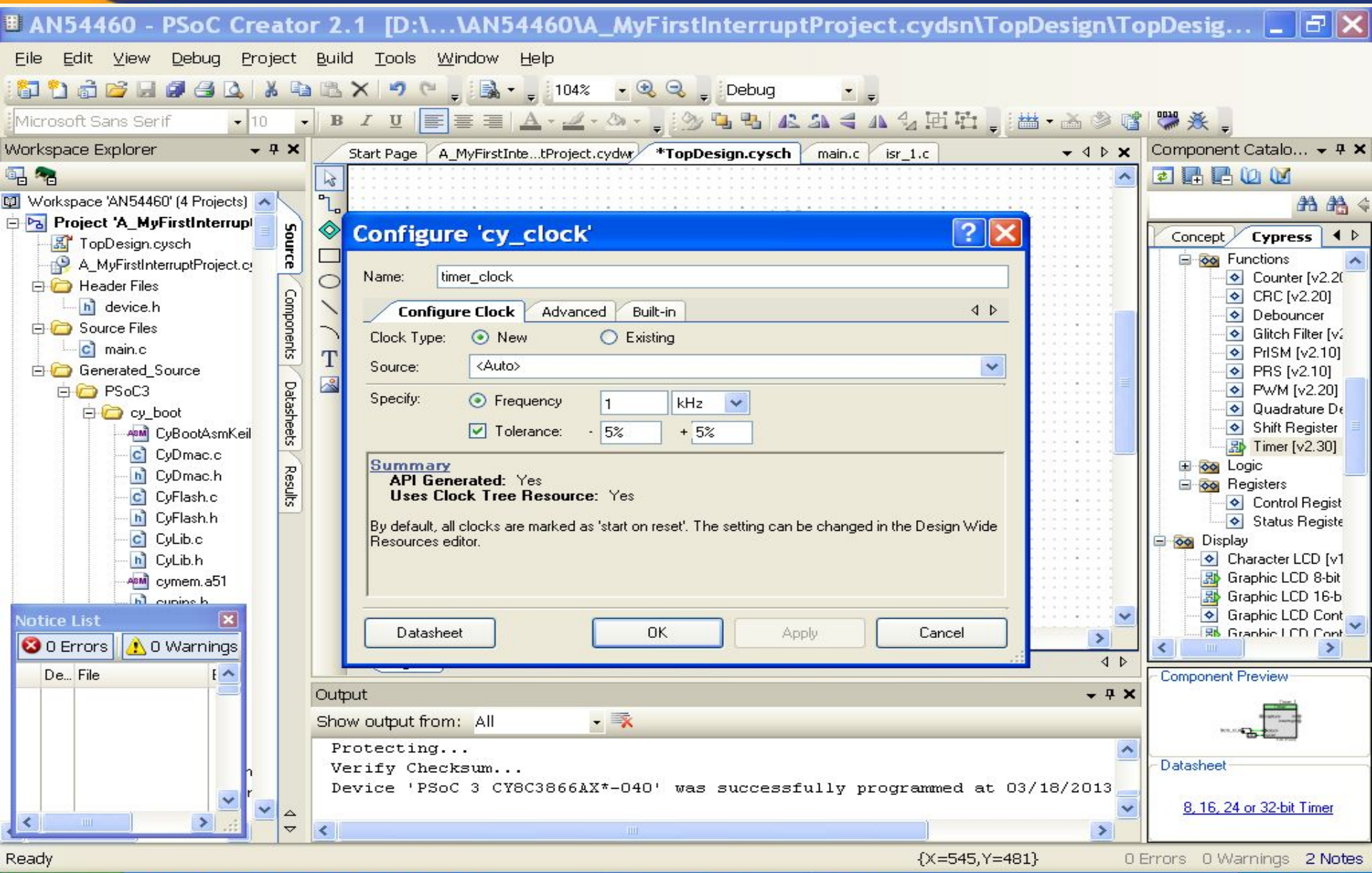
Lab_4.cywr


Lab_1 - PSoC Creator 2.1 [D:\PSoC_3\Lab_1\Lab_1.cydsn\Lab_1.cydwr]
File Edit View Debug Project Build Tools Window Help
Workspace Explorer (1 project)
Workspace 'Lab_1' (1 Projects)
Project 'Lab_1' [CY8C3866
TopDesign.cysch
Lab_1.cydwr
Header Files
device.h
Source Files
main.c
Source
Components
Datasheets
Results
Start Page
TopDesign.cysch
main.c
Lab_1.cydwr
CY8C3866AXI-040
100-TQFP
Alias
Name
Port
Pin
Lock
\LCD_Char:LCDPort[6:0]\
P0[6:0] IDAC:H
P0[7:1] IDAC:H
P2[6:0]
P2[7:1]
P3[6:0] OpAmp:
P3[7:1] OpAmp:
P4[6:0]
P4[7:1]
P5[6:0]
LCD_Char_LCDPort_6 - Digital
LCD_Char_LCDPort_5 - Digital
LCD_Char_LCDPort_4 - Digital
Pins
Analog
Clocks
Interrupts
DMA
System
Directives
Flash Security
Notice List
0 Errors
0 Warnings
De...
File
Error L
Output
Show output from: All
Log file for this session is located at: C:\Documents and Settings\Admin.MICROSOF-7D0472\Local Se
Ready
0 Errors 0 Warnings 0 Notes
Новости Украины | ...
Do_Present_1.doc - ...
Lab_1 - PSoC Creator...
EN
19:33

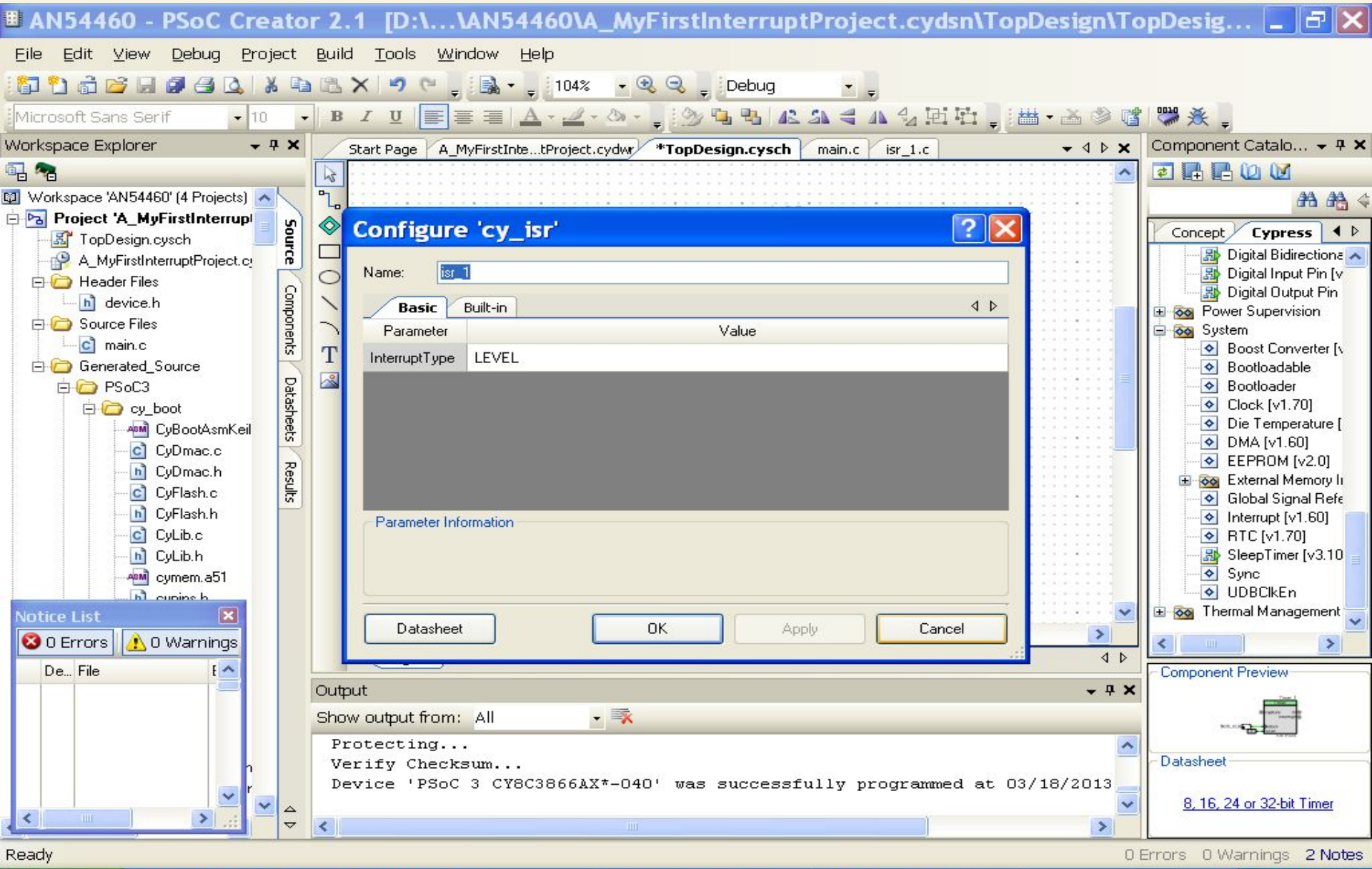
Lab_4 Interrupts



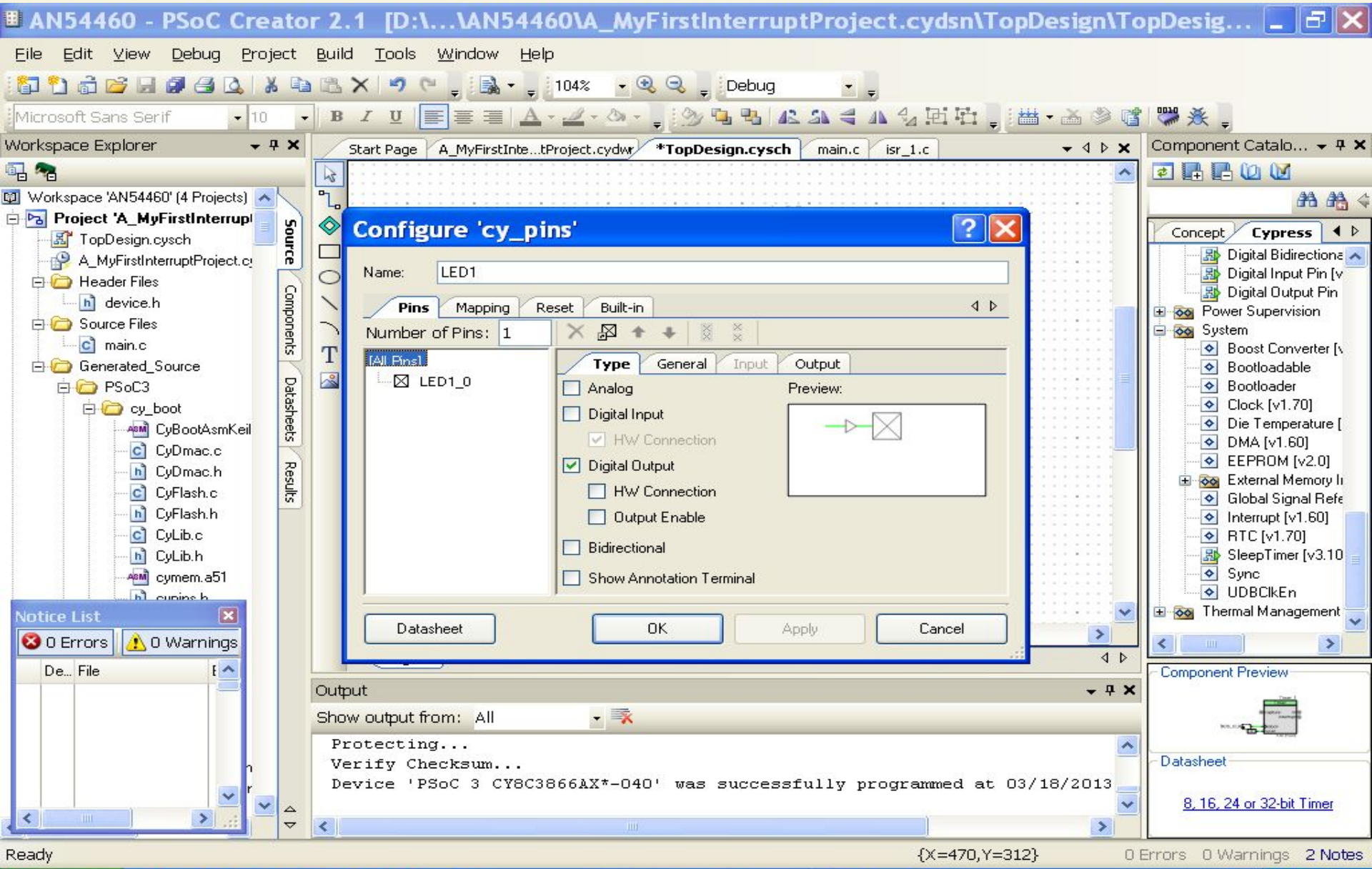
Lab_4 Interrupts



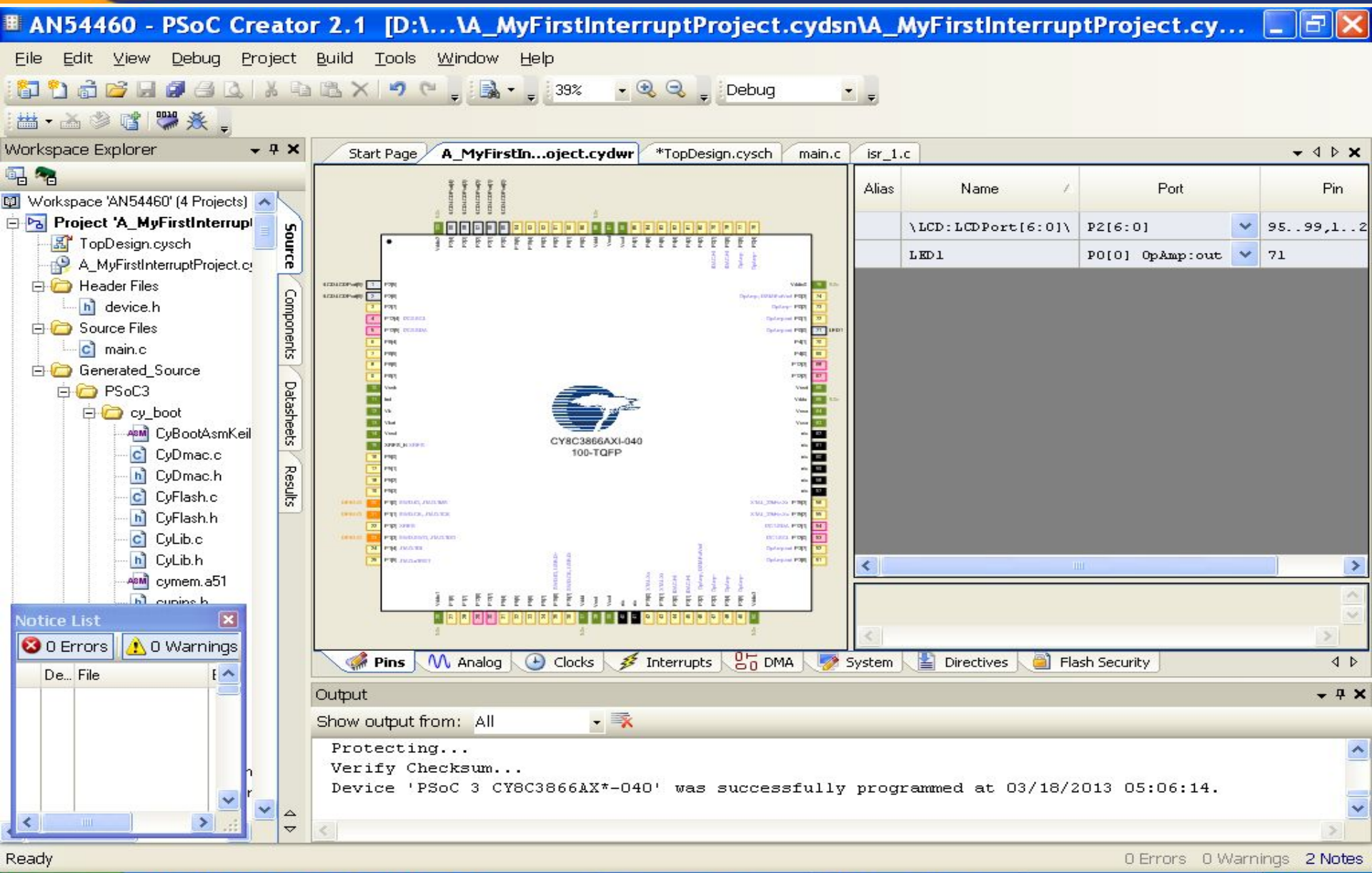
Lab_4 Interrupts



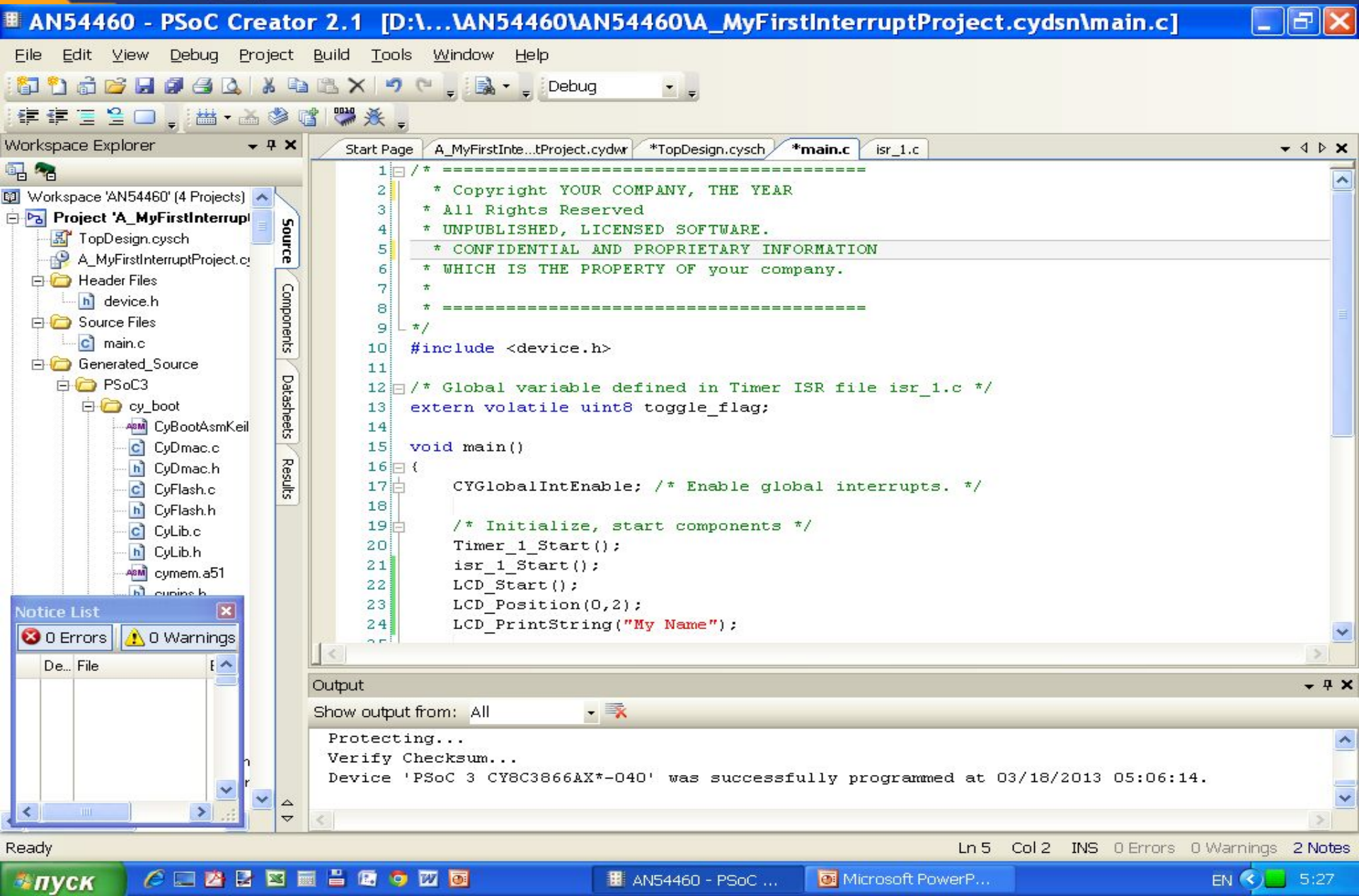
Lab_4 Interrupts



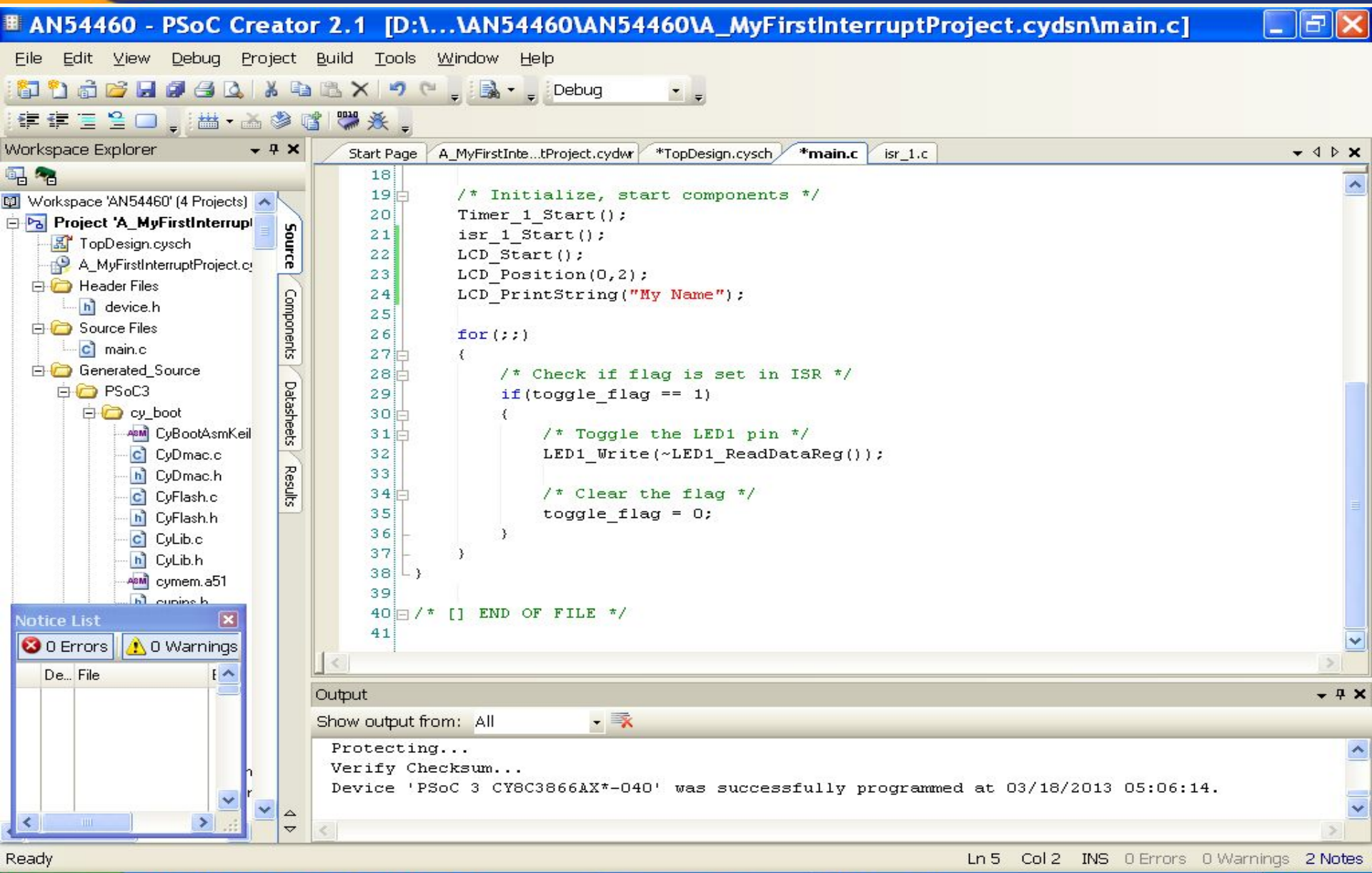
Lab_4 Interrupts



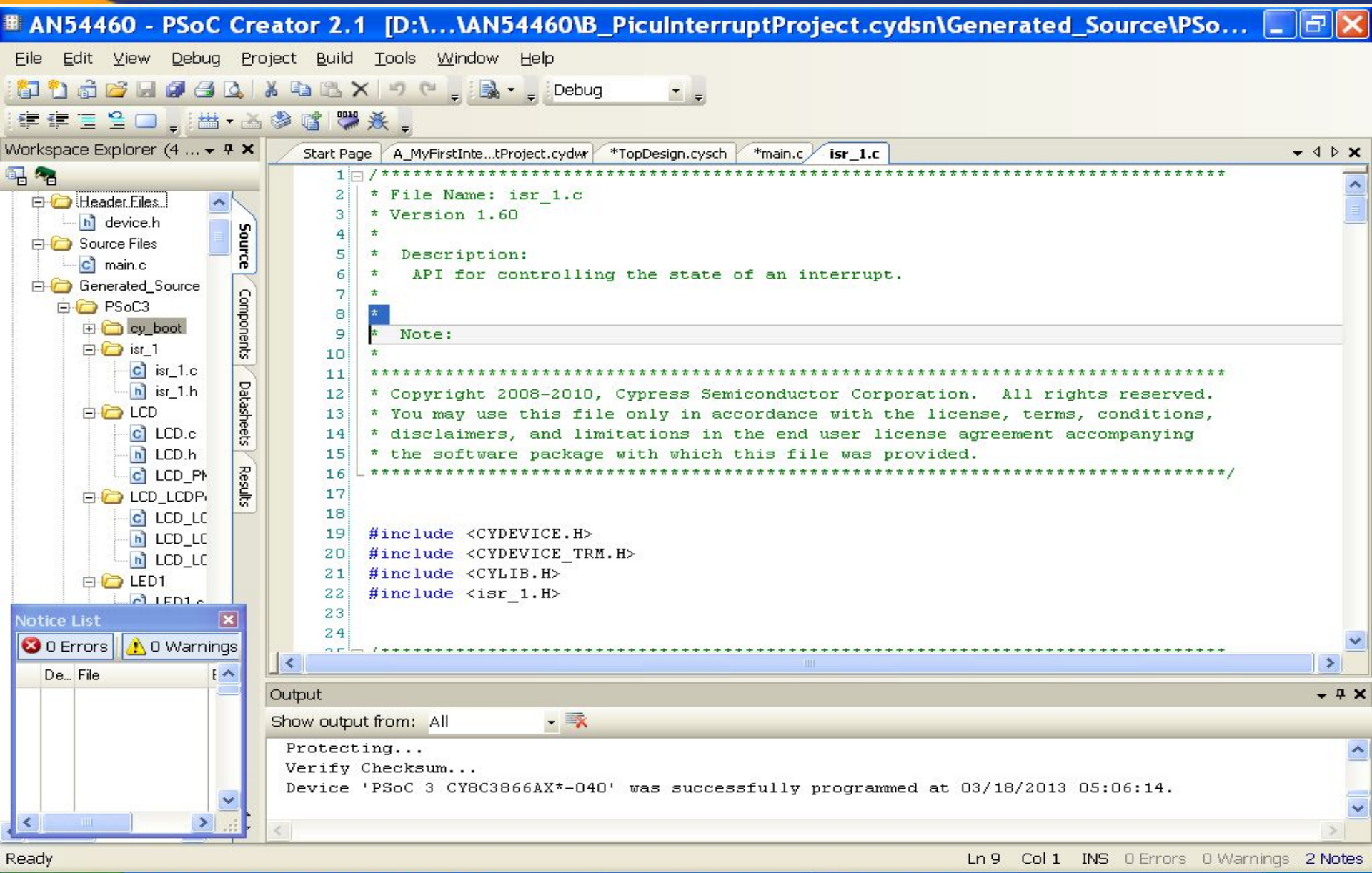
Lab_4 Interrupts



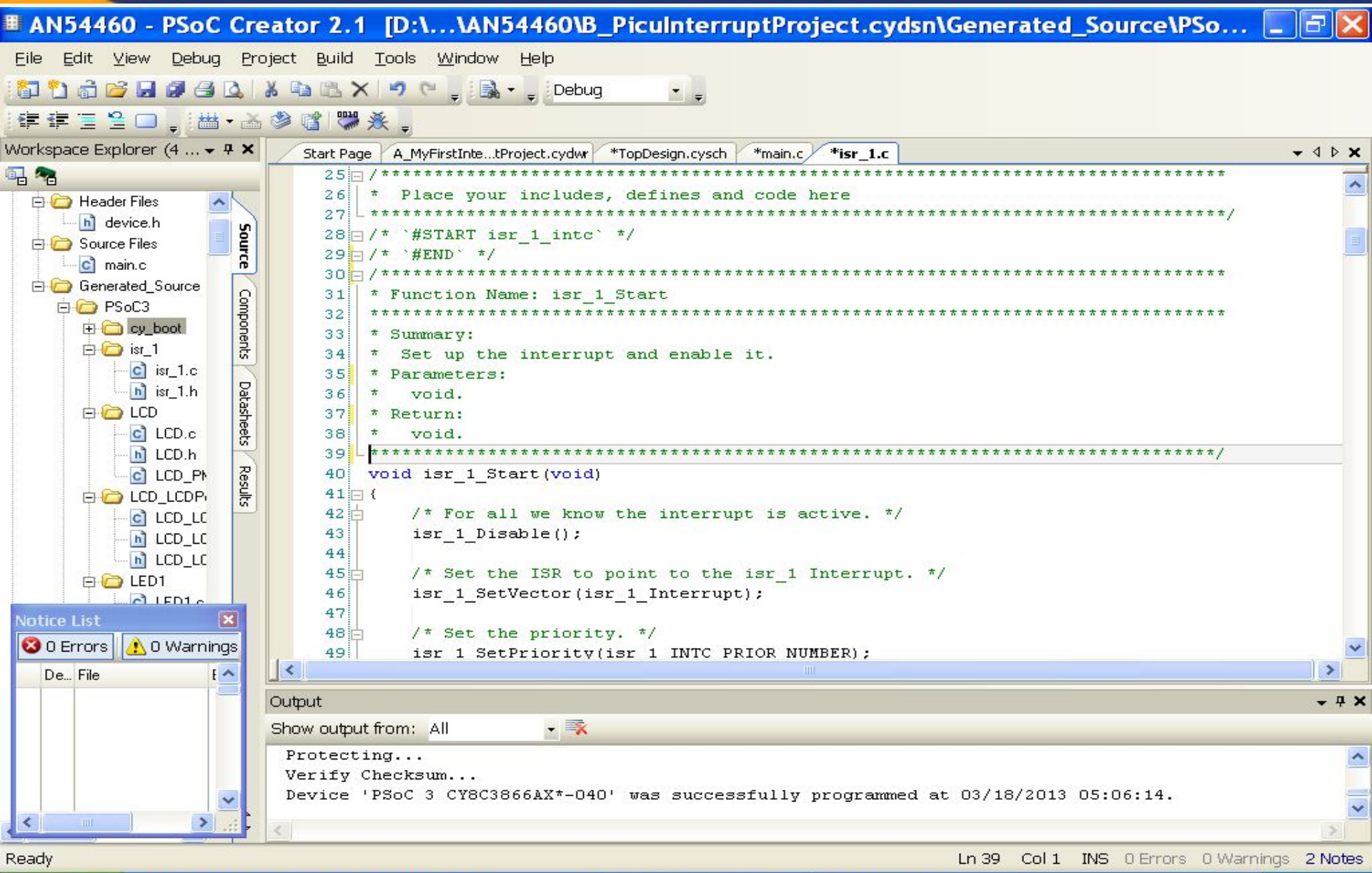
Lab_4 Interrupts



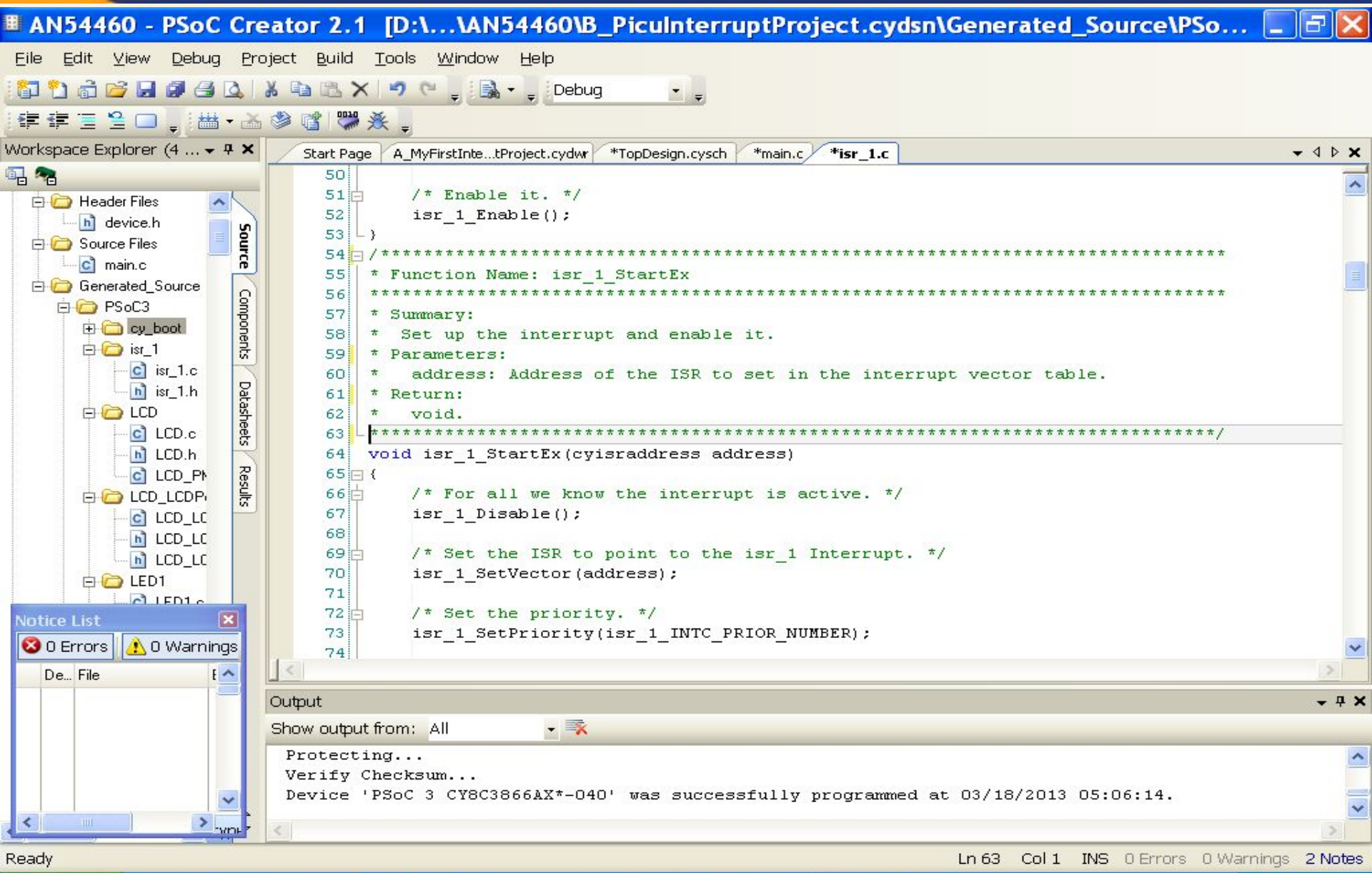
Lab_4 Interrupts



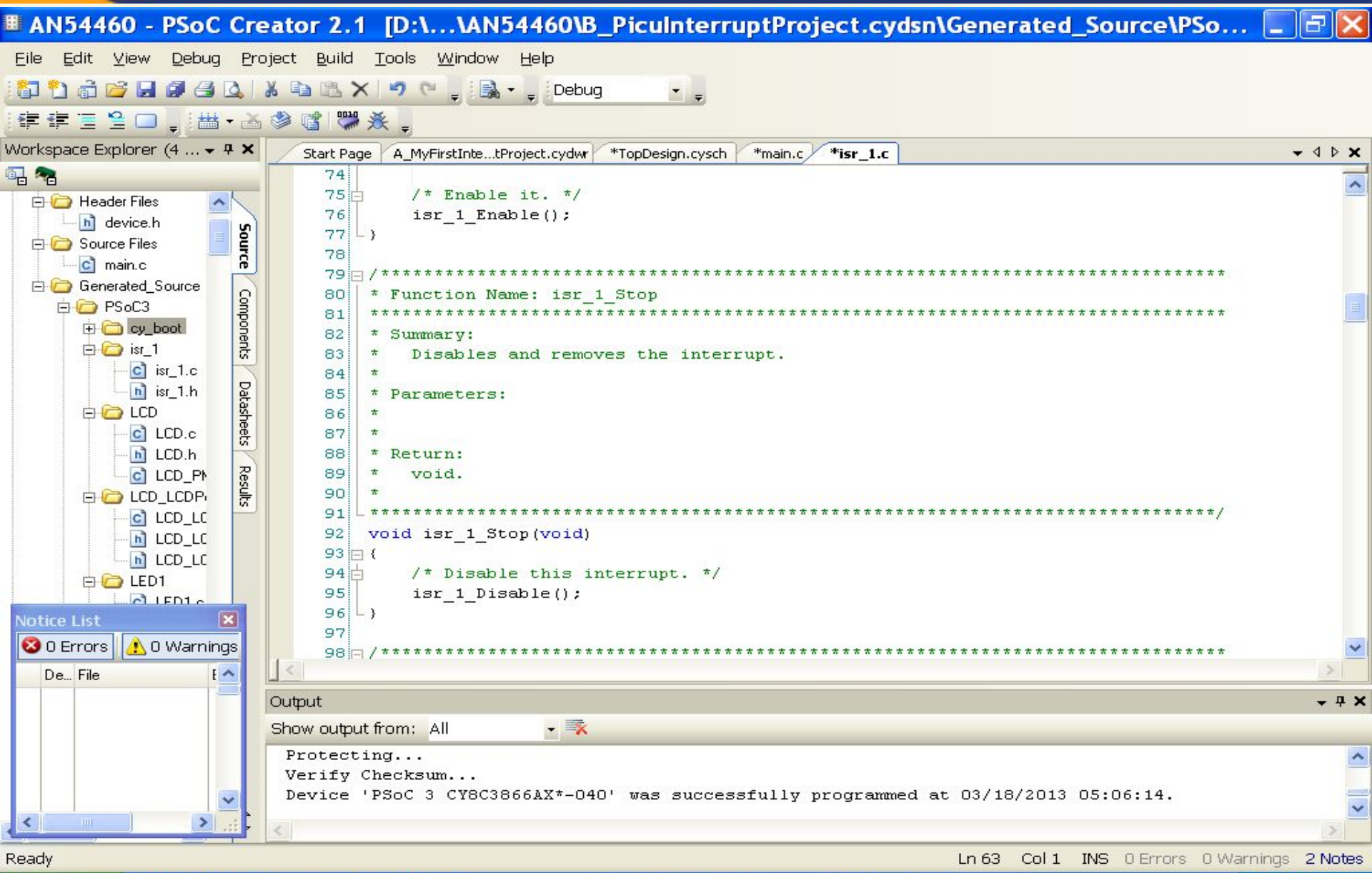
Lab_4 Interrupts



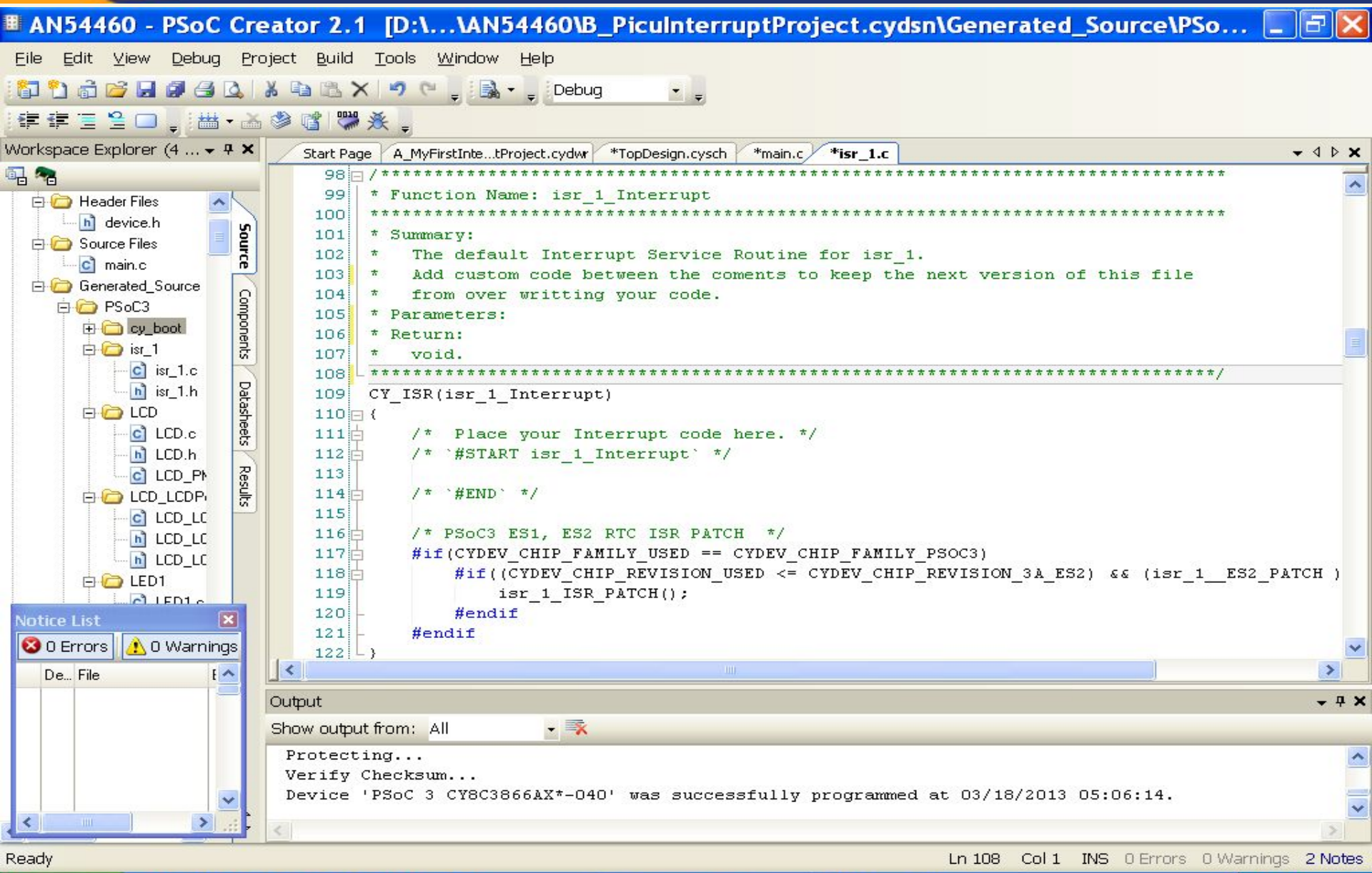
Lab_4 Interrupts



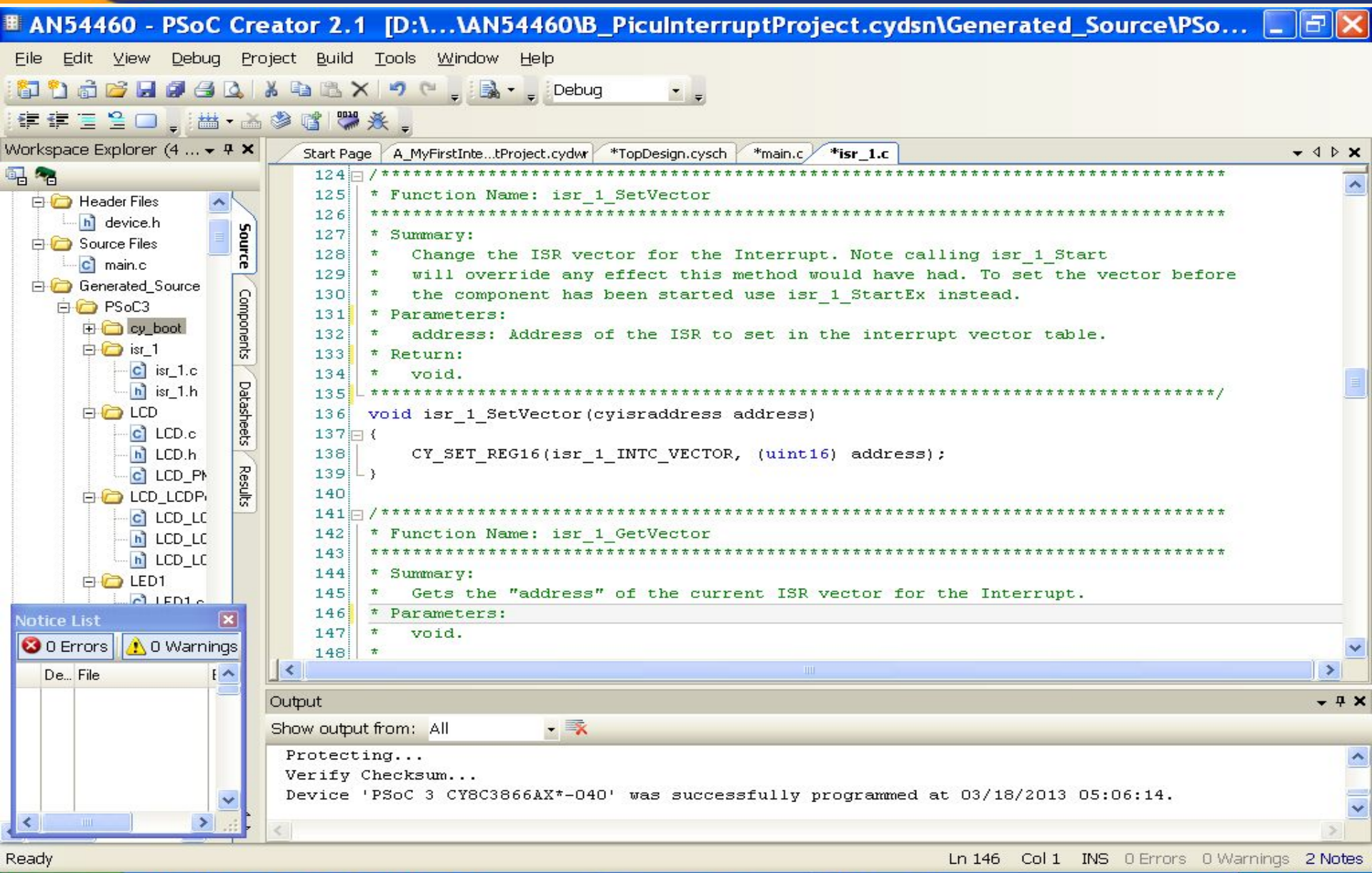
Lab_4 Interrupts



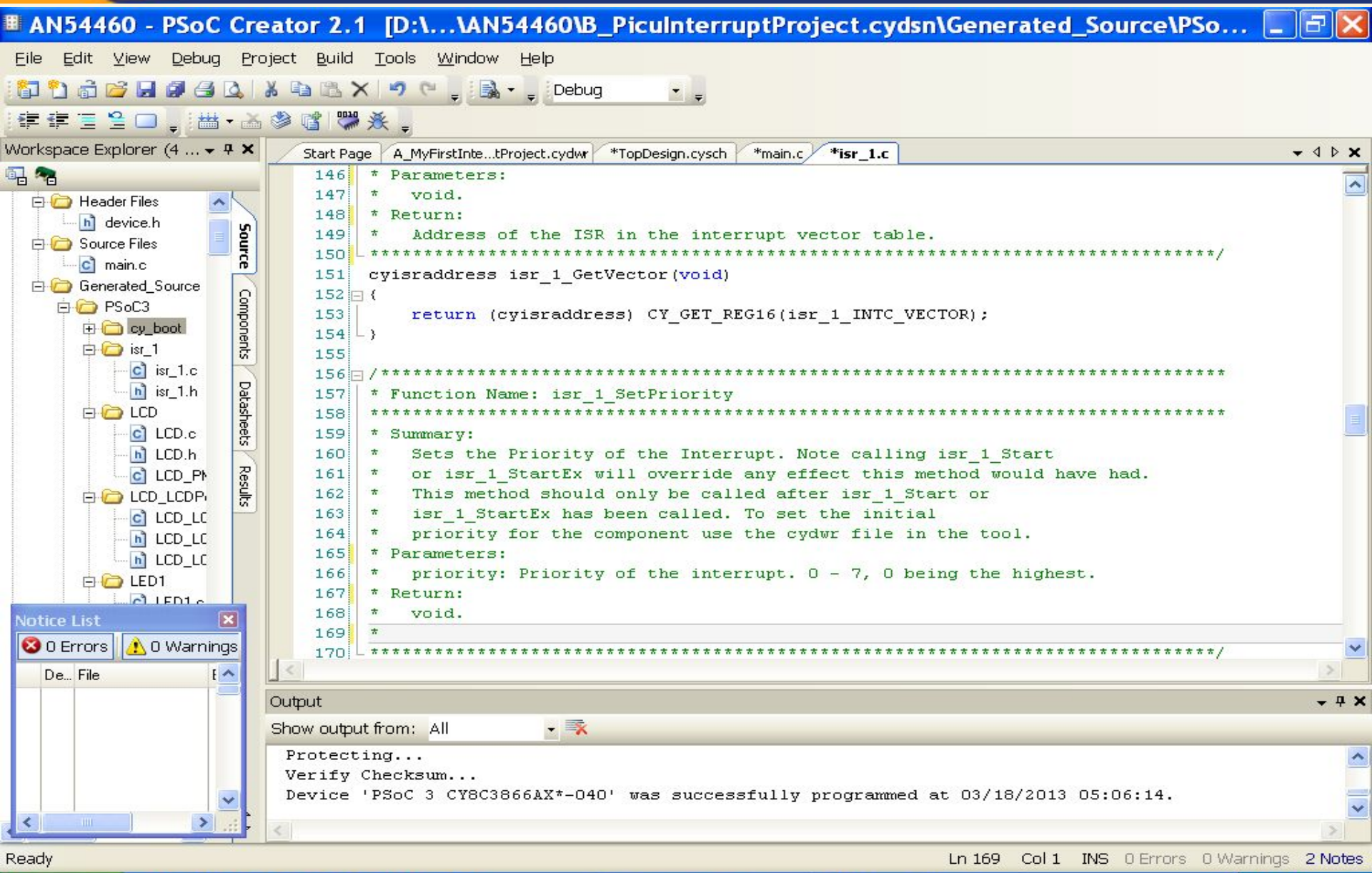
Lab_4 Interrupts



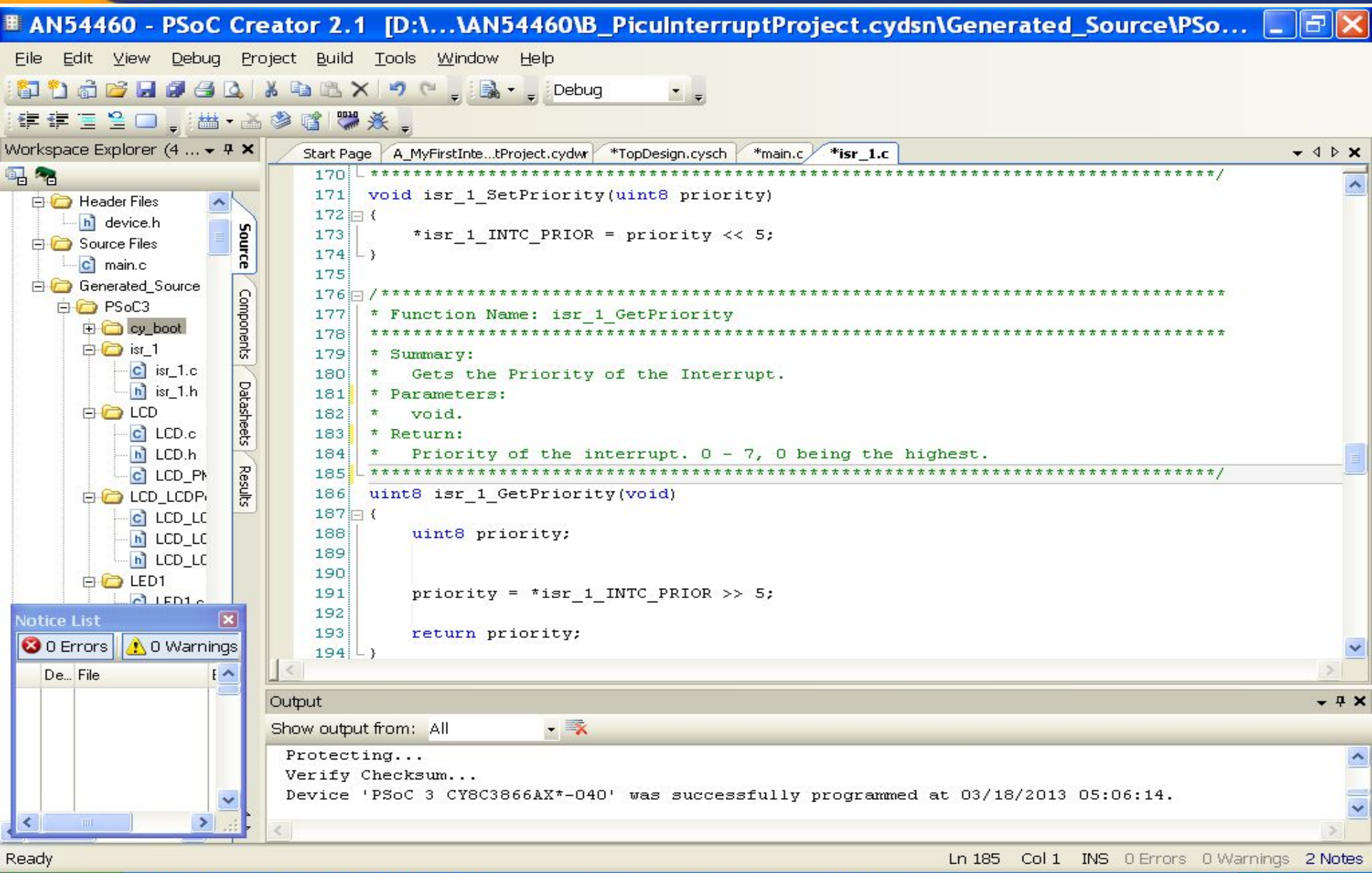
Lab_4 Interrupts



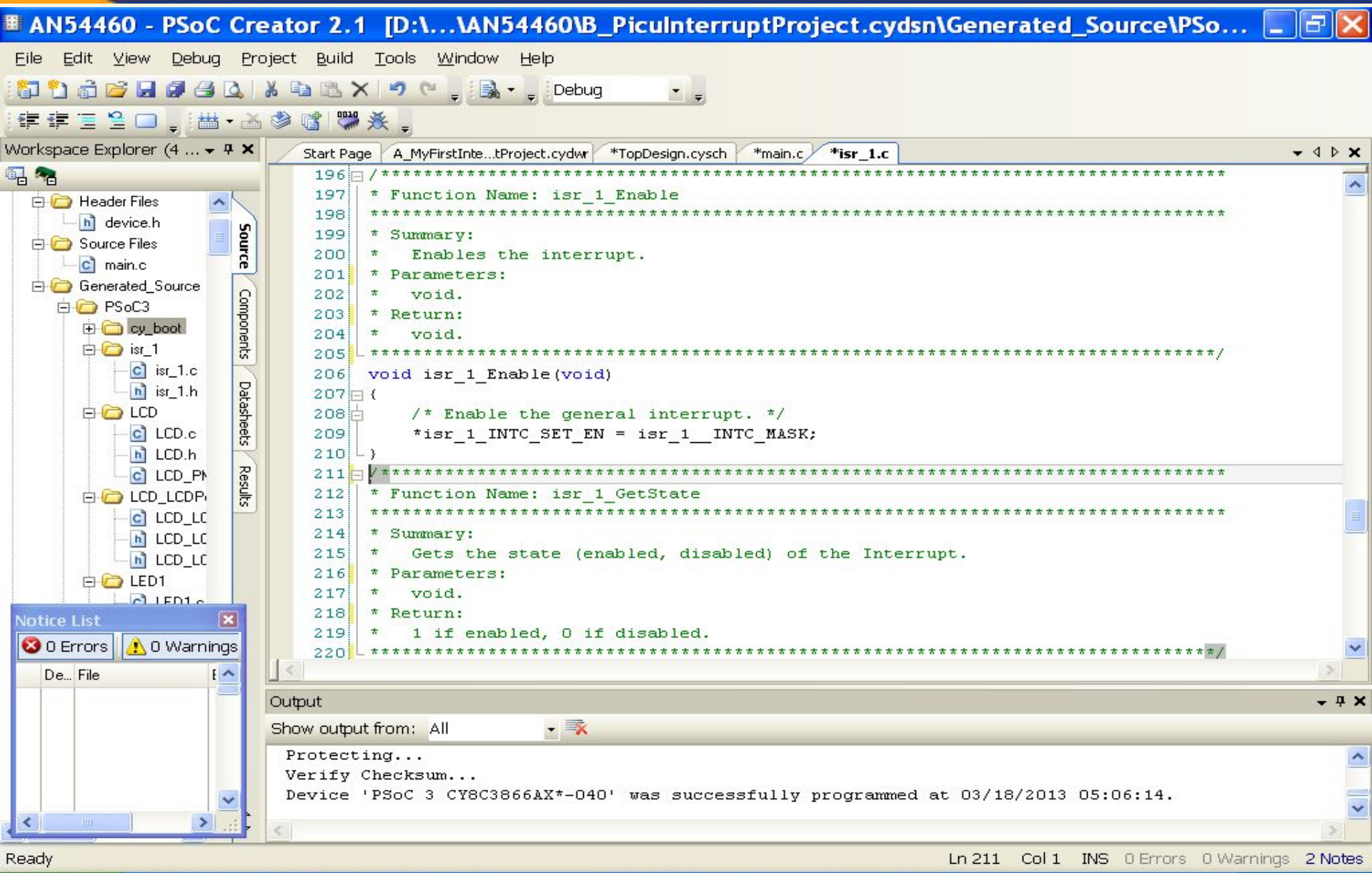
Lab_4 Interrupts



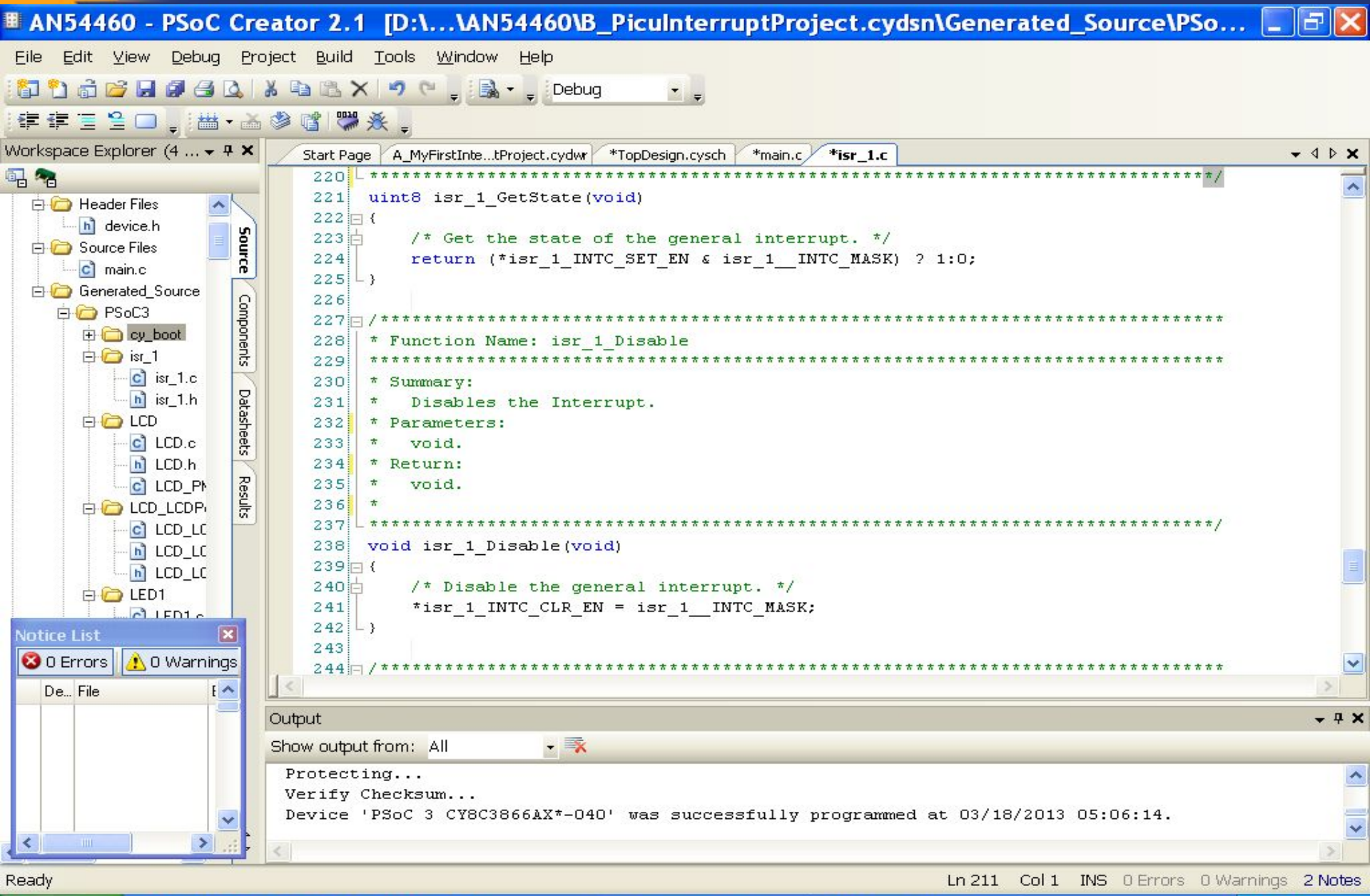
Lab_4 Interrupts



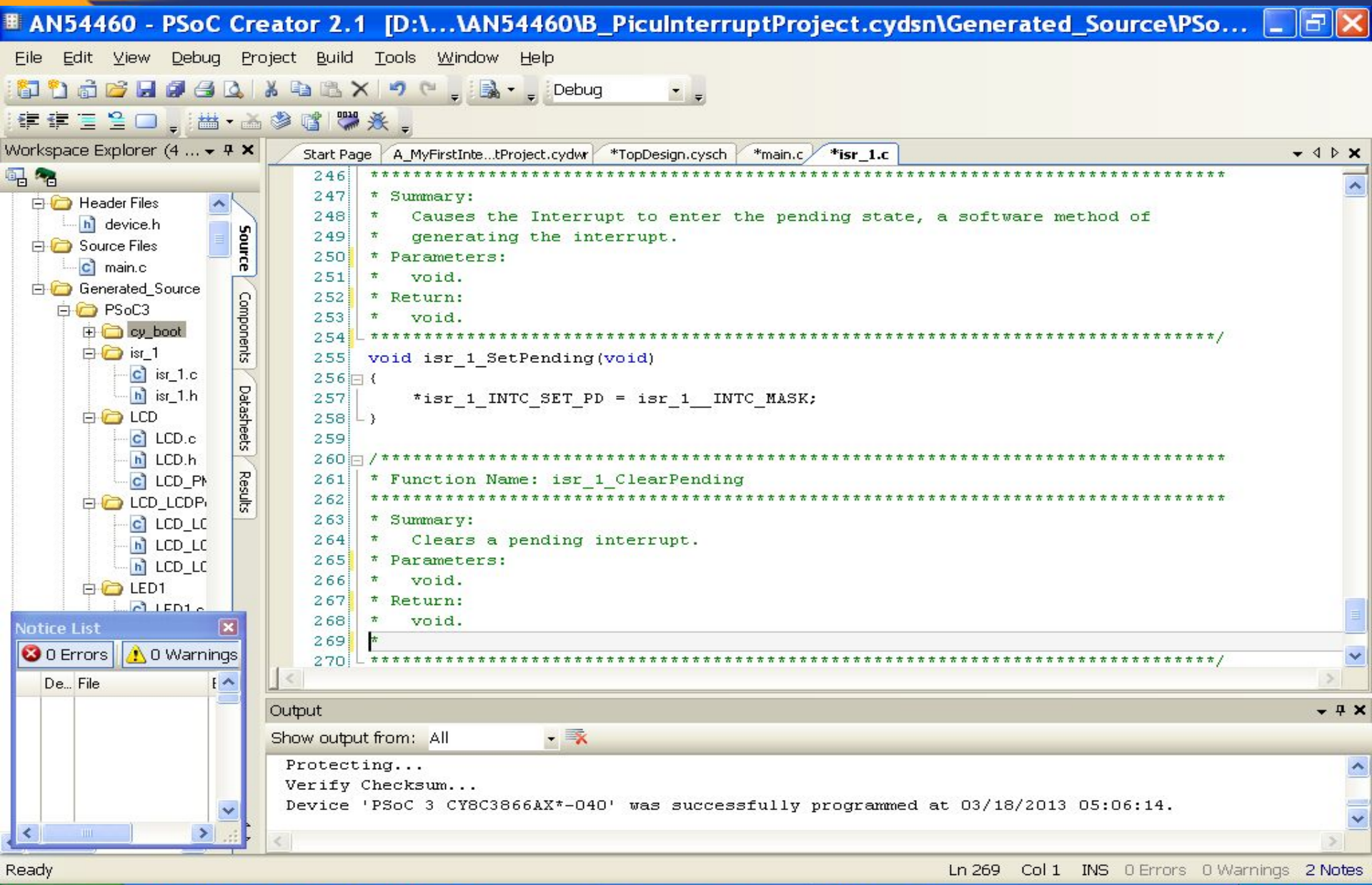
Lab_4 Interrupts

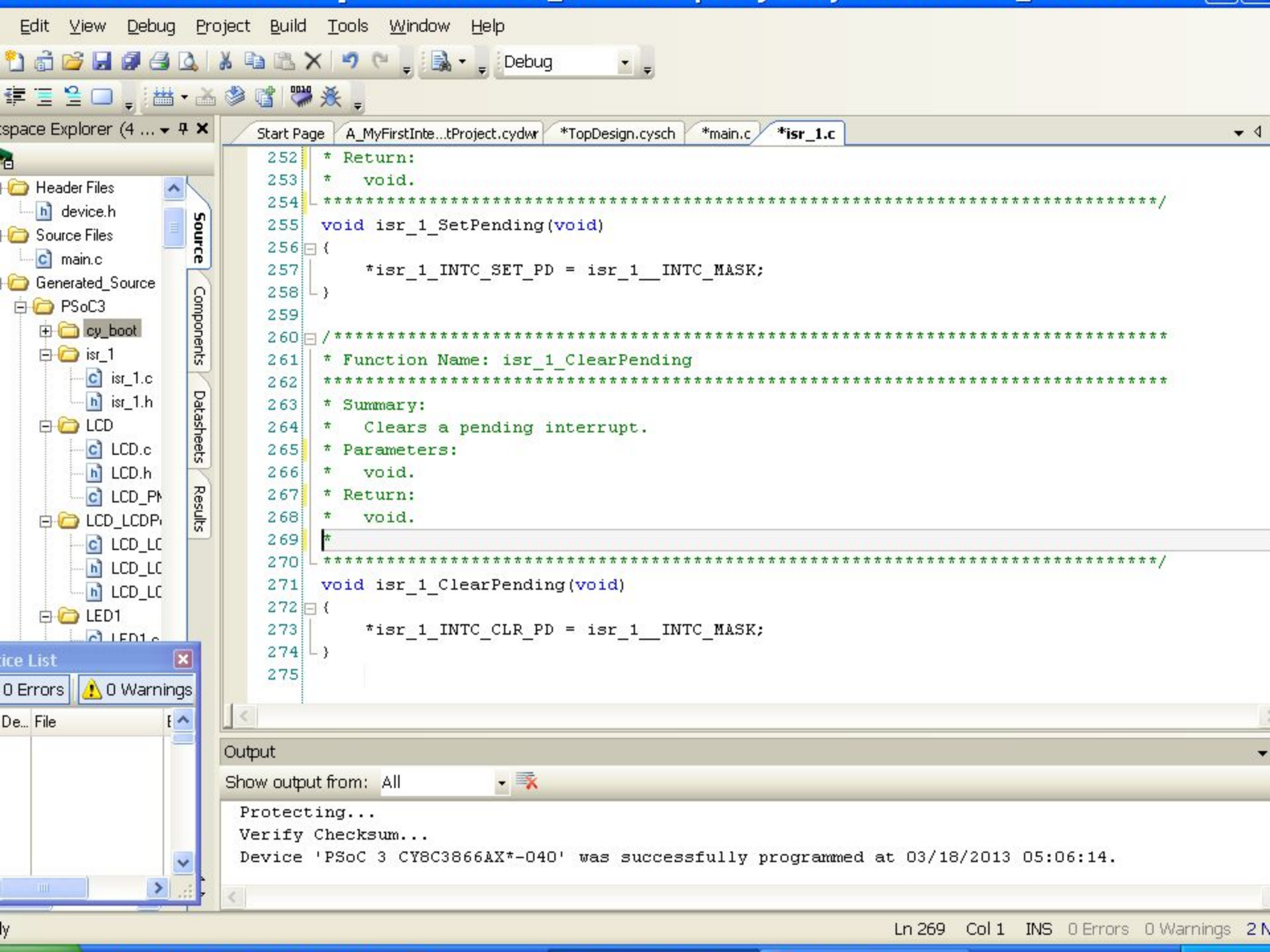


Lab_4 Interrupts



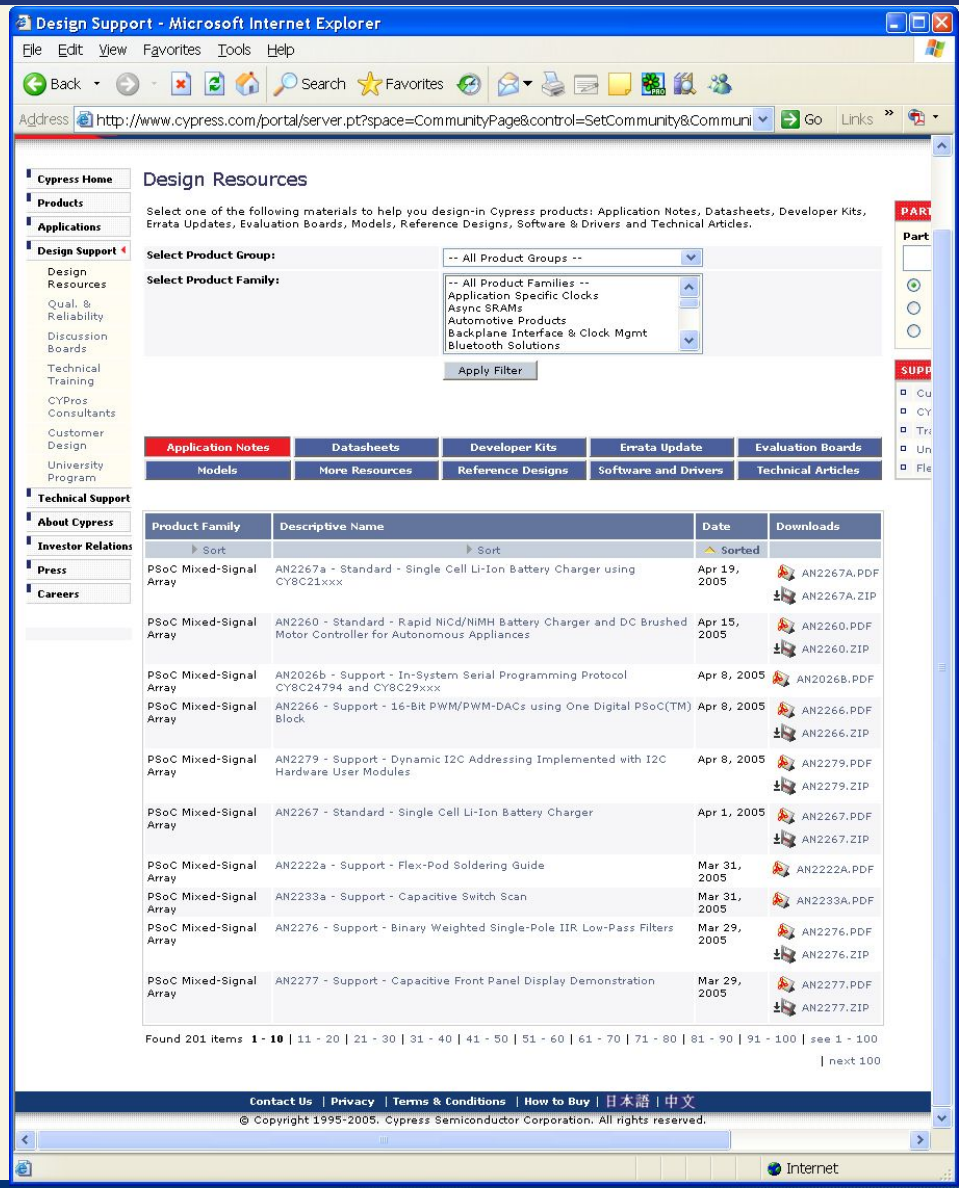
Lab_4 Interrupts




Edit View Debug Project Build Tools Window Help
Debug
Start Page
A_MyFirstInte...tProject.cydwr
*TopDesign.cysch
*main.c
*isr_1.c
Header Files
device.h
Source Files
main.c
Generated_Source
PSoC3
cy_boot
isr_1
isr_1.c
isr_1.h
LCD
LCD.c
LCD.h
LED1
Source
Components
Datasheets
Results
252 * Return:
253 * void.
254 ***/
255 void isr_1_SetPending(void)
256 {
257 *isr_1_INTC_SET_PD = isr_1__INTC_MASK;
258 }
259
260 /***
261 * Function Name: isr_1_ClearPending
262 **
263 * Summary:
264 * Clears a pending interrupt.
265 * Parameters:
266 * void.
267 * Return:
268 * void.
269 *
270 ***/
271 void isr_1_ClearPending(void)
272 {
273 *isr_1_INTC_CLR_PD = isr_1__INTC_MASK;
274 }
275
0 Errors
0 Warnings
De... File
Output
Show output from: All
Protecting...
Verify Checksum...
Device 'PSoC 3 CY8C3866AX*-040' was successfully programmed at 03/18/2013 05:06:14.
Ln 269 Col 1 INS 0 Errors 0 Warnings

Приклади застосування МК PSOC

На сайті фірми Cypress знаходиться більше 200 Application Notes і Reference Designs, які ілюструють області застосування мікроконтролерів PSoC.



Мікропроцесорна техніка

(лекція 4, кінець)

Благітко Б.Я.

2019 р.