

# Технологии регистрации заряженных частиц, сбор и анализ данных детекторов в ФВЭ

Лекция 5

# VMM

- VMM – электроника для STGC и MICROMEGAS проекта NSW
- VMM - специализированная интегральная схема (ASIC)
- Размер 21X21 мм
- VMM разработано Brookhaven National Laboratory (BNL)
- Состоит из 64 каналов с конфигурируемыми параметрами
- Регистрирует как негативные, так и позитивные сигналы
- Выходные данные:
  - Амплитуда (PDO) и время (TDO)
  - Адрес первого сработавшего канала (ART)
  - Аналоговые сигналы амплитуды и времени (для настройки)
- Данные передаются по двум проводам:
  - Data 0
  - Data 1

# VMM3 pinout

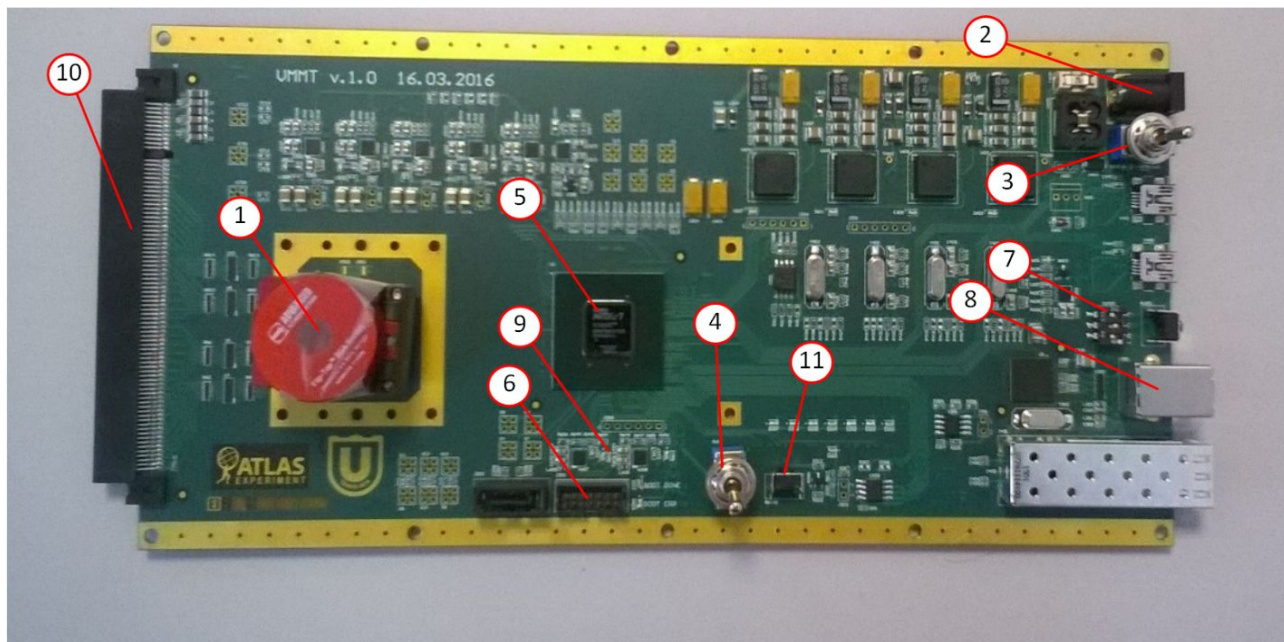
A	V <sub>ddk</sub>	V <sub>ddk</sub>	V <sub>ddk</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	trdb	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	V <sub>ddad</sub>	V <sub>ddad</sub>	V <sub>ddad</sub>	V <sub>ddad</sub>	+SETT -
B	V <sub>ddk</sub>	V <sub>ddk</sub>	V <sub>ddk</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	pdb	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>ssad</sub>	+TKD -	+CKTP -	SDI	SOC	CS	SOK	
C	i0	i1	i2	i3	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	rmo	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>ssad</sub>	+TKI -	+CKBC -	+ENA -	+CK6B -			
D	i4	i5	i6	i7	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>ssad</sub>	+CKIK -	+DTD -	+DTI -	+CKARF -			
E	i8	i9	i10	i11	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>ssad</sub>	+ART -	+CKDT -	+t0 -	+t1 -			
F	i12	i13	i14	i15	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>ssad</sub>	+t2 -	+t3 -	+t4 -	+t5 -			
G	i16	i17	i18	i19	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	+t6 -	+t7 -	+t8 -	+t9 -			
H	i20	i21	i22	i23	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	+t10 -	+t11 -	+t12 -	+t13 -	+t14 -		
J	i24	i25	i26	i27	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	+t15 -	+t16 -	+t17 -	+t18 -	+t19 -		
K	i28	i29	i30	i31	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	+t20 -	+t21 -	+t22 -	+t23 -	+t24 -		
L	i32	i33	i34	i35	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	+t25 -	+t26 -	+t27 -	+t28 -	+t29 -		
M	i36	i37	i38	i39	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	+t30 -	+t31 -	+t32 -	+t33 -	+t34 -		
N	i40	i41	i42	i43	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	+t35 -	+t36 -	+t37 -	+t38 -	+t39 -		
P	i44	i45	i46	i47	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	+t40 -	+t41 -	+t42 -	+t43 -			
R	i48	i49	i50	i51	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	+t44 -	+t45 -	+t46 -	+t47 -			
T	i52	i53	i54	i55	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	+t48 -	+t49 -	+t50 -	+t51 -			
U	i56	i57	i58	i59	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	+t52 -	+t53 -	+t54 -	+t55 -			
V	i60	i61	i62	i63	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	+t56 -	+t57 -	+t58 -	+t59 -			
W	V <sub>ddk</sub>	V <sub>ddk</sub>	V <sub>ddk</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	+t60 -	+t61 -	+t62 -	+t63 -			
Y	V <sub>ddk</sub>	V <sub>ddk</sub>	V <sub>ddk</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>dbi</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	V <sub>ssad</sub>	V <sub>ddad</sub>	V <sub>ddad</sub>	V <sub>ddad</sub>	V <sub>ddad</sub>	+SETB -

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
---	---	---	---	---	---	---	---	---	----	----	----	----	----	----	----	----	----	----	----

- V<sub>ddp</sub> preamp +1.2V
- V<sub>dd</sub> analog +1.2V
- V<sub>ss</sub> analog 0V
- V<sub>ddad</sub> ADC +1.2V
- V<sub>ssad</sub> ADC 0V
- V<sub>ddd</sub> digital +1.2V
- V<sub>ssd</sub> digital 0V
- analog in
- analog out
- digital SE IO
- + xxx - SLVS IO

# Тестирование чипов



- 1 - Сокет для установки микросхемы VMM3;
- 2 - Разъем подключения внешнего источника питания;
- 3 - Тумблер включения питания Тестера;
- 4 - Тумблер включения питания микросхемы VMM3;
- 5 - ПЛИС Artix-7;

- 6 - JTAG разъем;
- 7 - DIP переключатель режимов интерфейса USB 3.0;
- 8 - Разъем USB 3.0;
- 9 - Светодиоды;
- 10 - Разъем для подключения внешнего генератора тестовых сигналов;
- 11 - Кнопка FPGA Reset.

# Тестирование чипов. Приложение VMMT

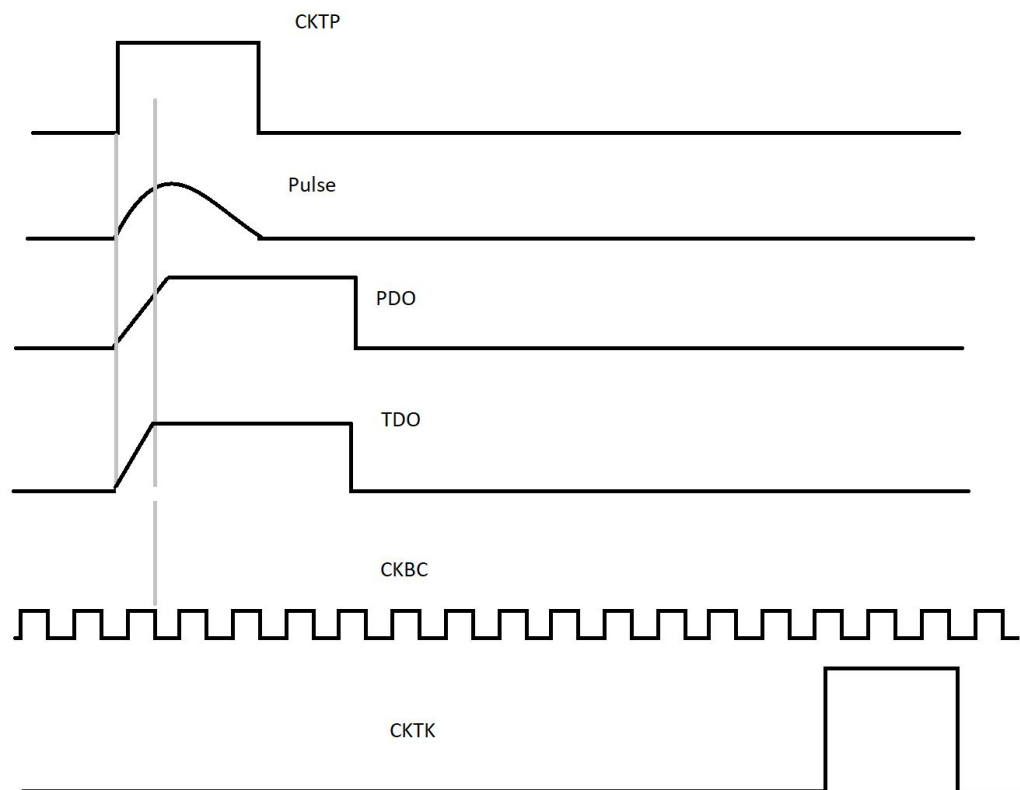
The screenshot displays the VMM3 Tester application interface, which is organized into several functional panels:

- File**: A menu bar at the top left.
- VMM Configuration**: The main configuration area, divided into:
  - Global Parameters**: Includes checkboxes for Positive Input Charge Polarity (spp), Disable-at-Peak (sdp), Route Analog Monitor to PDO Output (sbmx), Analog Output Buffers (pdo, tdo, mo), Leakage Current Disable (slg), Monitor Multiplexing (scmx), ART enable (sfa), Peaking Time (200 ns), Doubles the Leakage Current (sfn), Gain (0.5 mV/fC), Neighbor Triggering Enable (sng), Timing Outputs Control (stpp, stot), Timing Output (sttt), TAC Slope Adjustment (60), Coarse Threshold DAC (0), Internal Pulser DAC (0), 10-bit ADC conversion time (1), 8-bit ADC conversion time (1), and 6-bit ADC conversion time (1).
  - Channel Parameters**: Includes Ch. No. (0), Positive Polarity (sp), Large Sensor Capacitance Mode (sc), Leakage Current Disable (sl), 1.2pF test capacitor enable (st), Multiple test capacitor by 10 (sth), Mask Enable (sm), Trim Threshold DAC (0 mV), Channel Monitor Mode (smx), 10-bit ADC zero (1), 8-bit ADC zero (1), and 6-bit ADC zero (1).
  - ADCs Enable**: A checkbox for enabling ADCs (checked).
  - Terminator Settings**: A list of checkboxes for various terminators such as s32, stlc, srec, sbip, srat, sfrst, slvsbc, slvstp, slvstk, slvsdt, slvsart, slvstki, slvsena, slvs6b, sl0enaV, reset, and sl0ena.
  - Offset and Window Settings**: Includes L0 BC offset (1), Ch. taggig BC offset (1), Ch. taggig BC rollover (0), Trigger window size (100), Max hits per L0 (0), and L0 triggers ovf. skip (1).
  - Advanced Settings**: Includes checkboxes for sL0cktest, sL0ckinv, sL0dckinv, and nskipm\_i.
  - Serial Data and ART Settings**: Includes checkboxes for sdcks, sdcka, sdck6b, sdrv, ssh, and slvs, along with their corresponding descriptions like "enables 6-bit ADC (sttt en)", "8-bit ADC conversion mode", "Enable hi res ADC (8/10 bit)", "Enable auto-reset", and "ART flag synchronization".
- Channel Parameters**: A separate panel for configuring individual channels, including Ch. No. (0), Positive Polarity (sp), Large Sensor Capacitance Mode (sc), Leakage Current Disable (sl), 1.2pF test capacitor enable (st), Multiple test capacitor by 10 (sth), Mask Enable (sm), Trim Threshold DAC (0 mV), Channel Monitor Mode (smx), 10-bit ADC zero (1), 8-bit ADC zero (1), and 6-bit ADC zero (1). It features a "Set for All Channels" button.
- VMM3 ID**: A panel for setting the VMM3 ID (000001) and an "Auto" checkbox. It includes "Probe", "Slow Configure", and "Fast Configure" buttons.
- Gross Full Test**: Includes a "Full Test #3 (All Channels)" button, "Bunch mode" and "Log to file" checkboxes, and a "Path to Settings" button.
- Tester Status**: Displays the status "VMM Tester Board is ready. FPGA version b7053012".
- FPGA USB 3.0 Register i/o**: A panel for reading and writing registers, including fields for Address (hex) and Data (hex), and "Read" and "Write" buttons.
- Test Pulse Generator**: A panel for generating test pulses, including fields for Width (us) (0.2), Period (us) (500.0), and Burst size (0), and a "40" field for ckc, MHz.

EXIT

# Режимы работы VMM

## Continuous mode



# Режимы работы VMM

Continuous mode

8b-10b кодирование

hit data	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
	F	N	Chan# (6)						ADC (10)										TDC (8)								BCID (12)											

Побитовая передача данных по проводам data0 и data1

```

***** VMM3 Test Log *****
2017.06.27 16:13:16.875
FPGA version b7052602
Configuration file: ADC130_T230_PT200_G3.cfg
*****

```

```

VMM3 ID#          10338

Test pulse width   0.000 us
Test pulse period  500.008 us
Number of pulses   300
ckbc               0.000 Hz

```

Peaking Time (st) 200 ns

Gain (sg) 3.0 mV//fc

TAC Slope (stc) 60

Coarse Threshold DAC (sdt) 230

Internal Pulser DAC (sdp) 130

\*\*\*\*\*

## Пример лог-файла

1 – если событие  
 есть, 0 – если сработал сам канал,  
 Адрес канала  
 Амплитуда импульса  
 Время прихода импульса

F	T	Addr	Ampl	Time	Grey	Check	ARTSample	Event
1	1	07	0	0	0	[ 0 ] 50	0	1
1	0	08	0	0	0	[ 1 ]	1	
1	1	09	0	0	0	[ 2 ]	2	
1	1	10	0	0	0	[ 3 ]	3	
1	1	00	147	0	2	[ 64 ] 9	64	5
1	1	01	146	0	2	[ 65 ]	65	
1	1	02	141	0	2	[ 66 ]	66	
1	1	03	144	0	2	[ 67 ]	67	
1	1	04	128	0	2	[ 68 ]	68	
1	1	05	167	0	2	[ 69 ]	69	
1	1	06	152	0	2	[ 70 ]	70	
1	1	07	124	232	2	[ 71 ]	71	
1	1	08	113	232	2	[ 72 ]	72	
1	1	09	137	241	2	[ 73 ]	73	
1	1	10	178	255	2	[ 74 ]	74	
1	1	11	144	232	2	[ 75 ]	75	
1	1	12	152	0	2	[ 76 ]	76	
1	1	13	131	0	2	[ 77 ]	77	

Номер импульса

ART

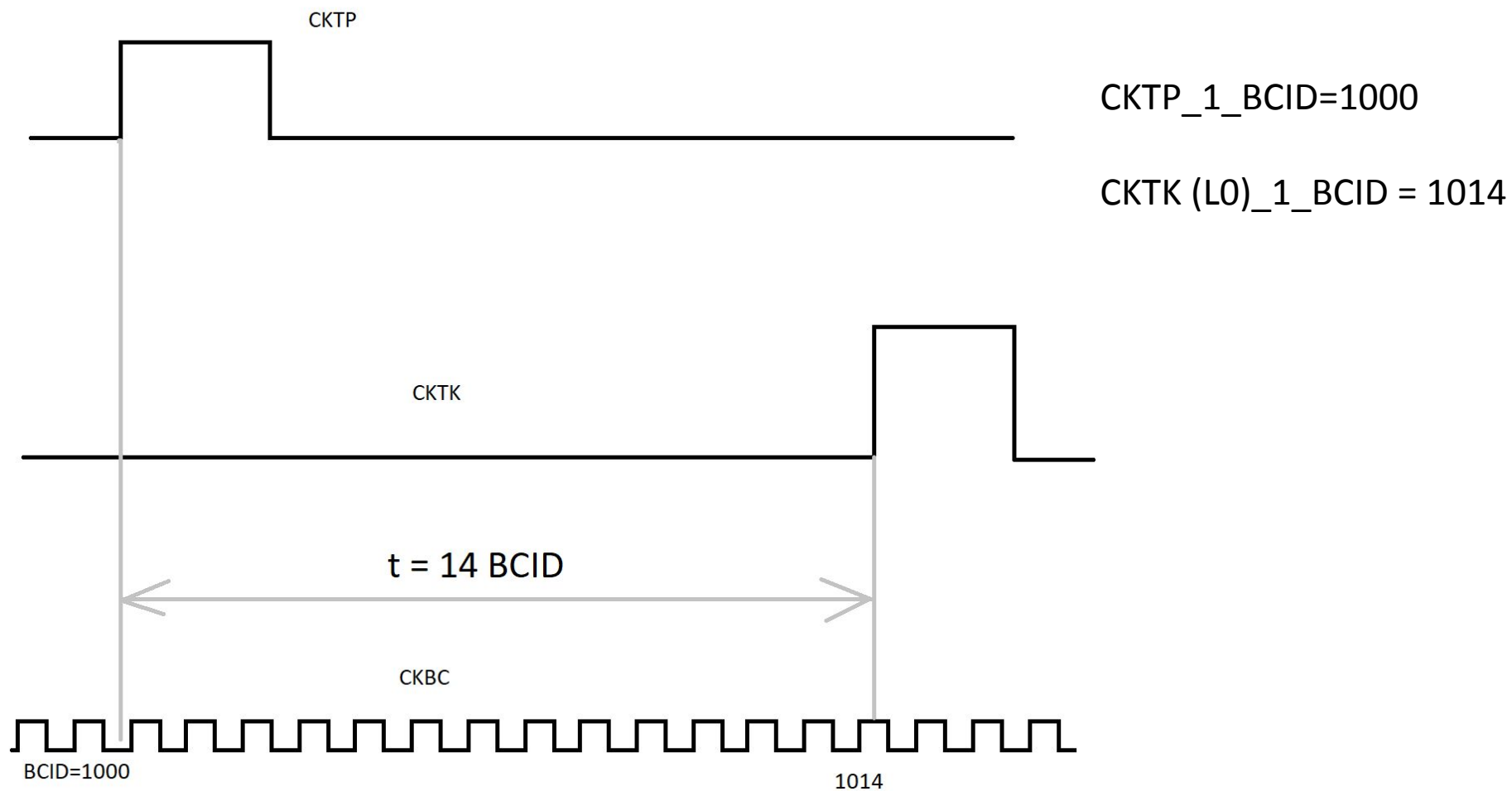


# Мониторирование сигналов с платы

Вывод на плате	Сигнал
X18	Test pulse
X7	CKBC
X14	CKDT
X15	Data0
X16	Data1
X17	CKTK
X700	MO
X701	PDO
X702	TDO

# Режимы работы VMM

L0-mode



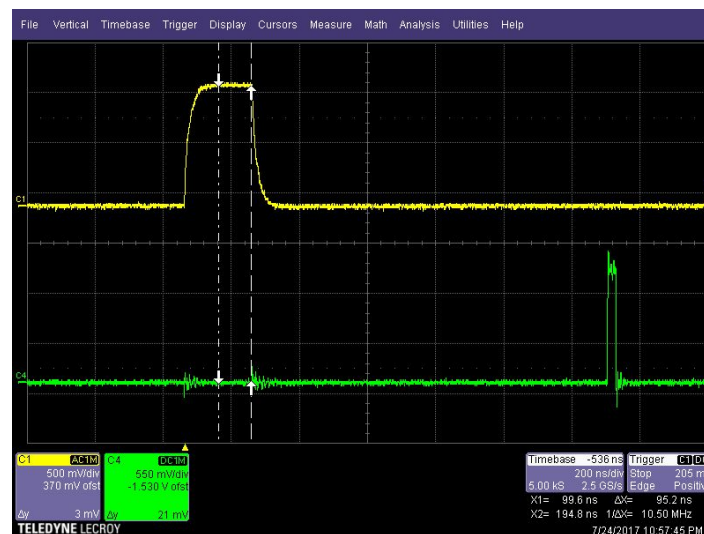
# Режимы работы VMM

L0-mode

CKTP\_1\_BCID=1000

CKTK (L0)\_1\_BCID = 1014

t = 14



The figure is a screenshot of the VMM3 configuration software interface. It features several input fields and checkboxes. On the left side, there are fields for 'L0 BC offset' (4081), 'Ch. taggig BC offset' (0), 'Ch. taggig BC rollover' (4095), 'Trigger window size' (7), 'Max hits per L0' (63), and 'L0 triggers ovf. skip' (0). Below these are checkboxes for 'sL0cktest', 'sL0ckinv', 'sL0ddckinv', and 'nskip |'. At the bottom left, the 'L0 pos' field is set to 14 and is highlighted with a red rectangle. In the center, the 'VMM3 ID' is set to 000001, with an 'Auto' checkbox. To the right of this are buttons for 'Probe', 'Slow Configure', and 'Fast Configure'. Below these is the 'Gross Full Test' section, which includes a 'Full Test #3 (All Channels)' button, 'Bunch mode' and 'Log to file' checkboxes, and a 'Path to Settings' button. At the bottom, the 'Tester Status' section displays the message 'VMM Tester Board is ready. FPGA version b7062302'. An 'EXIT' button is located at the bottom right.

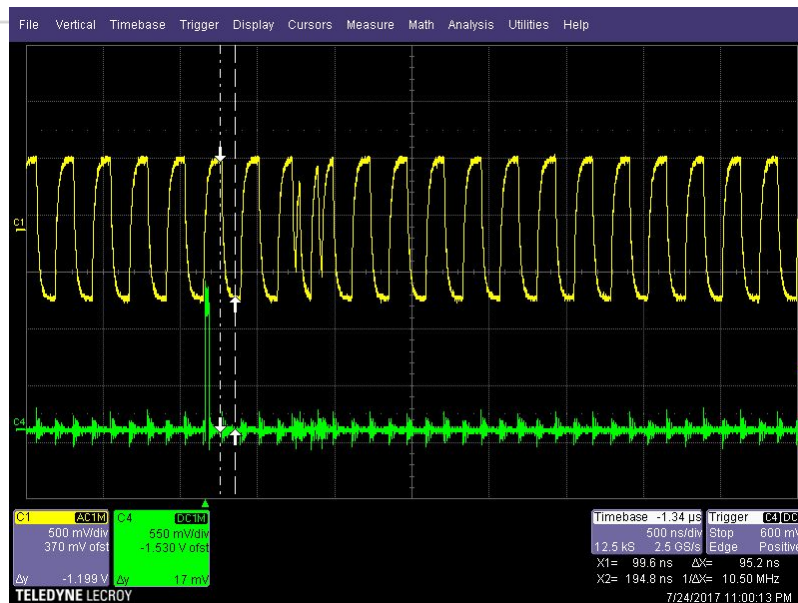
# Режимы работы VMM

L0-mode

- 8b-10b кодирование

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
header	V	P	orb		BCID (12)												1st word after comma															
hit data	1	P	R	T	Chan# (6)						ADC (10)						TDC (8)						N	rel BCID								

LL\_format\_VMM3out\_V04



# Виды Тестов

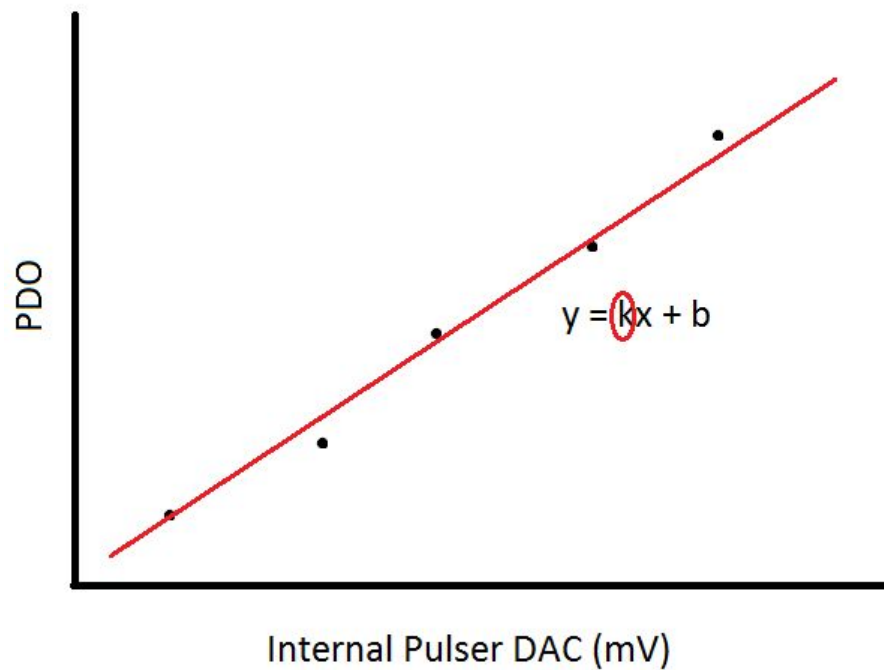
## Калибровка По амплитуде

1. Набрать сигналы с разными значениями DAC
2. Обработать и определить средние значения PDO для каждого канала, для каждого значения DAC



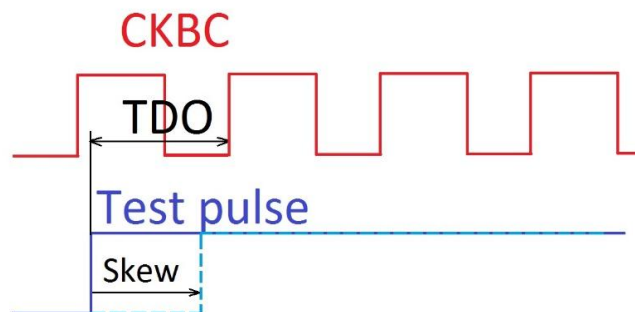
# Виды Тестов

- Калибровка
  - По амплитуде



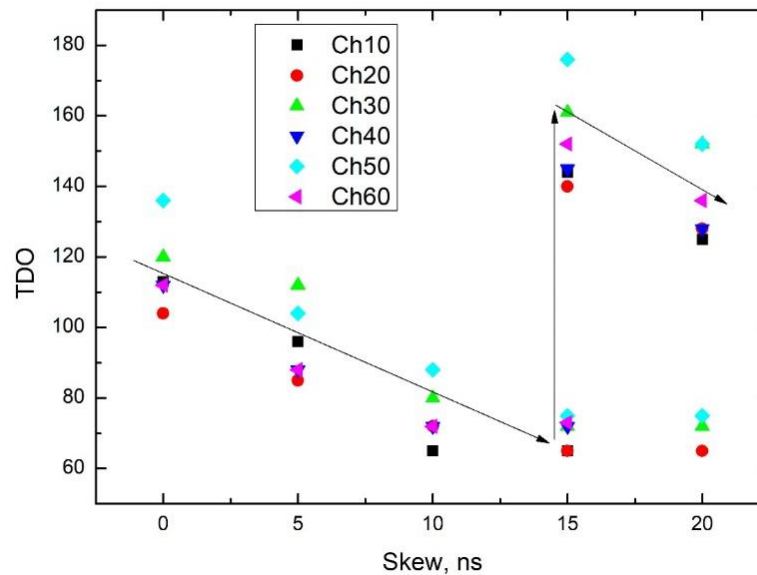
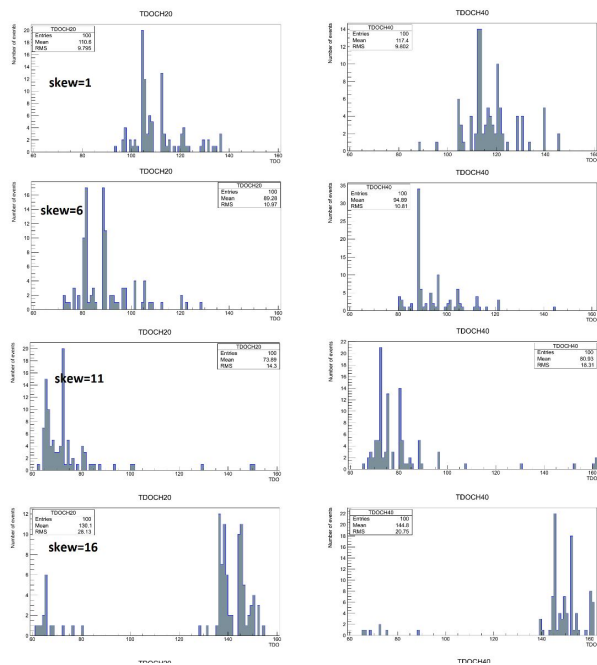
# Виды Тестов

- Калибровка
  - По времени



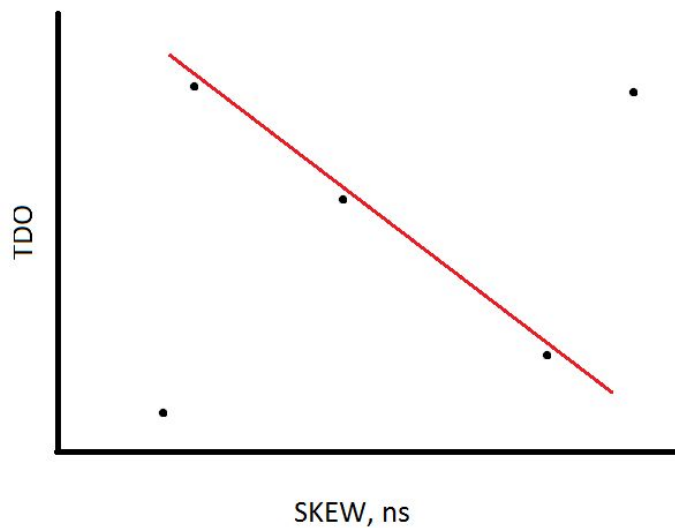
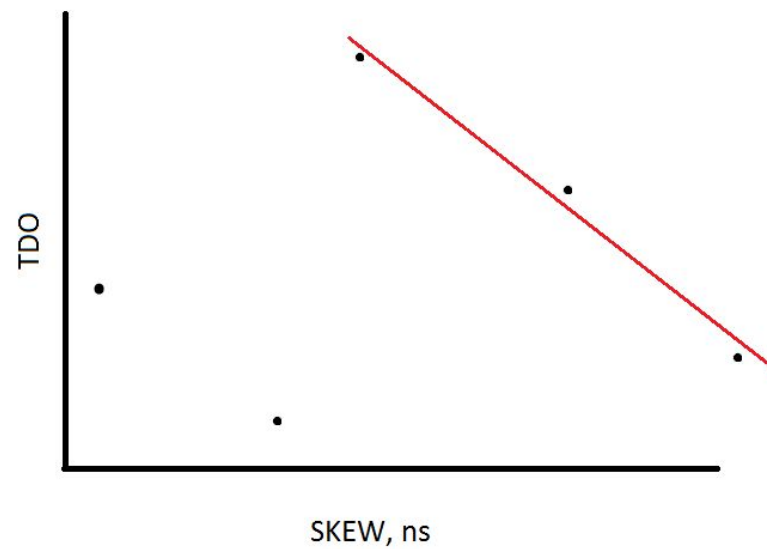
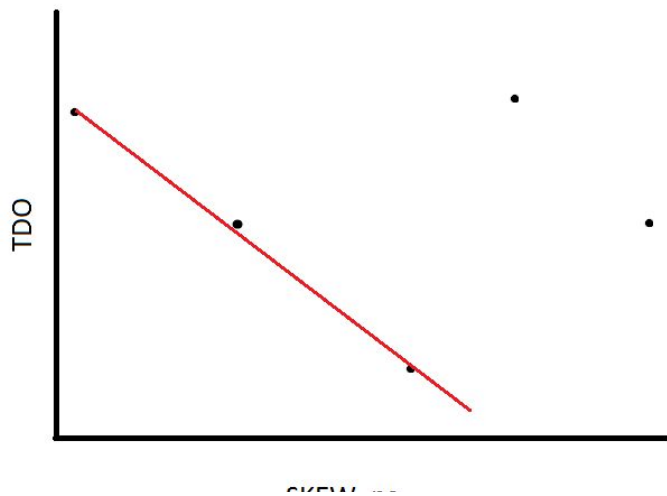
Channel 20

Channel=40



# Виды Тестов

- Калибровка
  - По времени





**Спасибо за внимание**