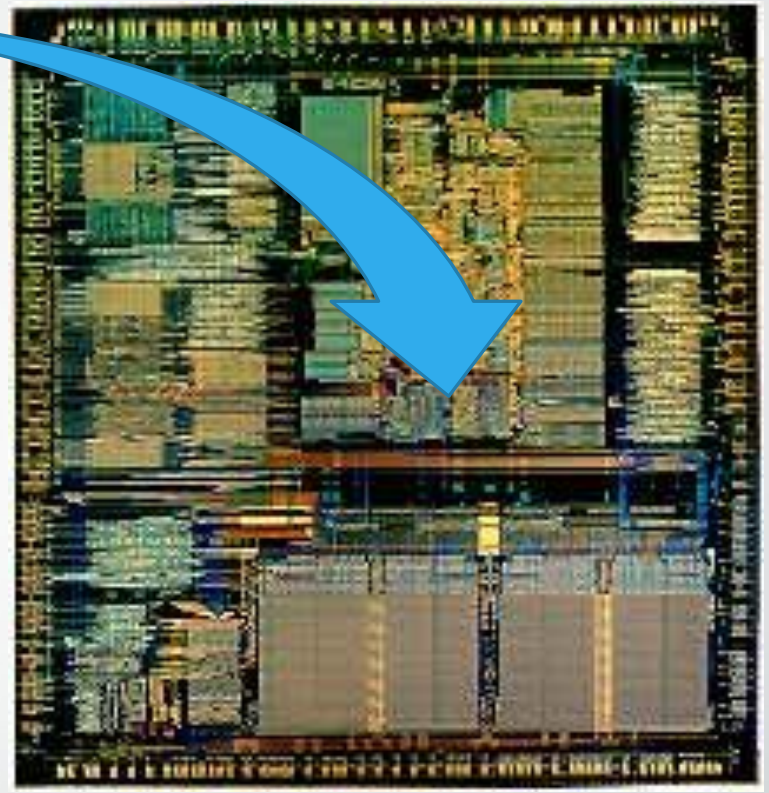
Logical foundations of system devices. Logic gates. Adders.

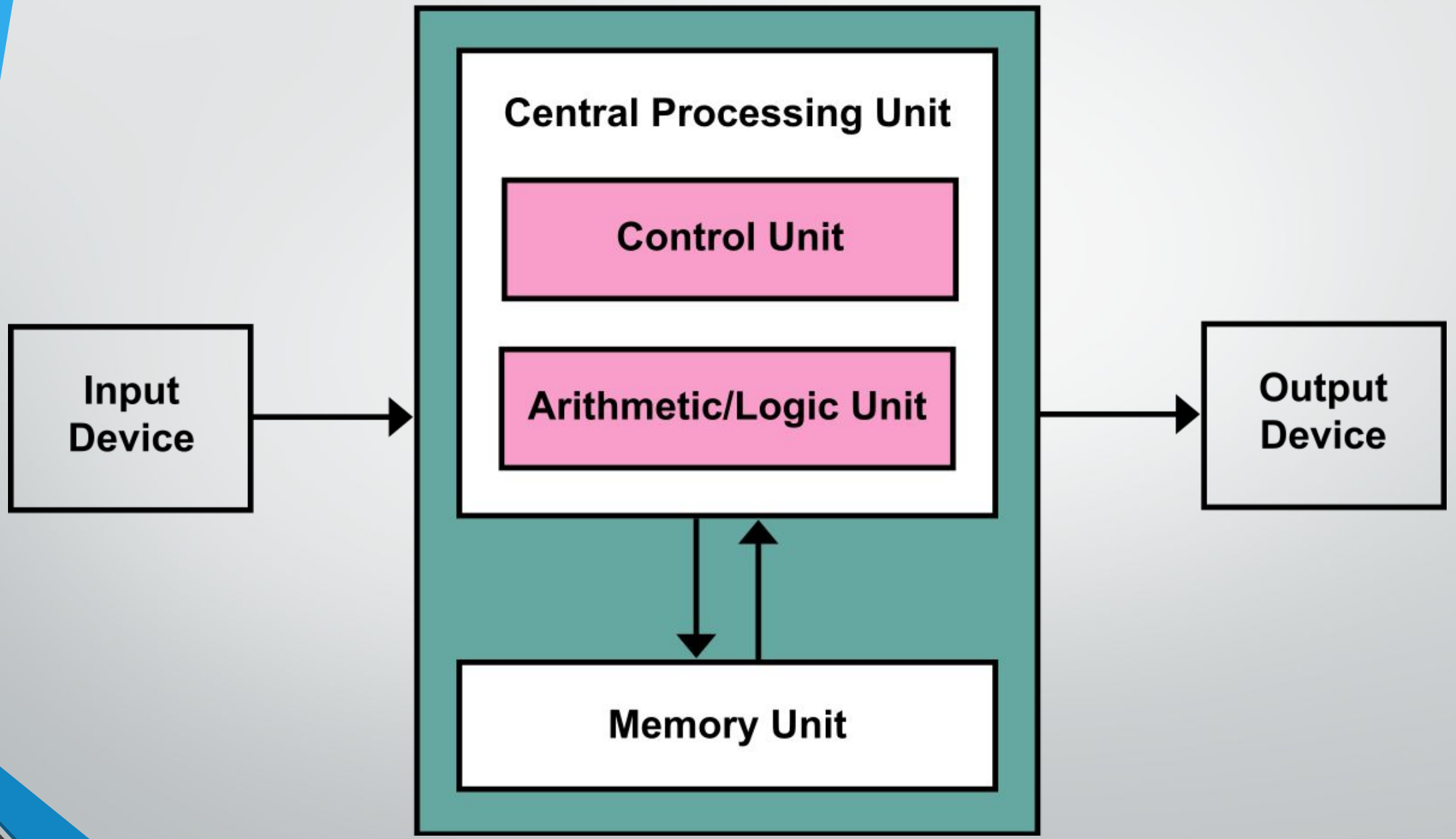
solve logistics problems at an elementary level

know that the CPU is made up from logic gates



What is von Neumann architecture?

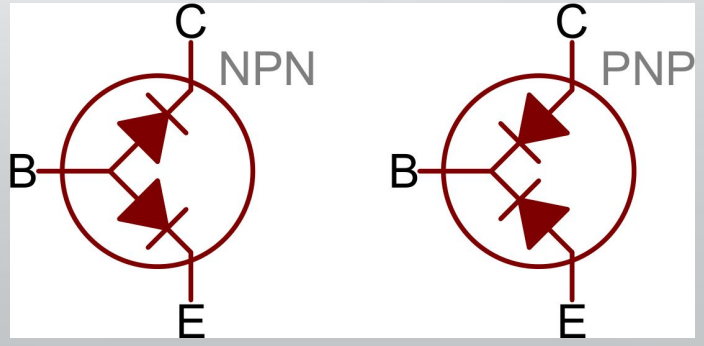
What does the microprocessor include?


Central Processing Unit
Control Unit
Arithmetic/Logic Unit
Input Device
Output Device
Memory Unit

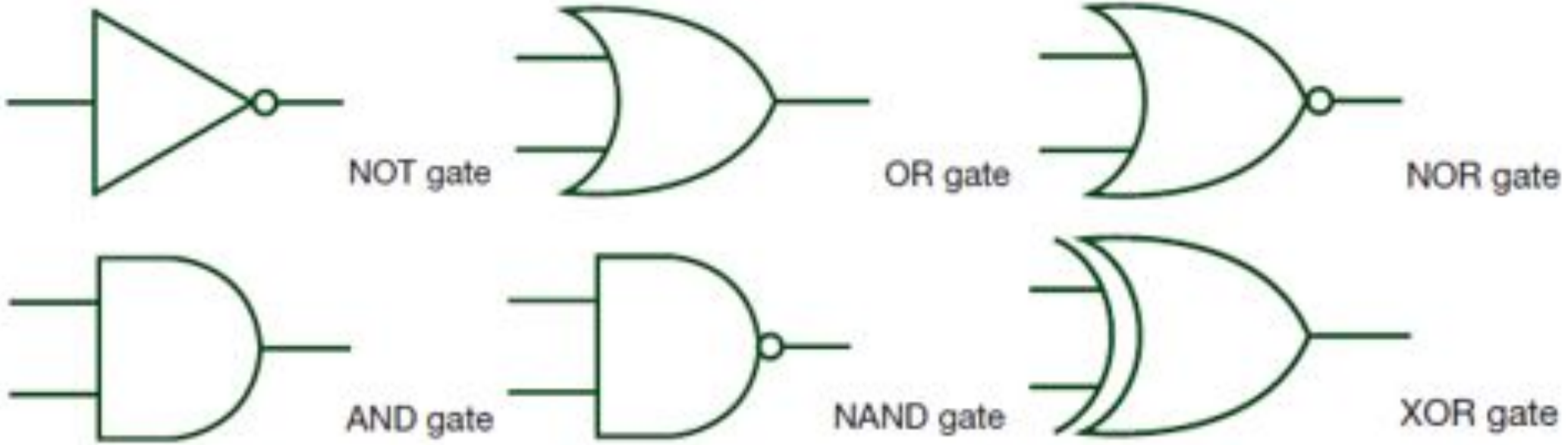
What are the functions of the ALU?

An **arithmetic logic unit** (**ALU**) is a combinational digital electronic circuit that performs arithmetic and bitwise operations on integer binary numbers.

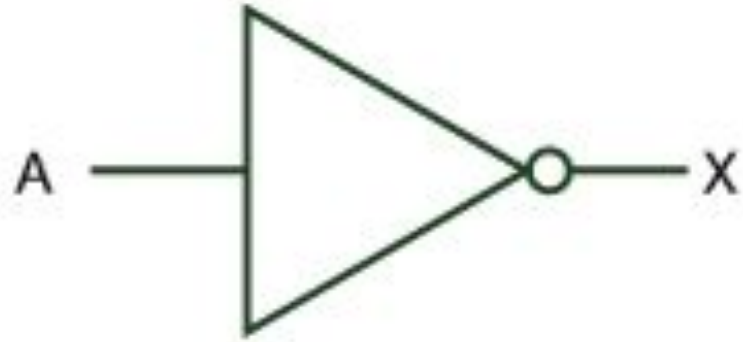
Logic gates are primarily implemented using diodes or transistors acting as electronic switches



Logic gates



NOT gate



The output (X) is **true** (i.e. 1 or ON) if:

INPUT A is **NOT TRUE** (i.e. 0 or OFF)

Truth table for: ***X = NOT A***

INPUT A	OUTPUT X
0	1
1	0

AND gate

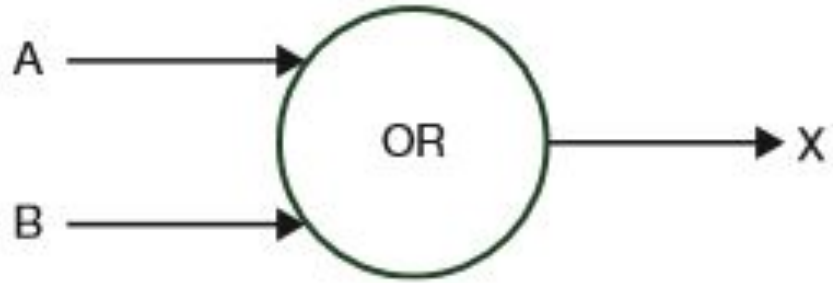
The output (X) is **true** (i.e. 1 or ON) if:

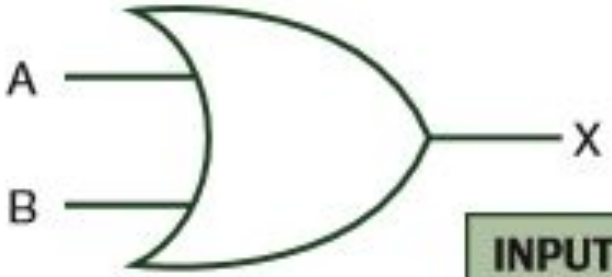
INPUT A AND INPUT B are **BOTH TRUE** (i.e. 1 or ON)

Truth table for: ***X = A AND B***

INPUT A	INPUT B	OUTPUT X
0	0	0
0	1	0
1	0	0
1	1	1

OR gate





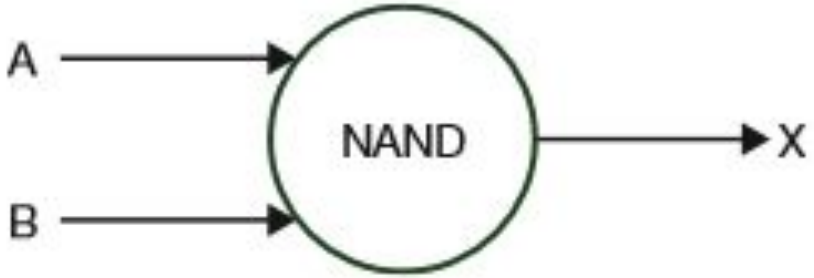
The output (X) is **true** (i.e. 1 or ON) if:

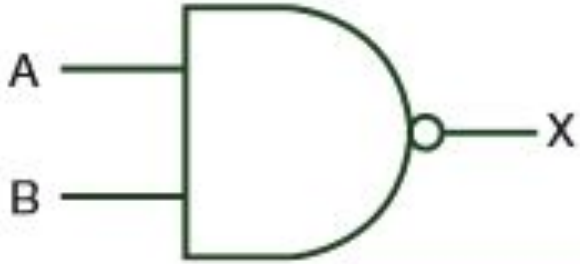
INPUT A OR INPUT B is **TRUE** (i.e. 1 or ON)

Truth table for: ***X = A OR B***

INPUT A	INPUT B	OUTPUT X
0	0	0
0	1	1
1	0	1
1	1	1

NAND gate





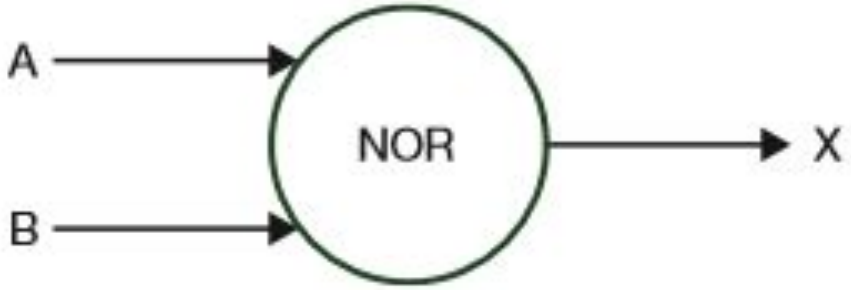
The output (X) is **true** (i.e. 1 or ON) if:

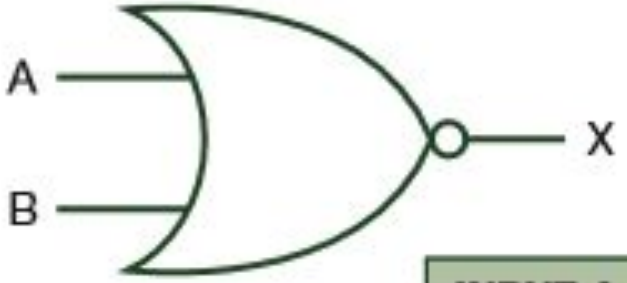
INPUT A AND INPUT B are **NOT BOTH TRUE** (i.e. 1 or ON)

Truth table for: ***X = NOT A AND B***

INPUT A	INPUT B	OUTPUT X
0	0	1
0	1	1
1	0	1
1	1	0

NOR gate





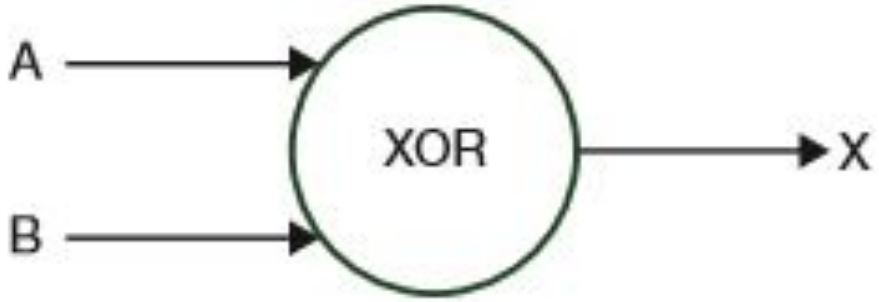
The output (X) is **true** (i.e. 1 or ON) if:

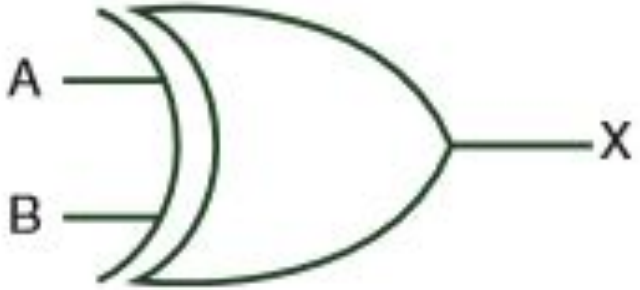
INPUT A OR INPUT B are **NOT BOTH TRUE** (i.e. 1 or ON)

Truth table for: ***X = NOT A OR B***

INPUT A	INPUT B	OUTPUT X
0	0	1
0	1	0
1	0	0
1	1	0

XOR gate





The output (X) is **true** (i.e. 1 or ON) if:

INPUT A OR (NOT INPUT B) OR (NOT INPUT A) OR INPUT B

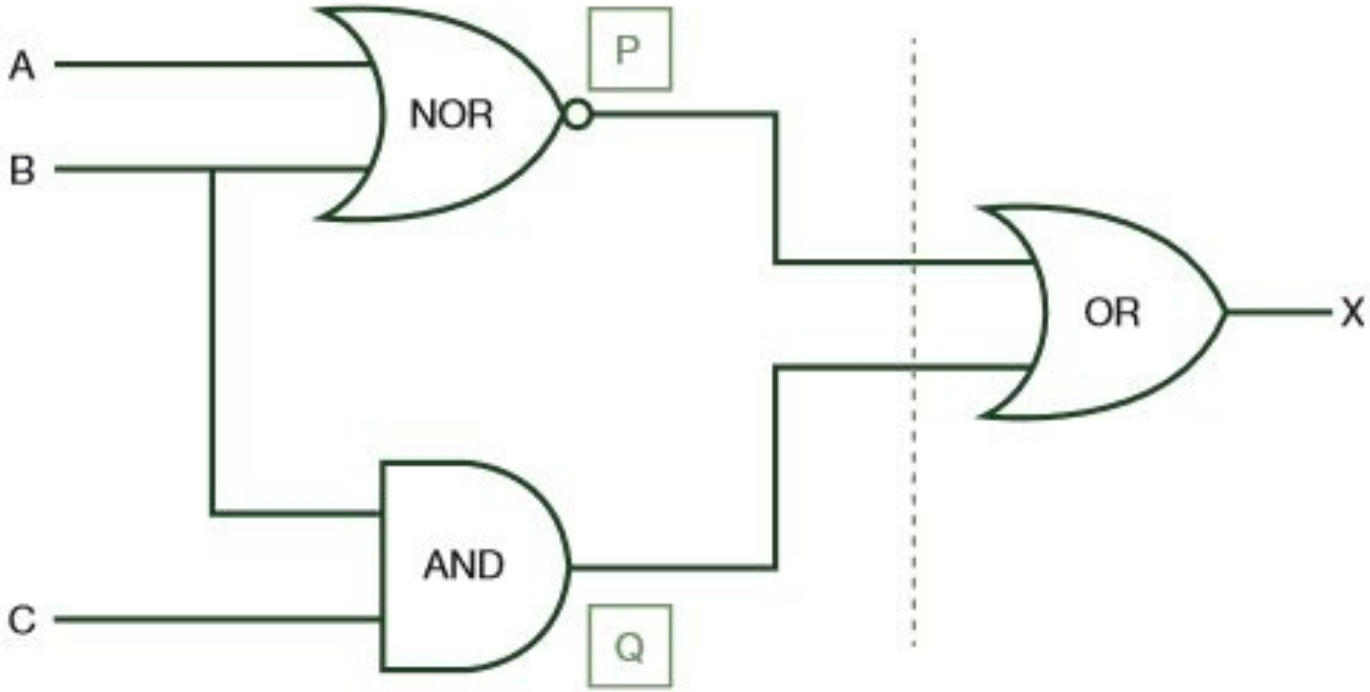
is **TRUE** (i.e. 1 or ON)

Truth table for: ***X = A OR (NOT B) OR (NOT A) OR B***

INPUT A	INPUT B	OUTPUT X
0	0	0
0	1	1
1	0	1
1	1	0

Example 1

Produce a truth table from the following logic circuit (network).



First part

There are 3 inputs; thus we must have 2^3 (i.e. 8) possible combinations of 1s and 0s.

To find the values (outputs) at points **P** and **Q**, it is necessary to consider the truth tables for the NOR gate (output P) and the AND gate (output Q) i.e.

P = A **NOR** B
Q = B **AND** C

We thus get:

INPUT A	INPUT B	INPUT C	OUTPUT P	OUTPUT Q
0	0	0	1	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	1

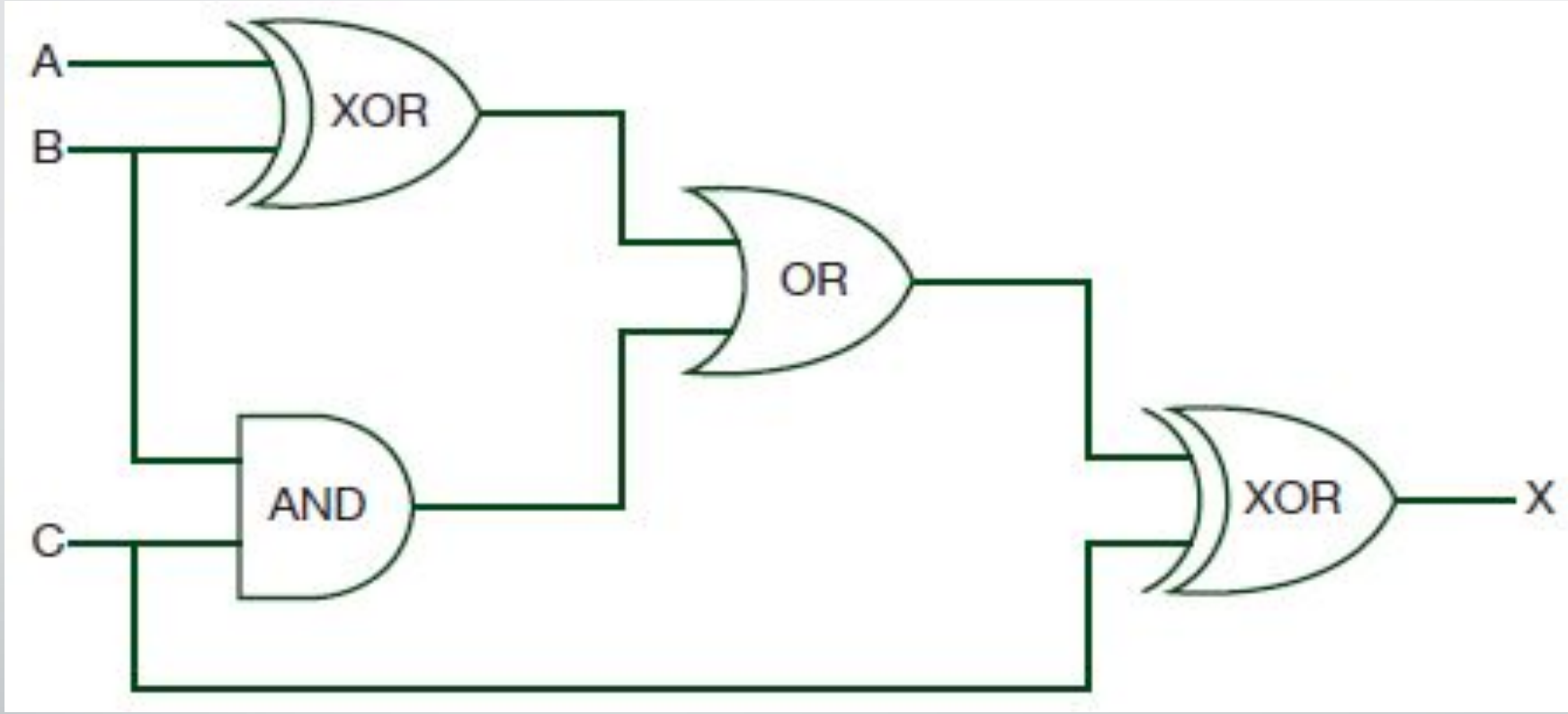
Second part

There are 8 values from P and Q which form the inputs to the last OR gate.

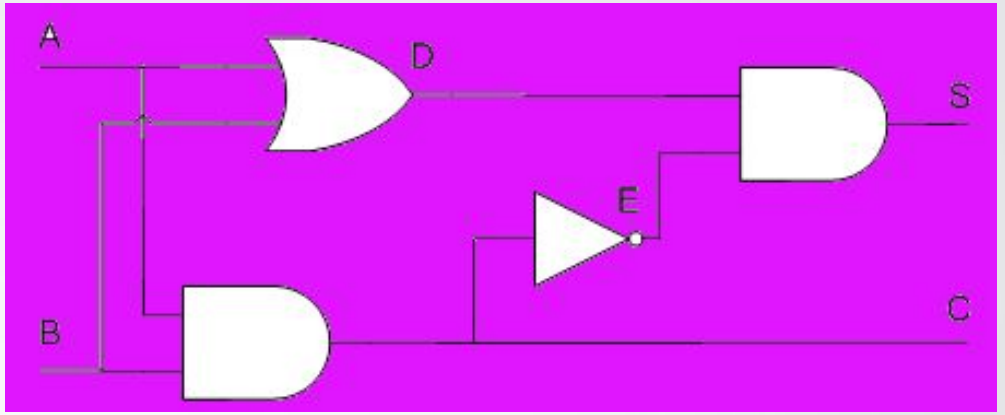
Hence we get X = P OR Q which gives the following truth table:

INPUT P	INPUT Q	OUTPUT X
1	0	1
1	0	1
0	0	0
0	1	1
0	0	0
0	0	0
0	0	0
0	1	1

Example 2



Half-Adder



- What is the output of this circuit?

A	B		D	E	S	C
0	0					
0	1					
1	0					
1	1					

- This circuit performs binary addition (C = carry)
- It also has a simpler equivalent:

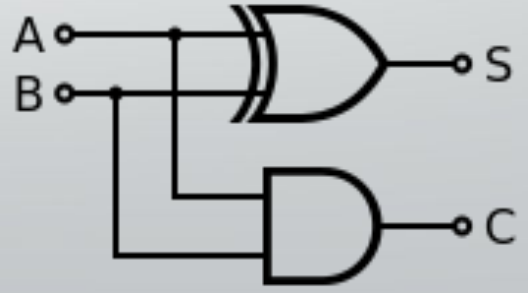
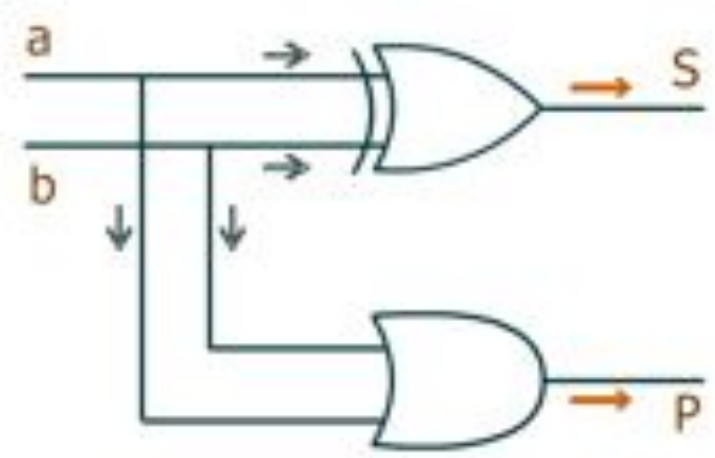
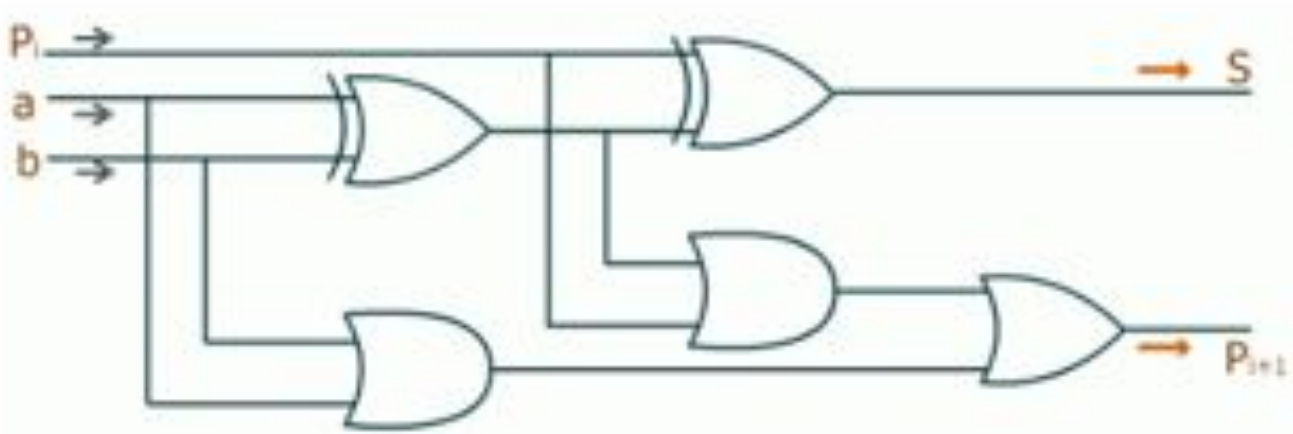


Схема полусумматора



a - первое слагаемое
b - второе слагаемое
S - сумма разряда
P - перенос в следующий разряд

Схема сумматора



a - первое слагаемое
b - второе слагаемое
S - сумма разряда
P_i - перенос из младшего разряда
P_{i+1} - перенос в старший разряд