Другие логические элементы
Определения

- Триггер
- Регистр
- Сумматор
- АЦП (ADC)
- ЦАП (DAC)

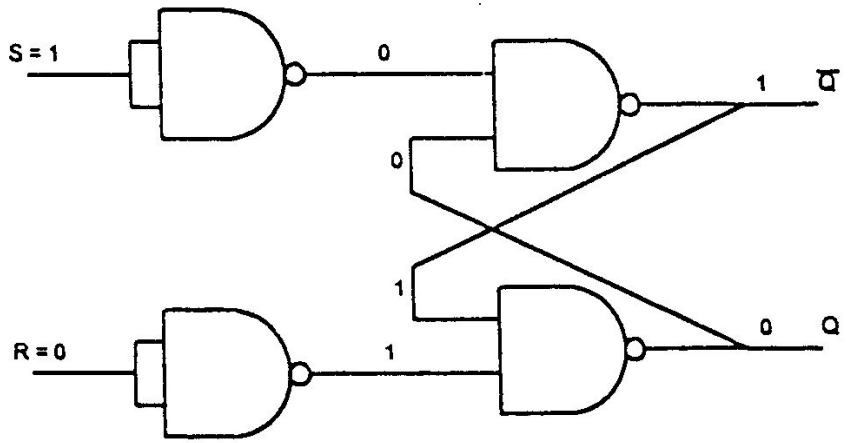
Триггер – Flip-Flop

- Триггер- ждущий мульльтивибратор
- Много есть типов
- Основные – три типа : Flip-Flops

  SR, RS , D или JK

SR Flip-Flop- ТРИГГЕР

The SR flip-flop has two output terminals Q and $\overline{Q}$. The diagram shows the SR flip-flop using NAND gates.



SR FLIP-FLOP

So basically the flip-flop can exist in two stable states:

$Q = 1\ (\overline{Q} = 0)$ or $Q = 0\ (\overline{Q} = 1)$.

SR Flip-Flop- ТРИГГЕР

When S = 1 R = 0 Q = 1 $\overline{Q}$ = 0 the flip flop is SET

When S = 0 R = 1 Q = 0 $\overline{Q}$ = 1 the flip flop is RESET

When S = 0 R = 0 then no change occurs Q and $\overline{Q}$ will be what they were before.

When S = 1 and R = 1 then Q = 1 and Q equals 1. The circuit is stable while S = R = 1, but if they are changed simultaneously from 1 to 0 then due to different switching times of the gates we cannot predict whether Q or $\overline{Q}$ will be 1.

The output state is said to be indeterminate so S = R = 1 should not be allowed to occur. The truth table is shown below.

Таблица FLIP-FLOP SR

S	R	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
0	0	Depends on state before inputs applied	
1	1	Indeterminate	

So basically the flip-flop can exist in two stable states:

$Q = 1$ ($\overline{Q} = 0$) or $Q = 0$ ($\overline{Q} = 1$).

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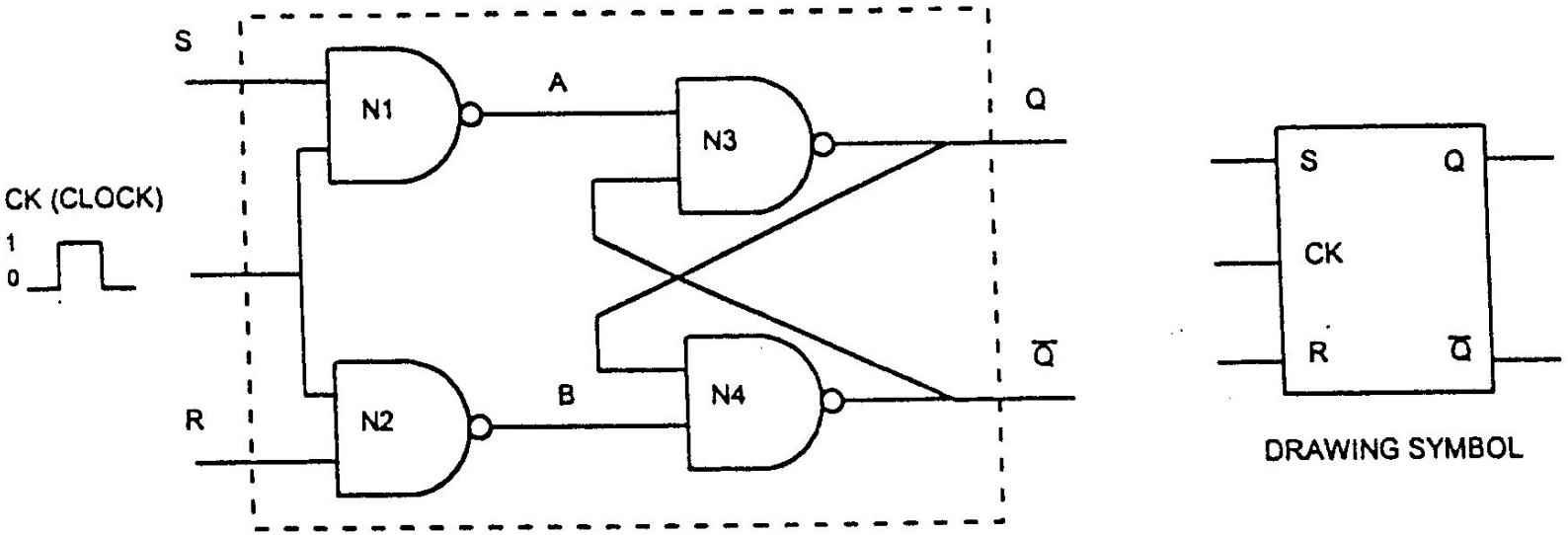
$Q = 1$ ($\overline{Q} = 0$) or $Q = 0$ ($\overline{Q} = 1$).

Clocks



CLOCKED SR FLIP FLOP

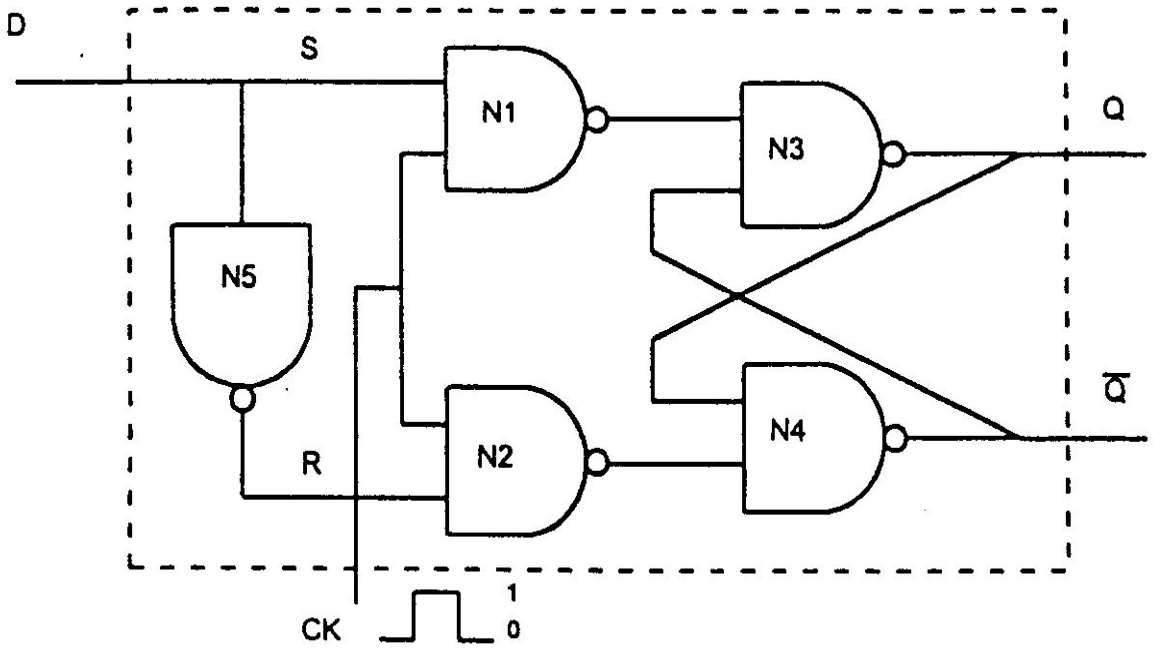
Clocks

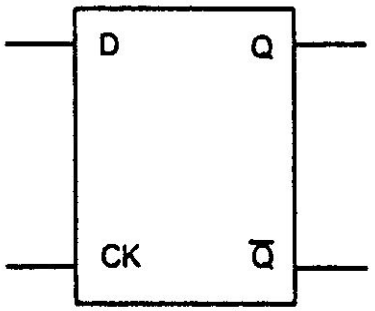
INPUTS		DURING CLOCK PULSE		OUTPUTS BEFORE CLOCK PULSE		OUTPUTS AFTER CLOCK PULSE		COMMENTS
S	R	A	B	Q	$\overline{Q}$	Q	$\overline{Q}$	
0	0	1	1	1	0	1	0	NO CHANGE IN OUTPUTS
0	0	1	1	1	0	1	0	
1	0	0	1	1	0	1	0	FLIP-FLOP SETS WITH $Q = 1$ & $\overline{Q} = 0$
1	0	0	1	0	1	1	0	
0	1	1	0	1	0	0	1	FLIP-FLOP RESETS WITH $Q = 0$ & $\overline{Q} = 1$
0	1	1	0	0	1	0	1	
1	1	0	0	1	0	1	1	THIS INPUT IS NOT ALLOWED
1	1	0	0	0	1	1	1	

TRUTH TABLE CLOCKED SR FLIP-FLOP

CLOCKED D- TYPE FLIP-FLOP

This is a modified SR flip-flop.

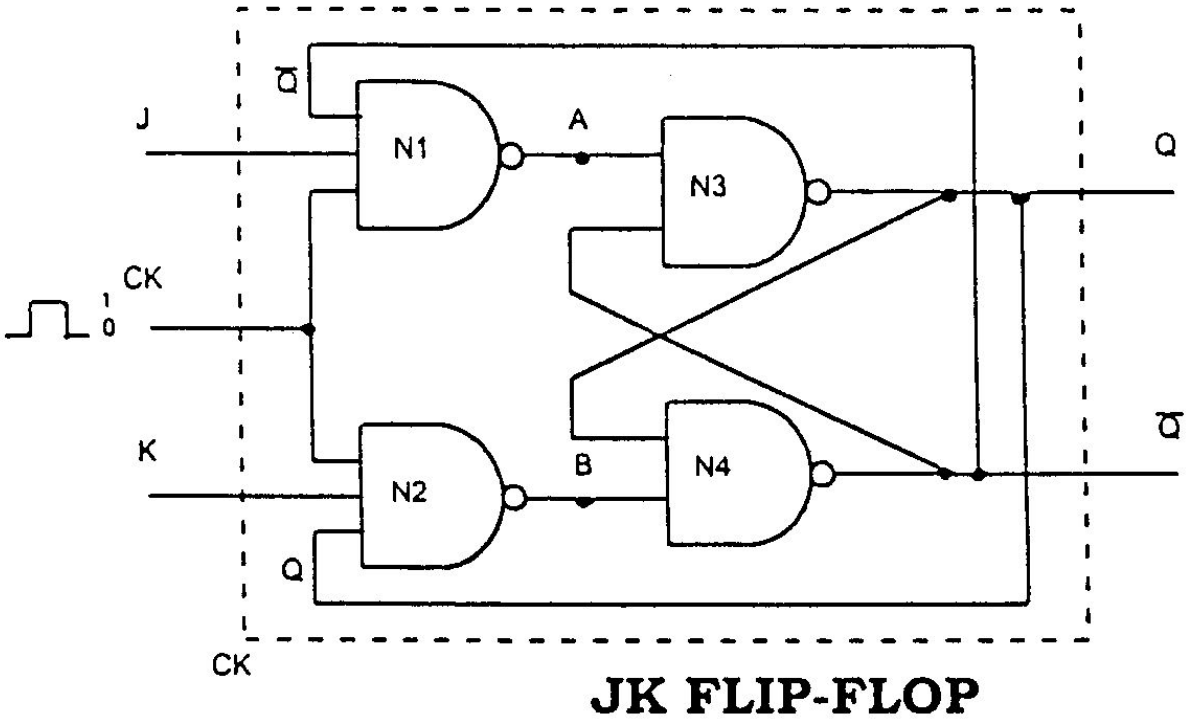




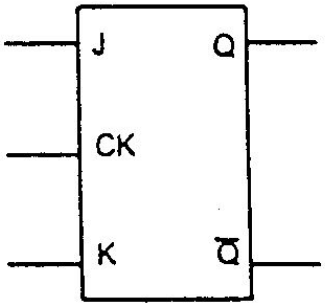
DRAWING SYMBOL

CLOCKED D TYPE FLIP-FLOP

JK FLIP - FLOP



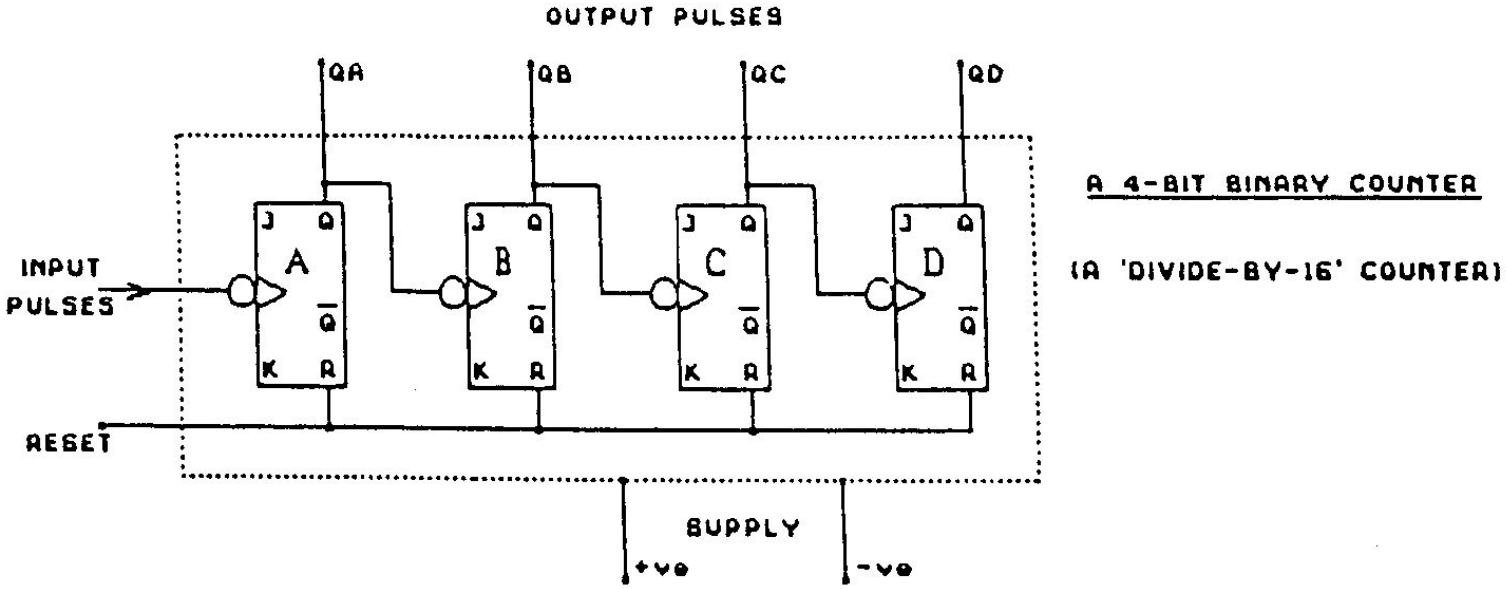
JK FLIP-FLOP



DRAWING SYMBOL

Эти триггеры используются в счётчиках и регистрах сдвига

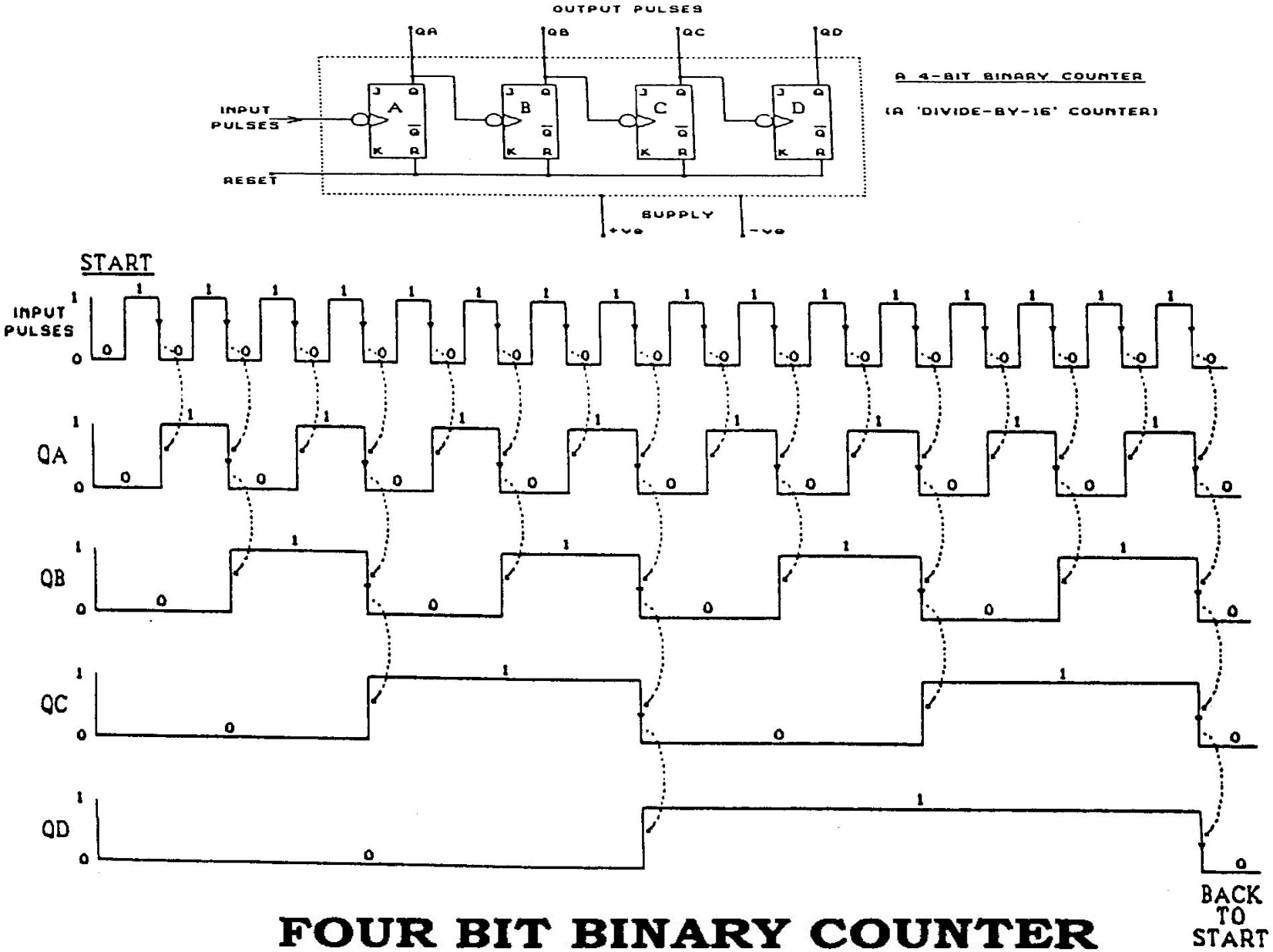
Counters – Счётчики



После 1-го импульса : Q_A= 1; Q_B=0; Q_C=0; Q_D=0; 0001 десят. 1

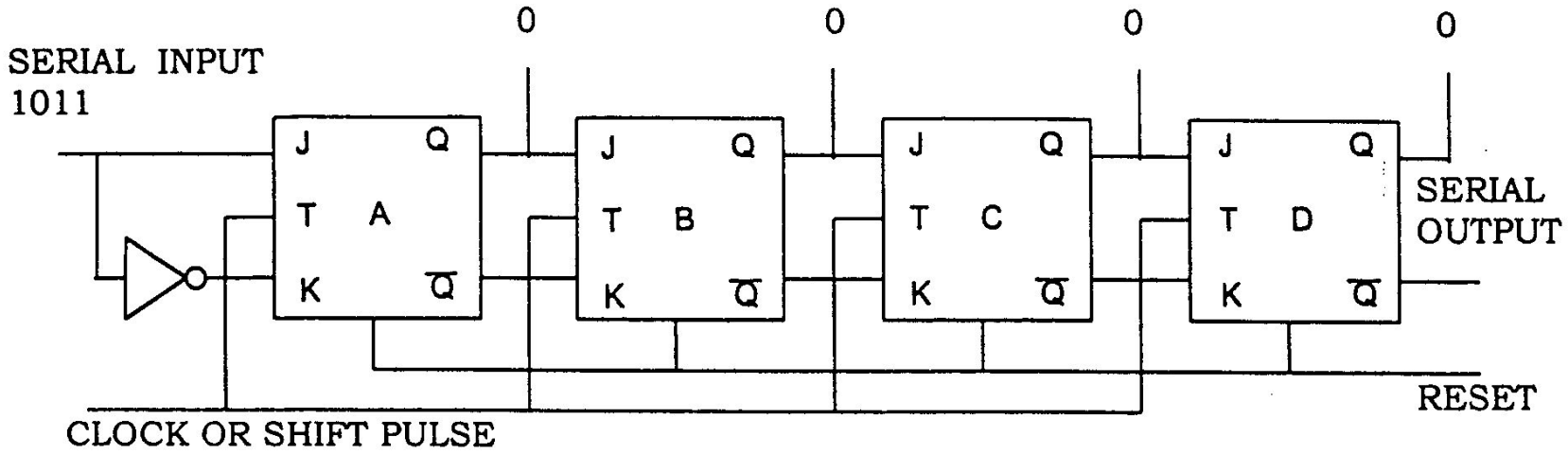
После 2-го импульса : Q_A= 0; Q_B=1; Q_C=0; Q_D=0; 0010 десят. 2

Когда счётчик достигнет 1111 десятичн. 15 - сброс регистров



FOUR BIT BINARY COUNTER

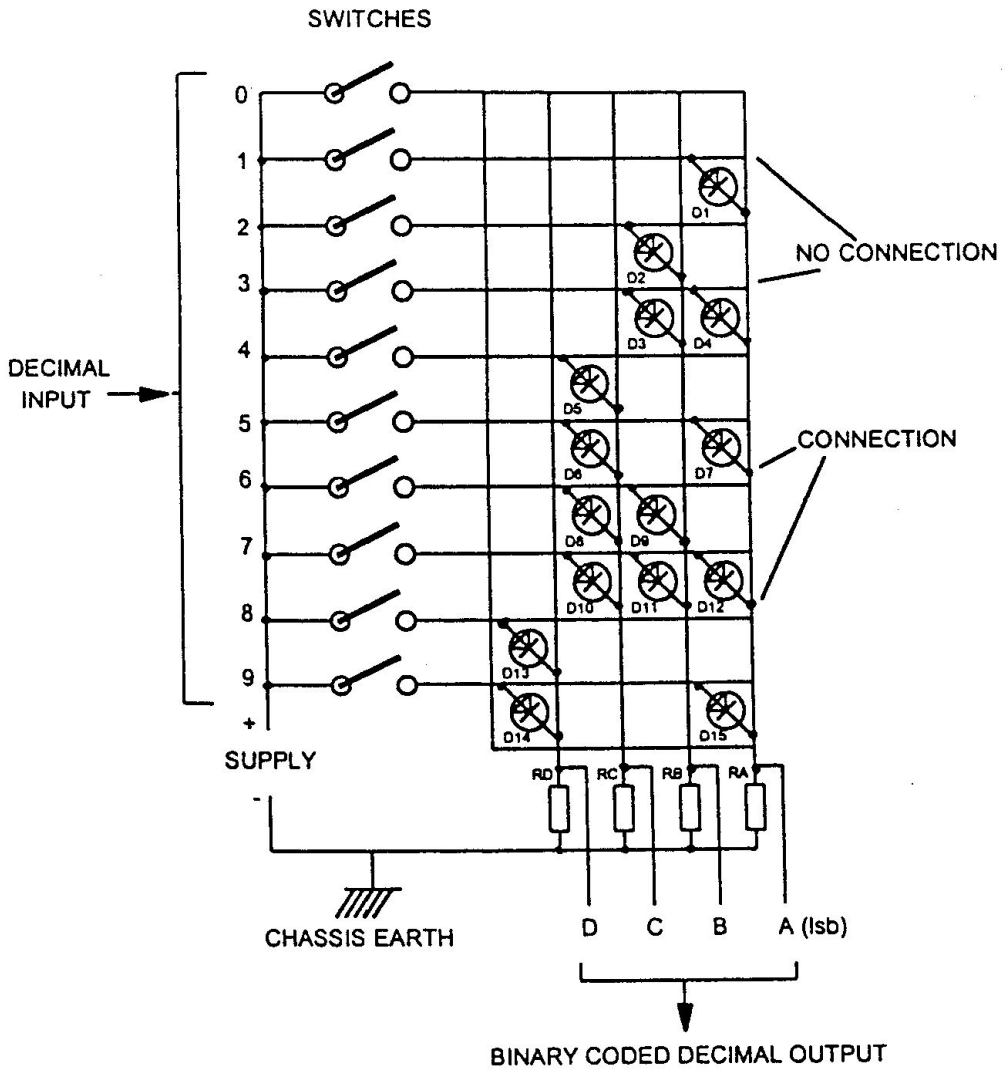
РЕГИСТР СДВИГА



FOUR BIT SHIFT REGISTER

Используется для хранения данных.
После каждого импульса содержание регистра смещается на одно место вправо

ENCODER- ШИФРАТОР

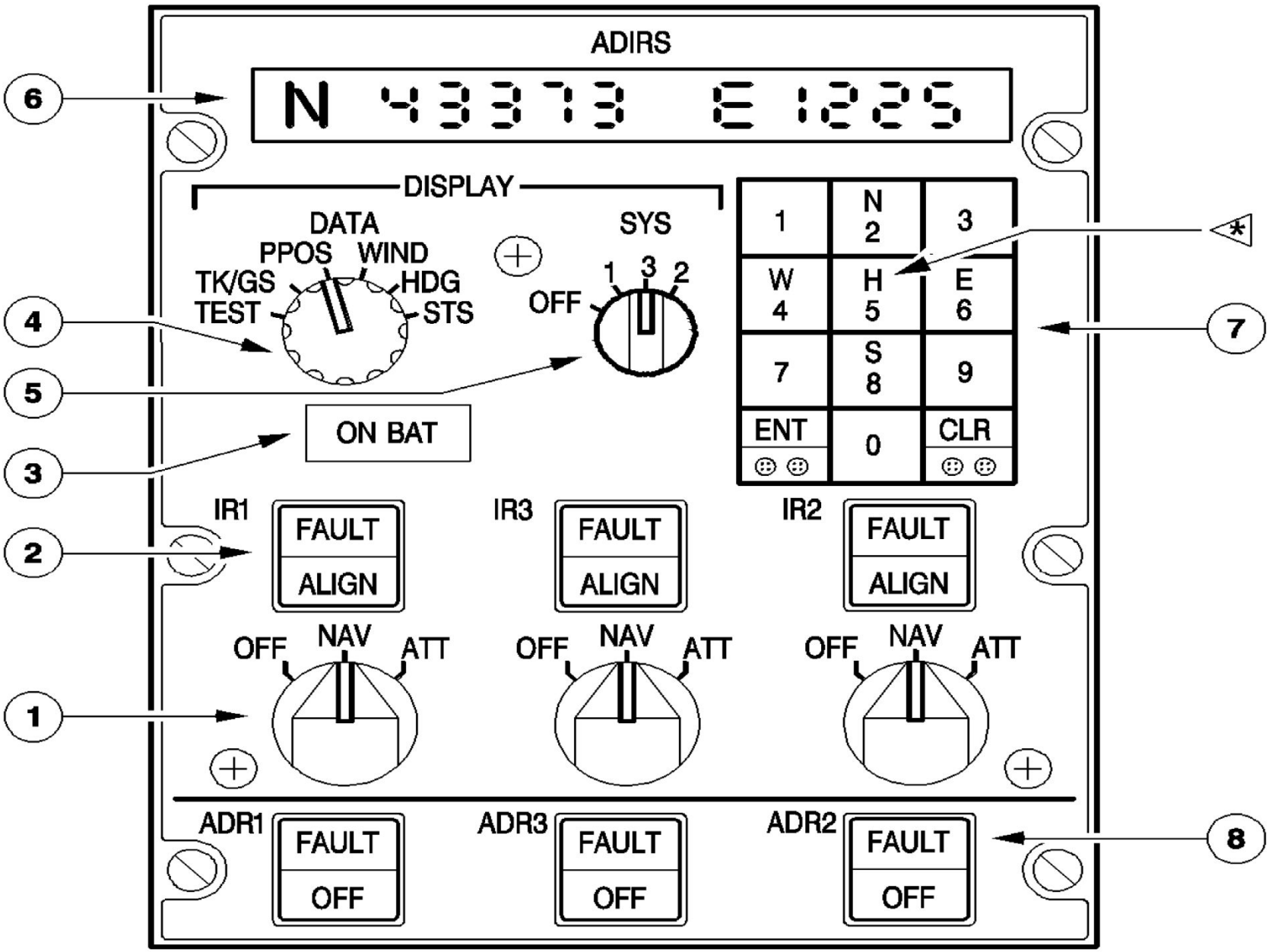


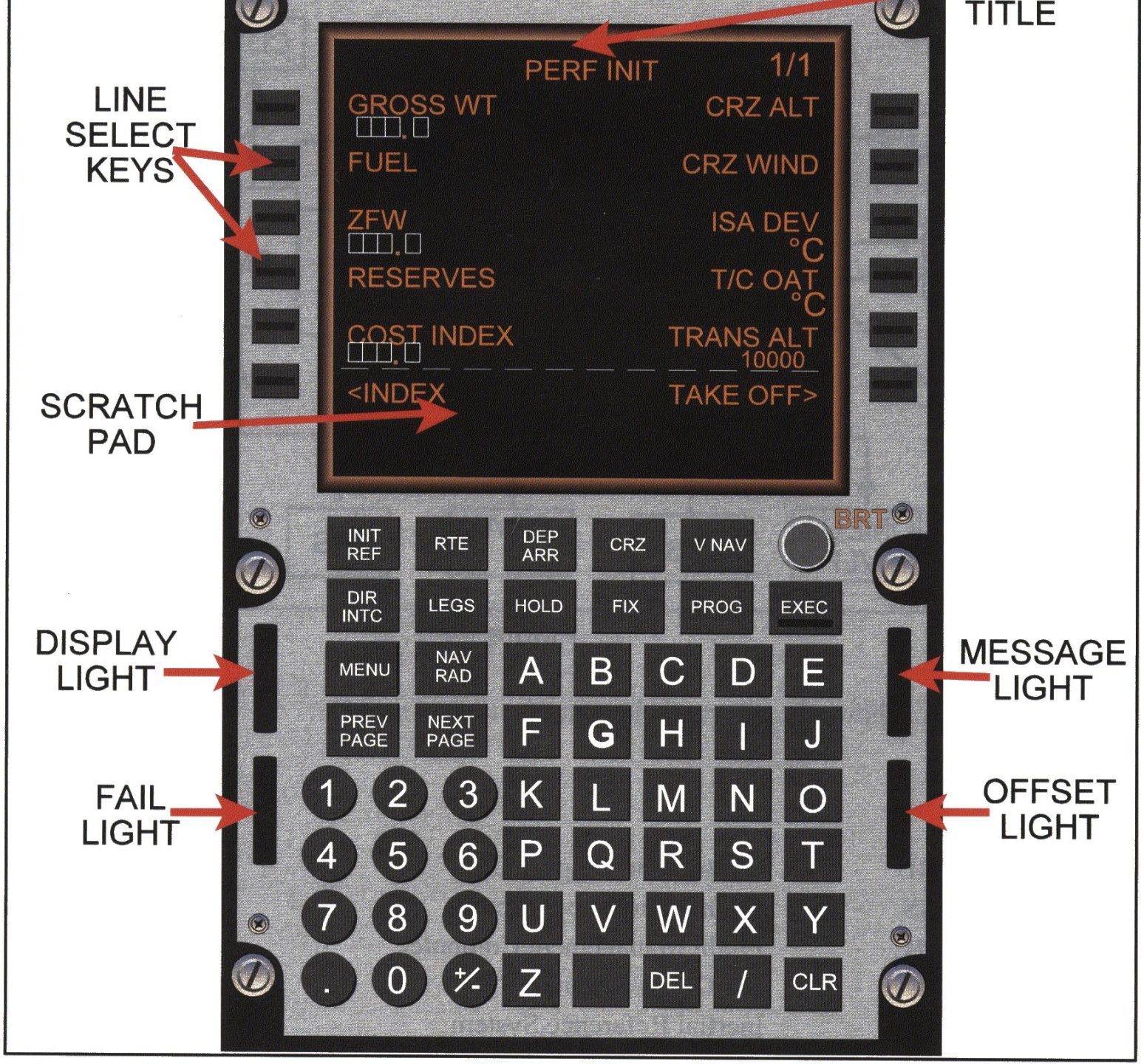
DECIMAL TO BCD ENCODER

Примеры использования

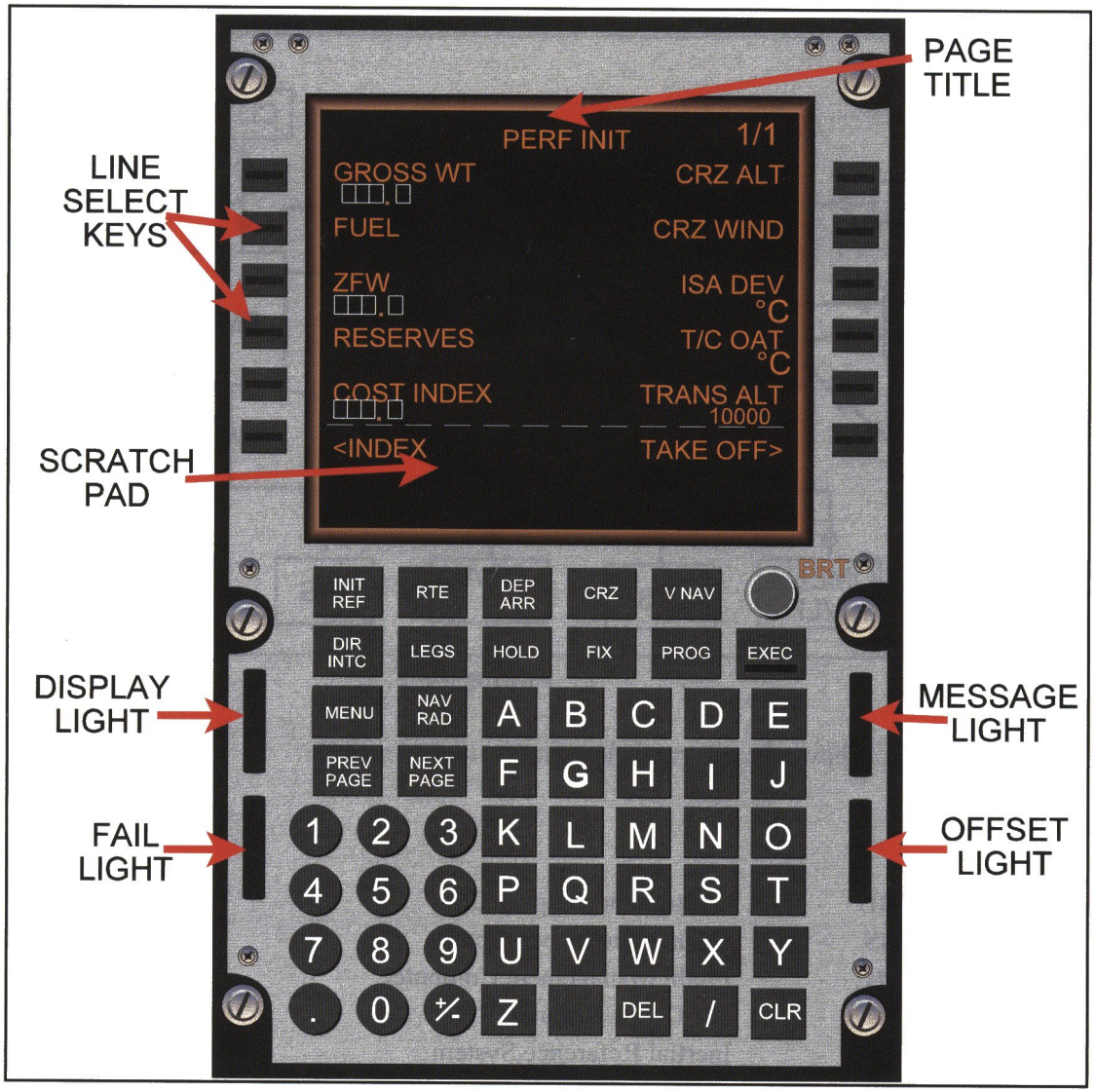
This principle will be employed in INS (Inertial Navigation Systems), IRS (Inertial Reference Systems) and FMS (Flight Management Systems) as all these have keyboards. So some form of encoding will convert the input signals into the correct code for the system.

INS , IRS , FMS идр

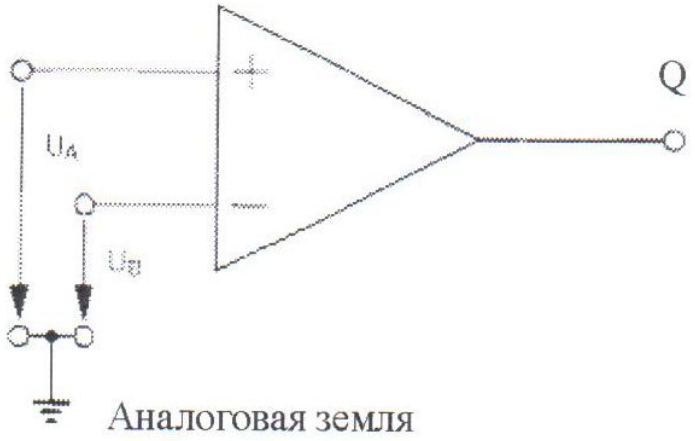

ADIRS
N 43373 E 1225
DISPLAY
DATA
PPOS
WIND
TK/GS
HDG
TEST
STS
SYS
OFF
1 3 2
ON BAT
1
N 2
3
W 4
H 5
E 6
7
S 8
9
ENT
0
CLR
*
IR1
IR3
IR2
FAULT
ALIGN
OFF
NAV
ATT
ADR1
ADR3
ADR2
FAULT
OFF
1
2
3
4
5
6
7
8


TITLE
PERF INIT
1/1
LINE SELECT KEYS
GROSS WT
CRZ ALT
FUEL
CRZ WIND
ZFW
ISA DEV °C
RESERVES
T/C OAT °C
COST INDEX
TRANS ALT
10000
SCRATCH PAD
<INDEX
TAKE OFF>
BRT
INIT REF
RTE
DEP ARR
CRZ
V NAV
DIR INTC
LEGS
HOLD
FIX
PROG
EXEC
DISPLAY LIGHT
MENU
NAV RAD
MESSAGE LIGHT
PREV PAGE
NEXT PAGE
FAIL LIGHT
OFFSET LIGHT
DEL
CLR

CDU FMS

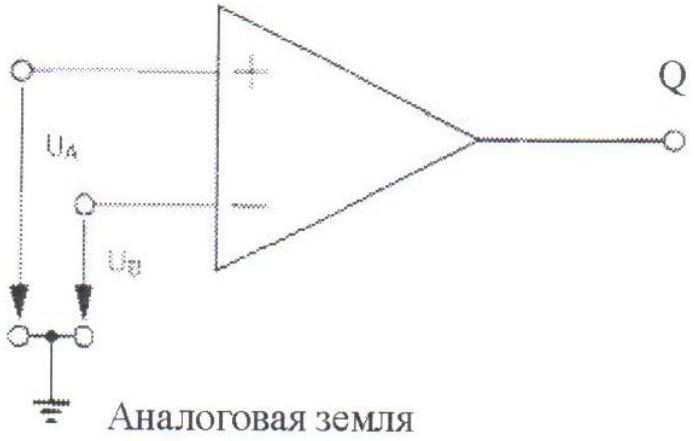

PAGE TITLE
PERF INIT 1/1
GROSS WT
CRZ ALT
FUEL
CRZ WIND
ZFW
ISA DEV °C
RESERVES
T/C OAT °C
COST INDEX
TRANS ALT 10000
<INDEX
TAKE OFF>
LINE SELECT KEYS
SCRATCH PAD
BRT
INIT REF
RTE
DEP ARR
CRZ
V NAV
DIR INTC
LEGS
HOLD
FIX
PROG
EXEC
MENU
NAV RAD
PREV PAGE
NEXT PAGE
DISPLAY LIGHT
MESSAGE LIGHT
FAIL LIGHT
OFFSET LIGHT
DEL
CLR

Аналого-цифровое преобразование без обратной связи
Компаратор



Входное напряжение	Логический выход
$U_A > U_B$	Q=1
$U_A < U_B$	Q=0
$U_A = U_B$	Предыдущее состояние

Аналого-цифровое преобразование без обратной связи
Компаратор



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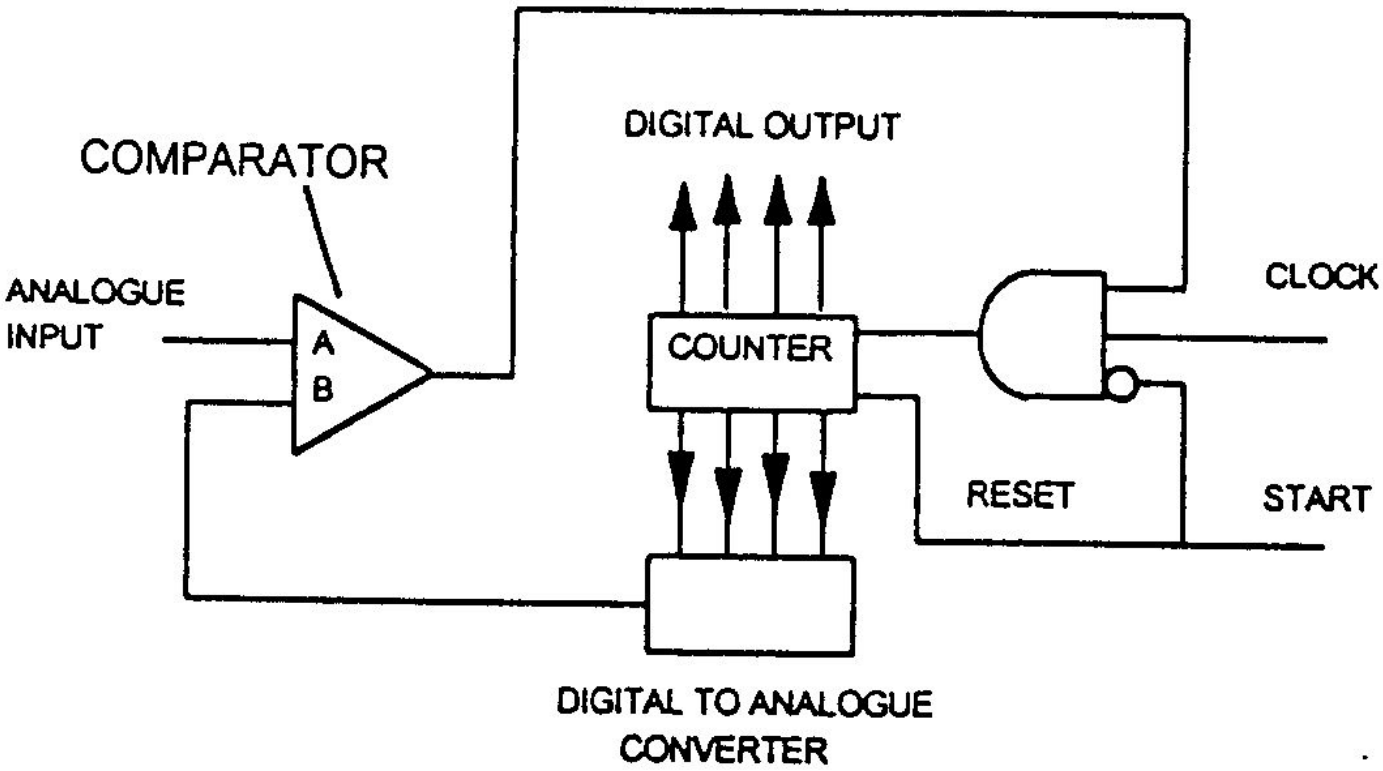
АЦП считывания (Flash Convertor)
Таблица выходов

Входное напряжение	Выходы компараторов									Выходы шифратора			Over-flow
	Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	B_2	B_1	B_0	
меньше 0 В	0	0	0	0	0	0	0	0	0	0	0	0	0
0<U<1,25 В	0	0	0	0	0	0	0	0	1	0	0	0	0
1,25<U<2,5 В	0	0	0	0	0	0	0	1	1	0	0	1	0
2,5<U<3,75 В	0	0	0	0	0	0	1	1	1	0	1	0	0
3,75<U<5,0 В	0	0	0	0	0	1	1	1	1	0	1	1	0
5,0<U<6,25 В	0	0	0	0	1	1	1	1	1	1	0	0	0
6,25<U<7,5 В	0	0	0	1	1	1	1	1	1	1	0	1	0
7,5<U<8,75 В	0	0	1	1	1	1	1	1	1	1	1	0	0
8,75<U<10,0В	0	1	1	1	1	1	1	1	1	1	1	1	0
10,0 < U	1	1	1	1	1	1	1	1	1	0	0	0	1

АЦП (ADC)



ANALOGUE TO DIGITAL CONVERTER

АЦП (ADC)

A comparator is a device with two inputs which compare the voltages at each input to determine which is greater, the output is logic 1 if A is larger than B and logic 0 if input B is larger than A. On start B is 0, A is the larger output, from the comparator is logic state1 and when the START pulse goes low the AND gate 'opens' and the clock pulses go to the counter. Each pulse causes the counter to advance.

As the counter counts up, its value is converted into it's analogue equivalent by the digital to analogue convertor (DAC or D to A or D/A) and applied to the comparator at B. The DAC output therefore increases in steps until it reaches just above the analogue input level ie, B input >A. The comparator output goes low, AND gate closes, the count stops, the digital read-out is then taken from the counter.

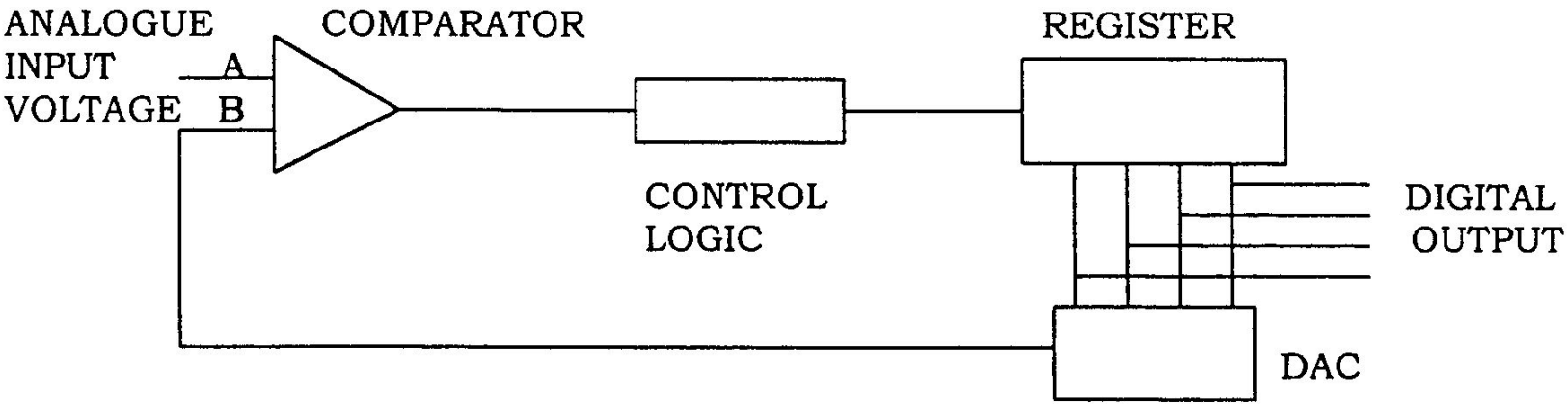
АЦП (ADC)

The best approximation we can obtain, depends on how much input B has to be greater than A ie, the step size, this is known as the quantization error. This type of Analogue to Digital (ADC or A to D or A/D) converter is slow in operation and is unsuitable for high speed operation, and of course the larger the voltage the longer (more steps) time it takes. The comparator would be an operational amplier (see JAR Module 4).

This problem can be partly overcome by using an up/down counter. It counts up when the comparator is logic 1 and down when the comparator output is logic 0. As the analogue input varies it simply counts up or down from the previous count rather than re-setting to zero as did the digital ramp convertor. This type is called the continuous digital-ramp convertor and is a considerable improvement on the previous one.

However, the fastest type of ADC of the ones considered is the successive approximation type.

АЦП-



SUCCESSIVE APPROXIMATION TYPE OF D TO A CONVERTER

АЦП-

SUCCESSIVE APPROXIMATION TYPE OF D TO A CONVERTER

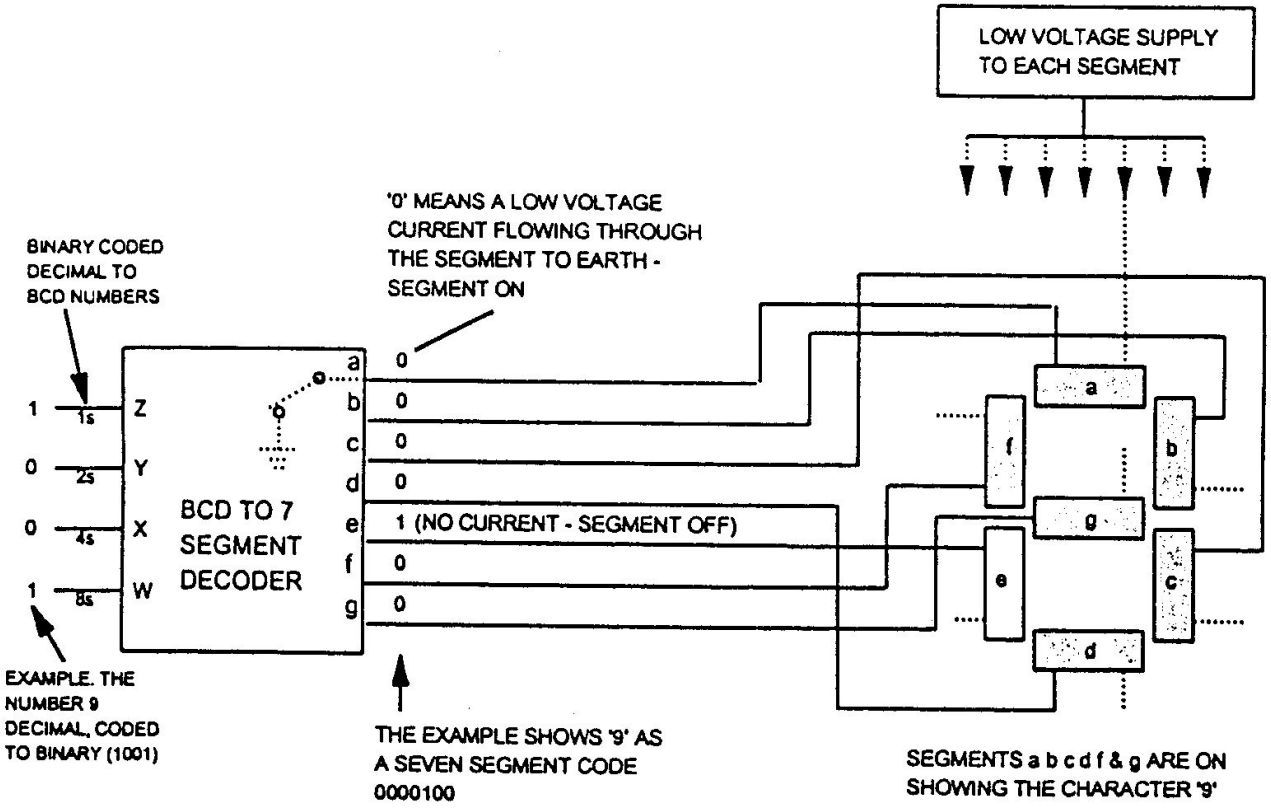
This is similar to the previous circuit but the register is used instead of a counter and a control logic block is included between the comparator and register, which controls the output of the register.

Initially a reset signal puts all bits in the register to 0. The control logic sets the MSB in the register to 1 and the rest to logic 0. The output of the DAC is then compared to the analogue input if B > A then this number is too large and the MSB remains at 1.

At the next clock pulse the control changes the next bit in the register B>A it is set to 0 if B<A it is set to 1 and so on until all the bit values are found. The digital read out can then be read.

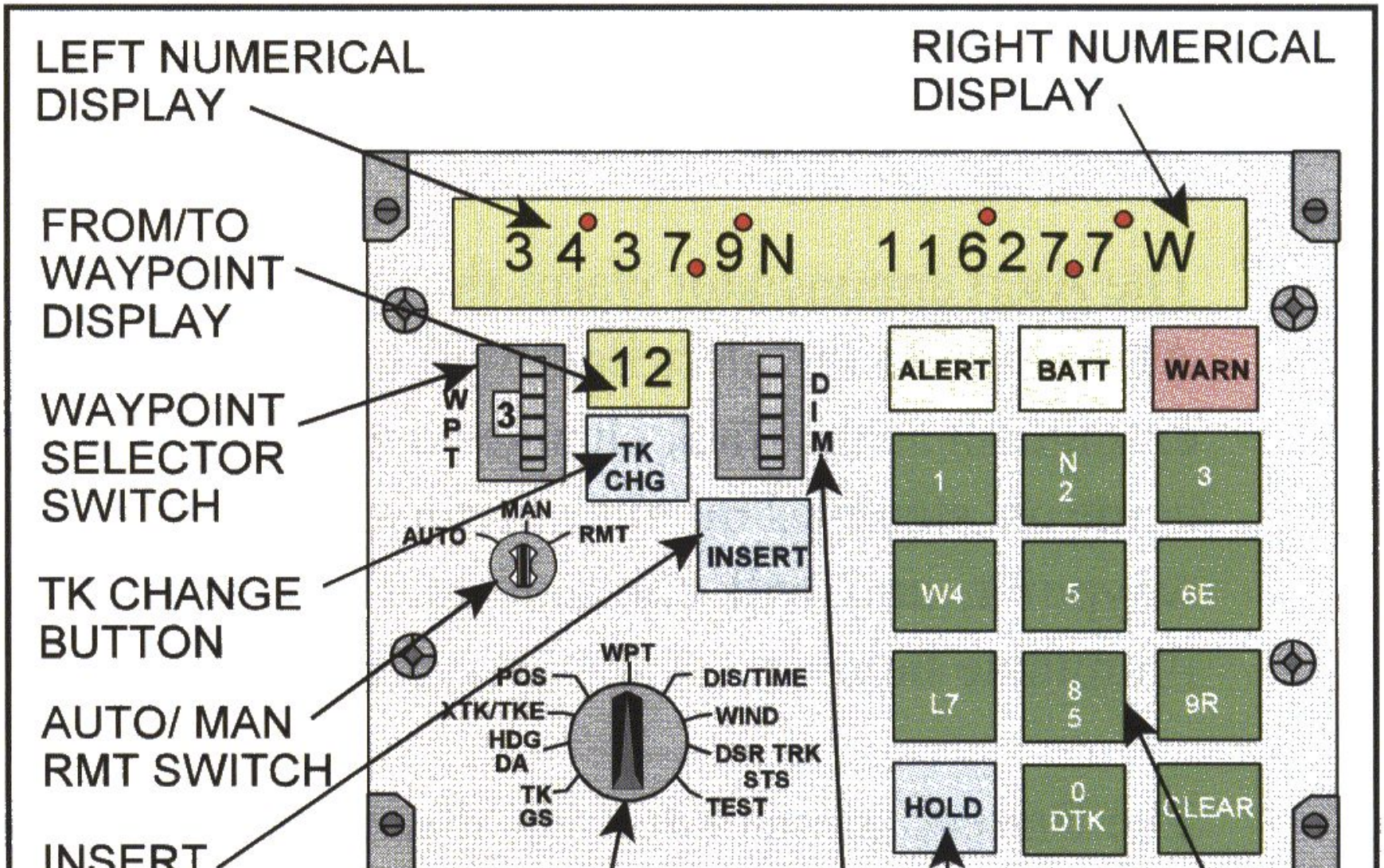
This has a fast conversion time which does not depend on the analogue voltage level but just the number of bits in the convertor.

DECODER- ДЕШИФРАТОР

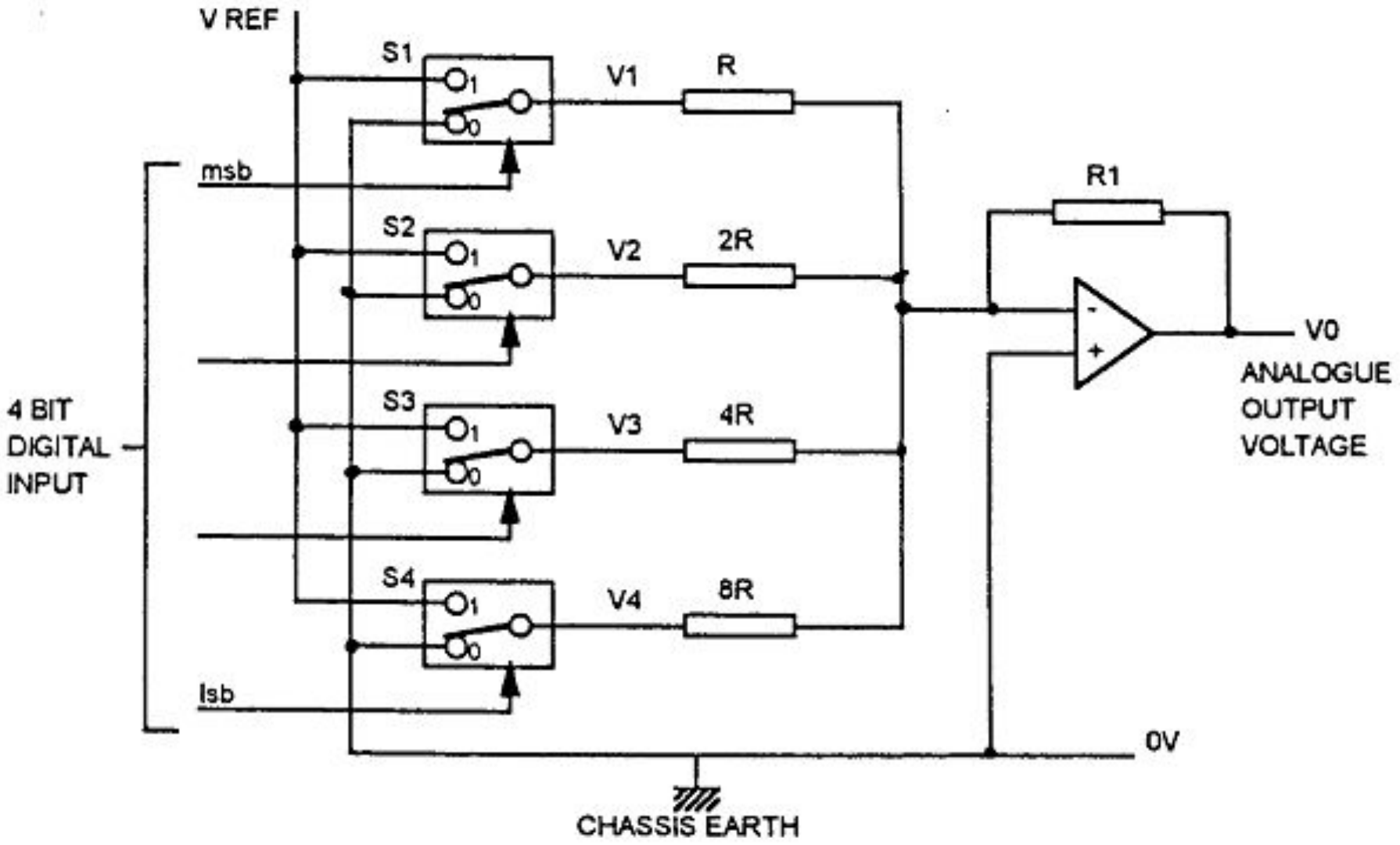


BCD TO SEVEN SEGMENT DECODER

Примеры использования



ЦАП (DAC) – Цифро-аналоговый преобразователь



ЦАП (DAC) – Цифро-аналоговый преобразователь

Digital to Analogue Converter

The next drawing shows a binary weighted resistor method, so called as the values of the resistors increase in accordance with the binary system eg, R, 2R, 4R, 8R. The output from the resistor chain is connected to an operational amplifier as a summing amplifier with a feedback resistor R_f. The output V_0 is therefore $V_0 = -R_f\left(\frac{V_1}{R} + \frac{V_2}{2R} + \frac{V_3}{4R} + \frac{V_4}{8R}\right)$ (see JAR Module 4)

Also in the circuit are four switches S, S_1, S_2, S_3, S_4 which are electronic switches (digitally controlled). Each switch connects the resistor to a fixed reference V_{ref} when the input bit is logic 1 (+5v) and to ground (0v) when the input bit is logic 0.

Assuming that $R_f = R = 1K$ then the output formula becomes:

$$V_0 = -\left(V_1 + \frac{V_2}{2} + \frac{V_3}{4} + \frac{V_4}{8}\right)$$

If the input number is 0001 then:

$$V_1 = V_2 = V_3 = 0$$

ЦАП (DAC) – Цифро-аналоговый преобразователь

ie each of the electronic switches connecting the input to ground.

V_4 will be connected to V_{ref}, we will assume that V_{ref} is – 8v so the formula becomes:

$$V_0 = -\left(0 + 0 + 0_4 - \frac{8}{8}\right)$$

$$V_0 = +\ 1v$$

Note. With the example shown the output was positive but if V_{ref} was +8v then the output would be –1v.

With an input of 0100 $V_1 = V_3 = V_4 = 0$

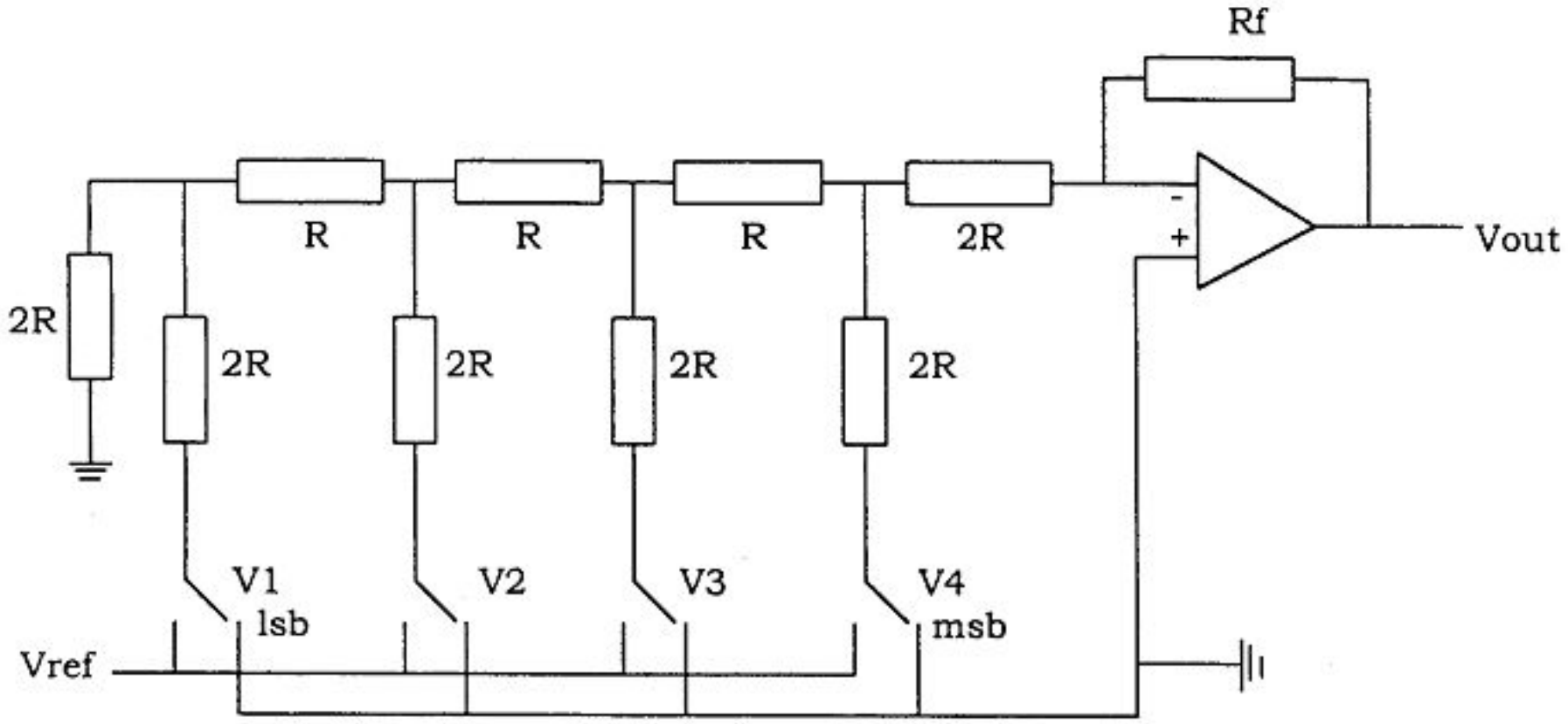
$V_2 = V_{ref}$. Assume again $V_{ref} = -8v$

$$V_0 = -\left(-\frac{8}{2}\right) = +\ 4v$$

$$V_0 = \left(0 + -\frac{8}{2} + 0 + 0\right)$$

As you can see the weighting of the LSB is 1v *in this case.*

R-2R Type D to A Convertor



Another problem is the larger the bit word the more the range of resistors is required ie, for every extra bit the range of the required resistors doubles. So another method of converting digital to analogue must be found for digital words with a large number of bits - it is called the R – 2R type.

R-2R Type D to A Convertor

The circuit works on the principle that a pair of 2R resistors at the end of the ladder can be considered in parallel, forming an overall resistance R.

This system does use twice the number of resistors compared to the binary weighted network, but the use of only two values of resistors means the system can handle any number of input bits, simply be extending the resistor ladder.

It is not essential you know the full operation of this DAC but you should know it exists.

With reference to the drawing above $V_{out} = \frac{V}{16} \cdot \frac{R_f}{R}(8v_4 + 4v_3 + 4v_2 + 4v_1)$ for the bit input shown.