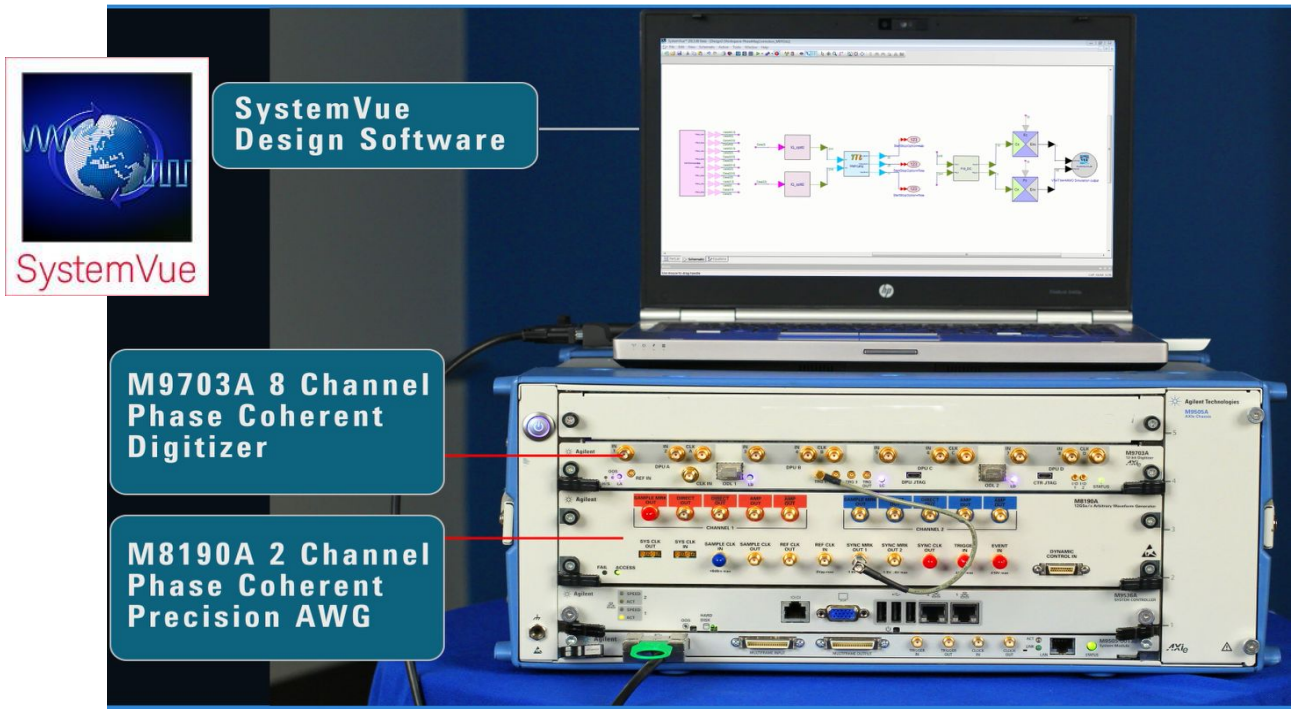
Using SystemVue's Open FPGA Design Flow + M8190A Sig Gen + M9703A High Speed Digitizer

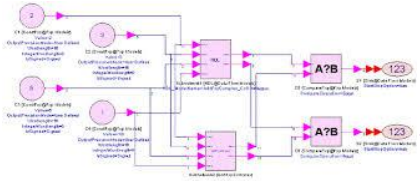
April 17, 2015



KEYSIGHT TECHNOLOGIES

Hardware Design Using SystemVue

SystemVue



Graphical Design Entry

Signal Generation

ModelSim PRO

3rd Party HDL Simulators

System Level Modeling

FPGA

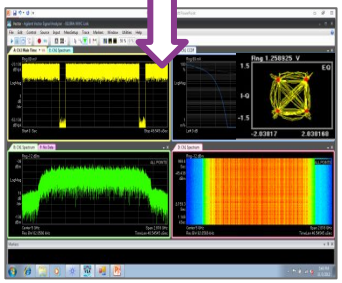
FPGA Platforms

HDL Files

IP

Textual/Binary Entry

Signal Analysis



Instrument FPGA

SystemVue Hardware Design Kit

Model based graphical design tool

Predict hardware behaviors, before committing to a full FPGA implementation

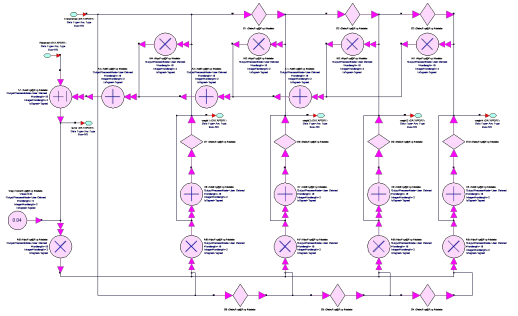
- Cycle-accurate, Bit-true model
- Examine bit growth and adjust the word length setting
- Detect the event of overflow and underflow

Realistic RTL level design and verification tool

- IP integration with custom HDL code import and Xilinx IP integrator
- Co-simulation with RTL simulators ModelSim / QuestaSim and RiveraPRo
- Automatic HDL code generation

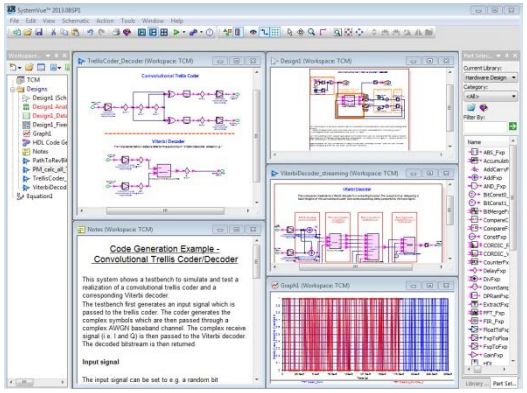
Functional verification revolution

- Combined with communication architect platform SystemVue
- Provide direct connection with Keysight instrument and measurement software



Graphical hardware design entry using vendor independent fixed point primitive models

Fully parameterized higher level fixed point blocks



Hierarchical desktop design environment with integrated display, analysis and co-simulation

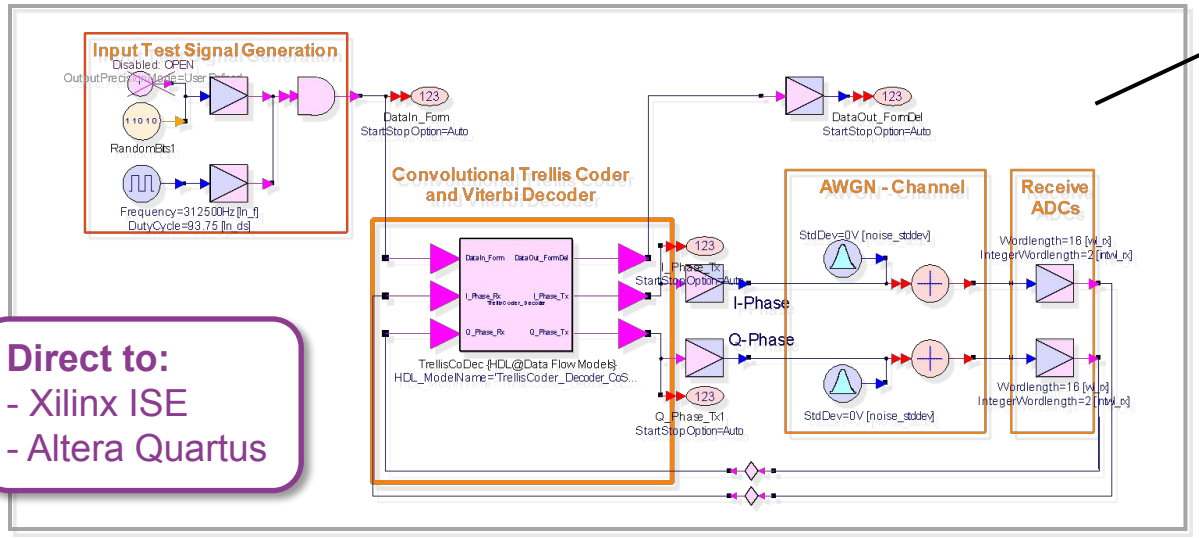
PART I: SystemVue Open FPGA Design Flow

Automatic HDL Code Generation

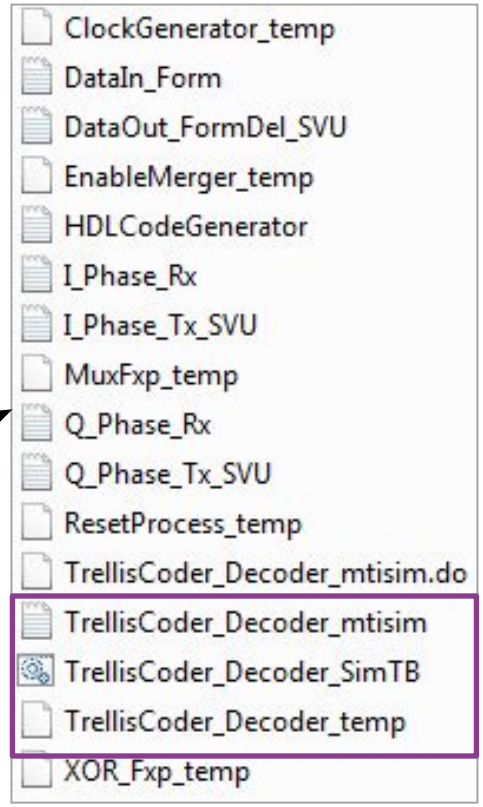
Provides path to rapid prototyping and hardware implementation

Generating hierarchical VHDL/Verilog allows path to rapid validation

- Fast realizations from schematic
- Generates HDL co-sim Test bench
- Easy model-based polymorphism
- Hardware ***target agnostic*** and support Xilinx/Altera

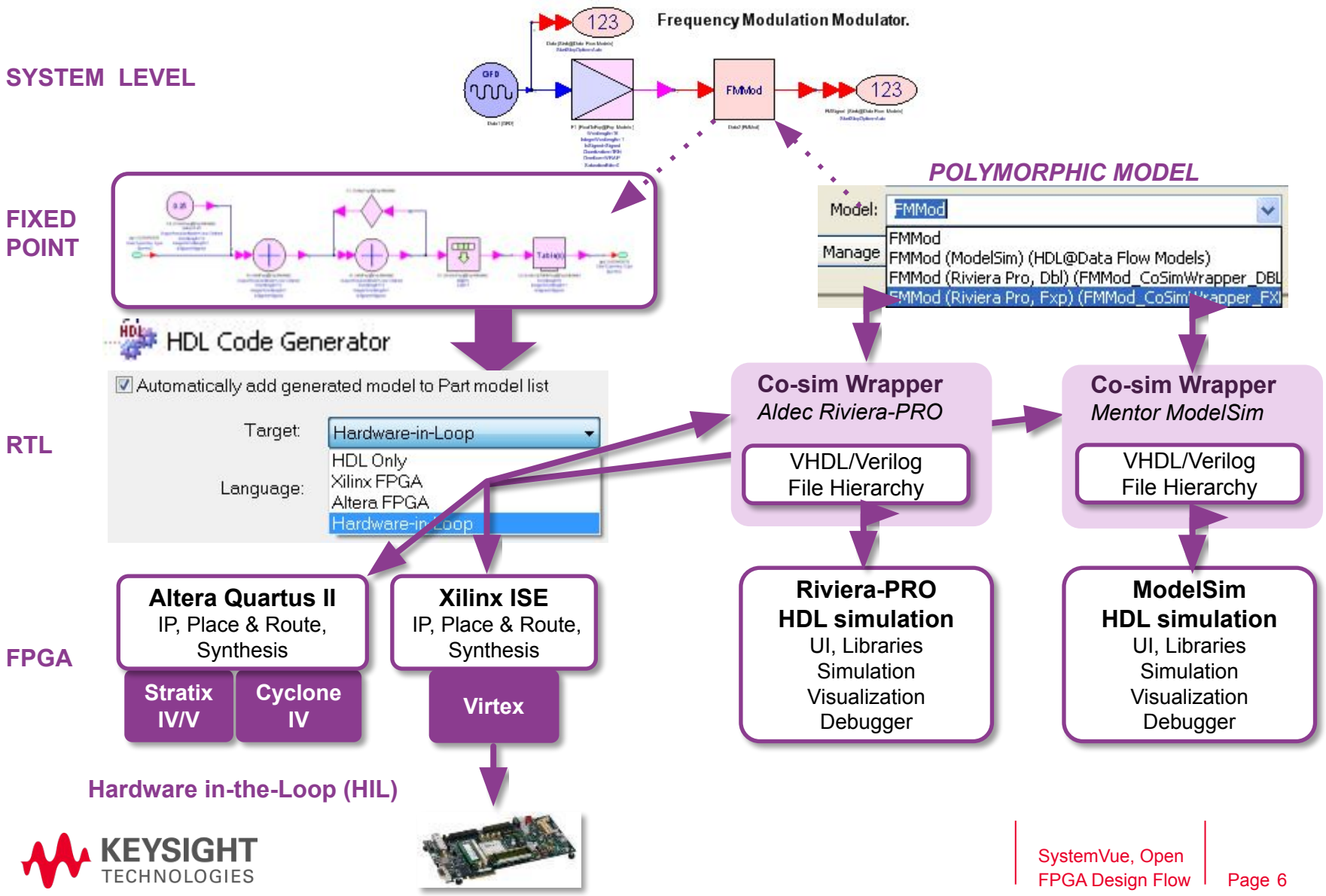


Direct to:
- Xilinx ISE
- Altera Quartus

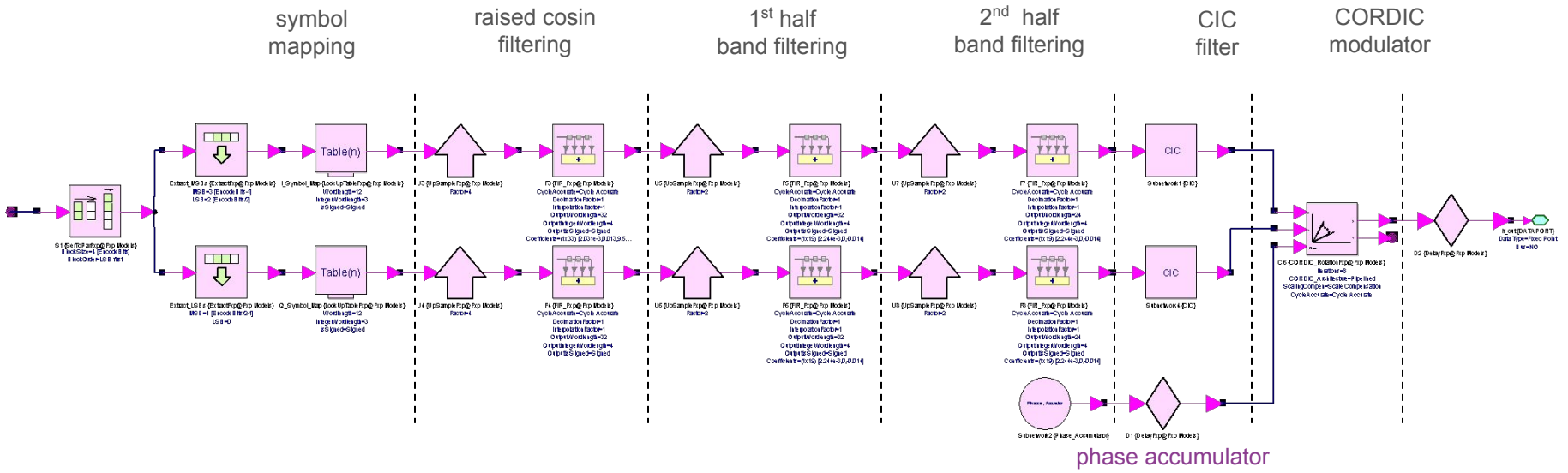


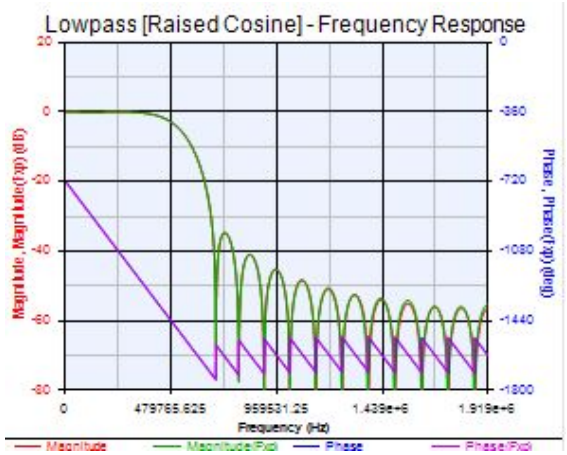
Test vector generation : ON

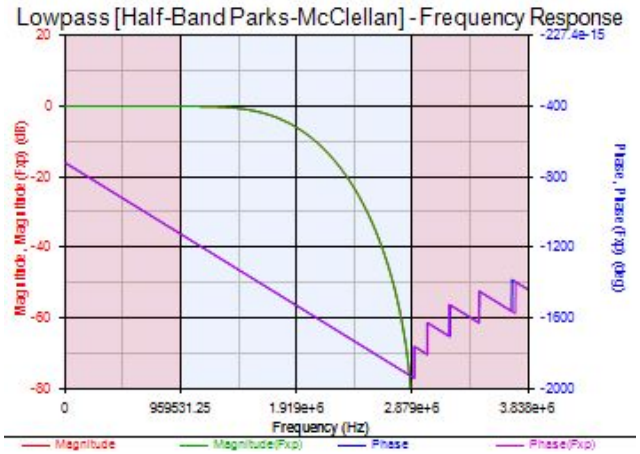
SystemVue FPGA Design Flow



Various fixed point blocks for hardware design

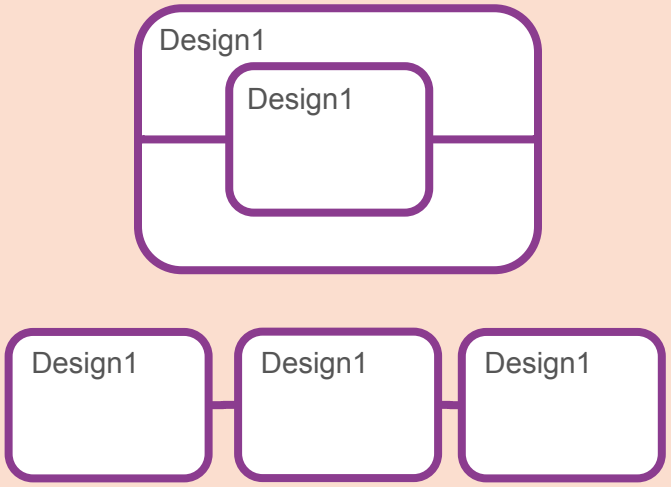




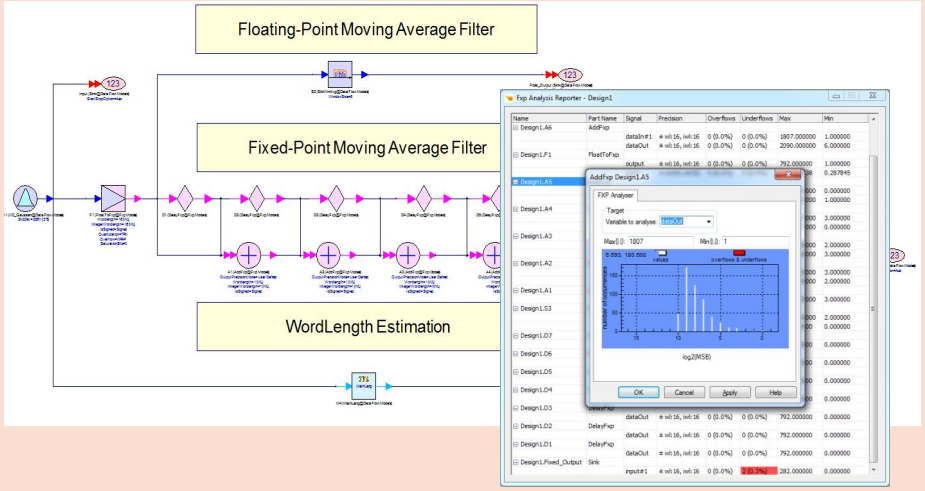


Design Optimization

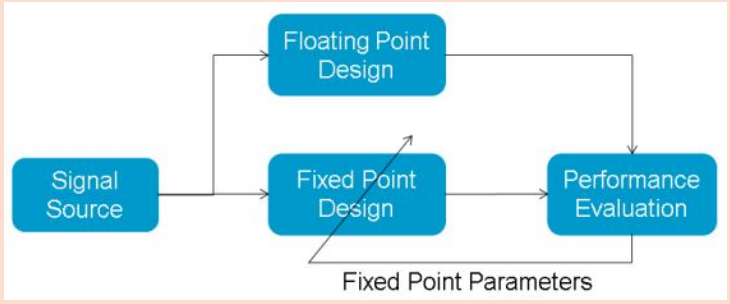
Recursive Graphical Design



Fixed Point Analysis



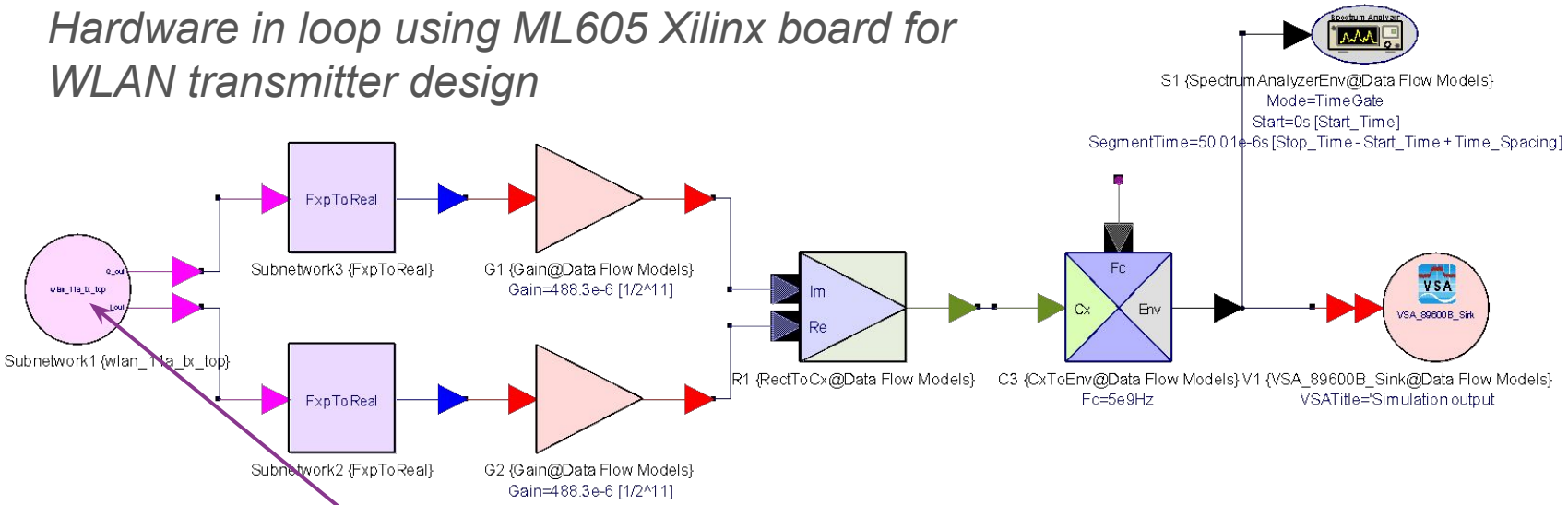
Sweep Analysis



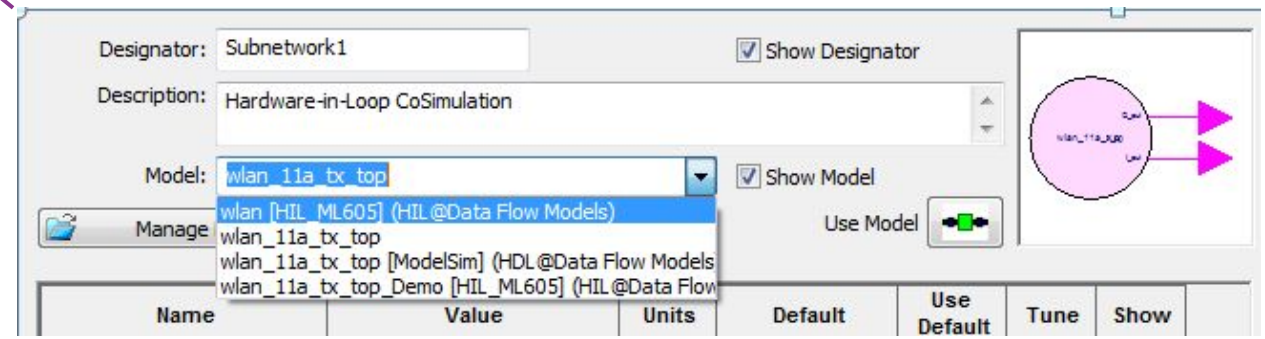
Demo One

SystemVue general FPGA design flow

Hardware in loop using ML605 Xilinx board for WLAN transmitter design



Native simulation
HDL co-simulation
HIL co-simulation



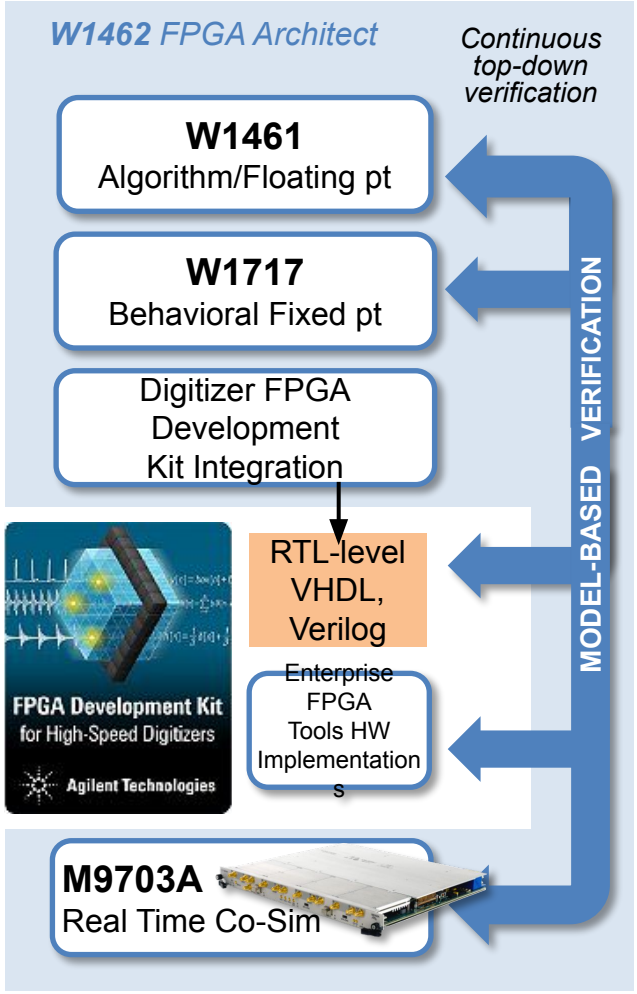
PART II: Integrated Design Flow for M9703A Digitizer

Integrated Hardware Design Flow for Digitizer

Realization of ***rapid real-time application development*** for high performance wideband digitizer

- Integrated flow for algorithm design & simulation, hardware design & implementation
- ***Custom algorithm*** design and software level simulation
- ***M9703A_Template*** design
- Hardware co-simulation with ***M9703A_CoSim*** model
- One push button approach for the ***bit file generation*** and FPGA ***programming***

MODEL-BASED DESIGN FLOW

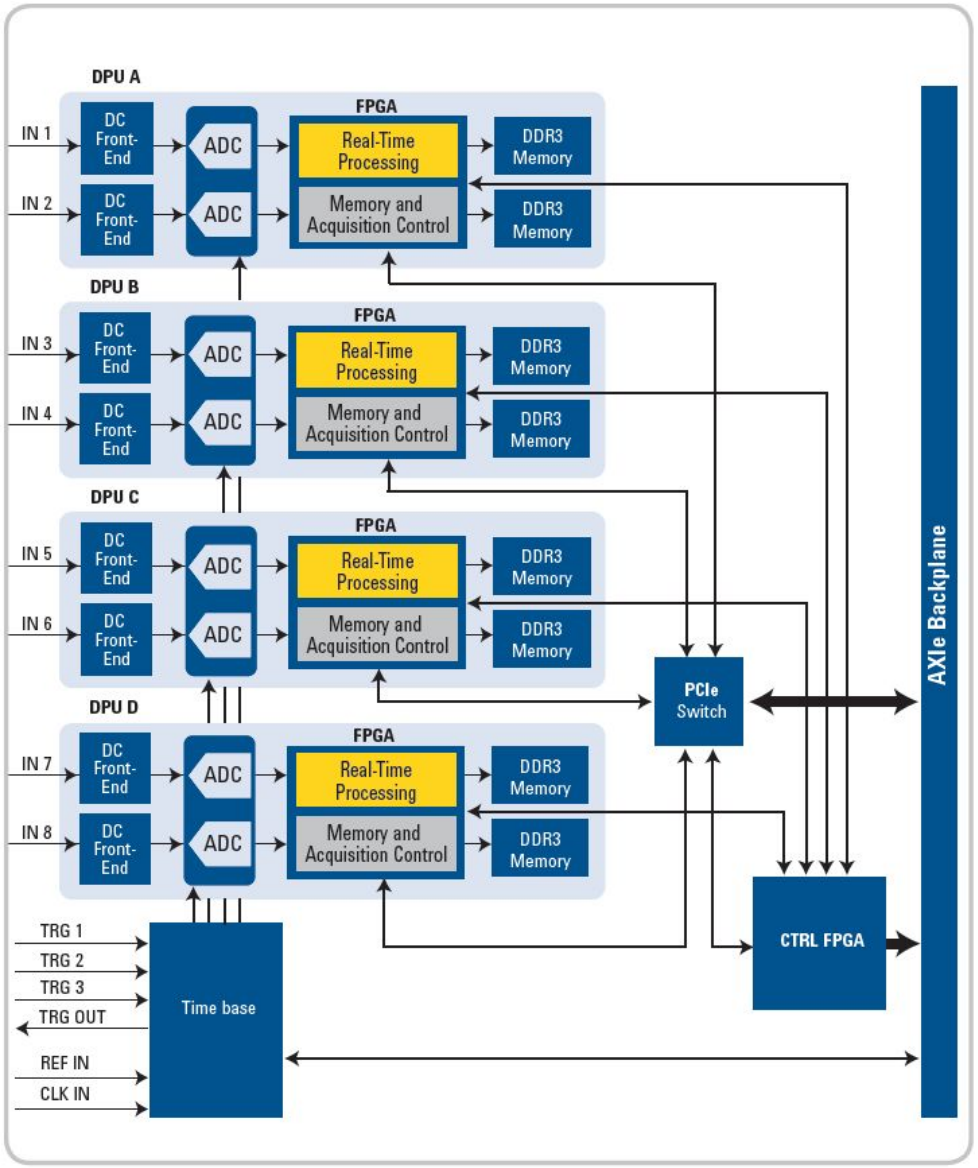


Key Benefits of the integrated design flow

- Early development of Firmware/Software APIs **before HW arrives**
- **Standard conforming** baseband stimulus and response metrology
- Simplify complex post analysis
- Overcome function test limitation of a timing based simulator
- Real world system level simulation

Overview of M9703A High Speed Digitizer

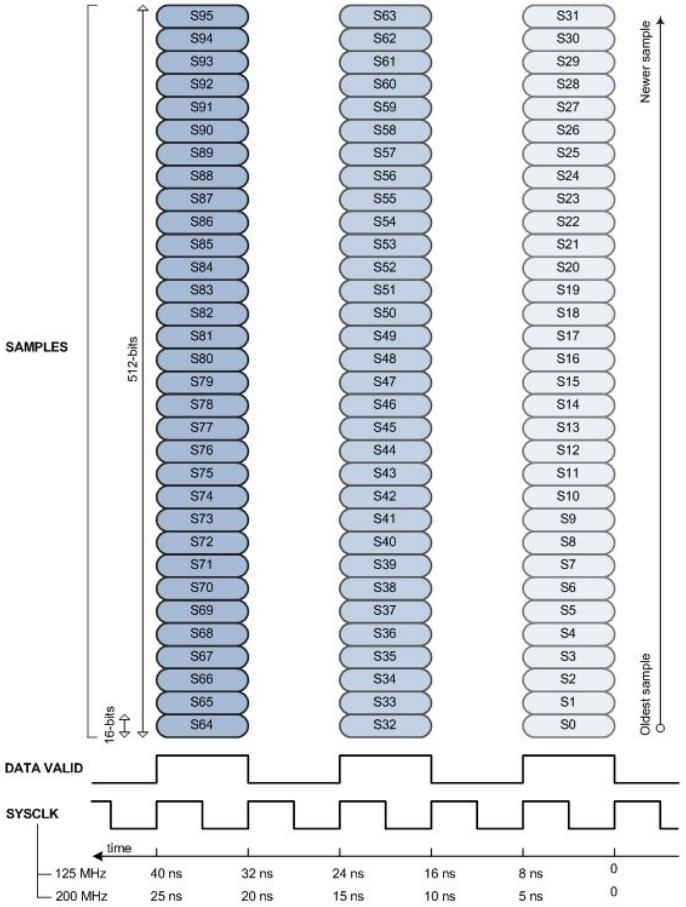
- 8 phase-coherent channels (4 when interleaving), 12-bit wideband digital digitizer/receiver
- Up to 1.6 GS/s for 8 channels or up to 3.2 GS/s for 4 channels (interleaving mode)
- Input frequency range of DC to 650 MHz (can be extended to DC to 2GHz with –F10 option)
- AXIe standard based
- Application fields: multi-channel applications in advanced aerospace & defense, RF communications and physics.



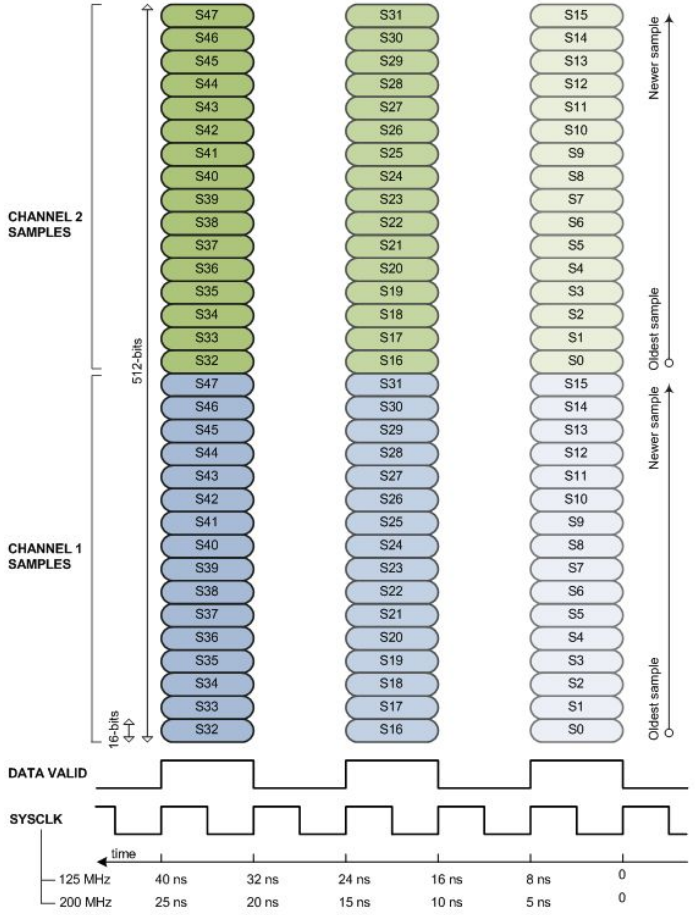
KEYSIGHT TECHNOLOGIES

DPU FPGA user core ADC input format

1-Ch mode (3.2GS/s)



2-Ch mode (1.6GS/s)



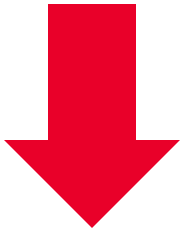
KEYSIGHT TECHNOLOGIES

M9703A FPGA Design Flow

Overview

Design entry and software simulation

M9703A FPGA programming file auto generation



M9703A instrument co-simulation with SystemVue

M9703A FPGA Design Flow

Overview

Design entry and software simulation

M9703A FPGA programming file auto generation

M9703A instrument co-simulation with SystemVue

M9703A FPGA Design Flow

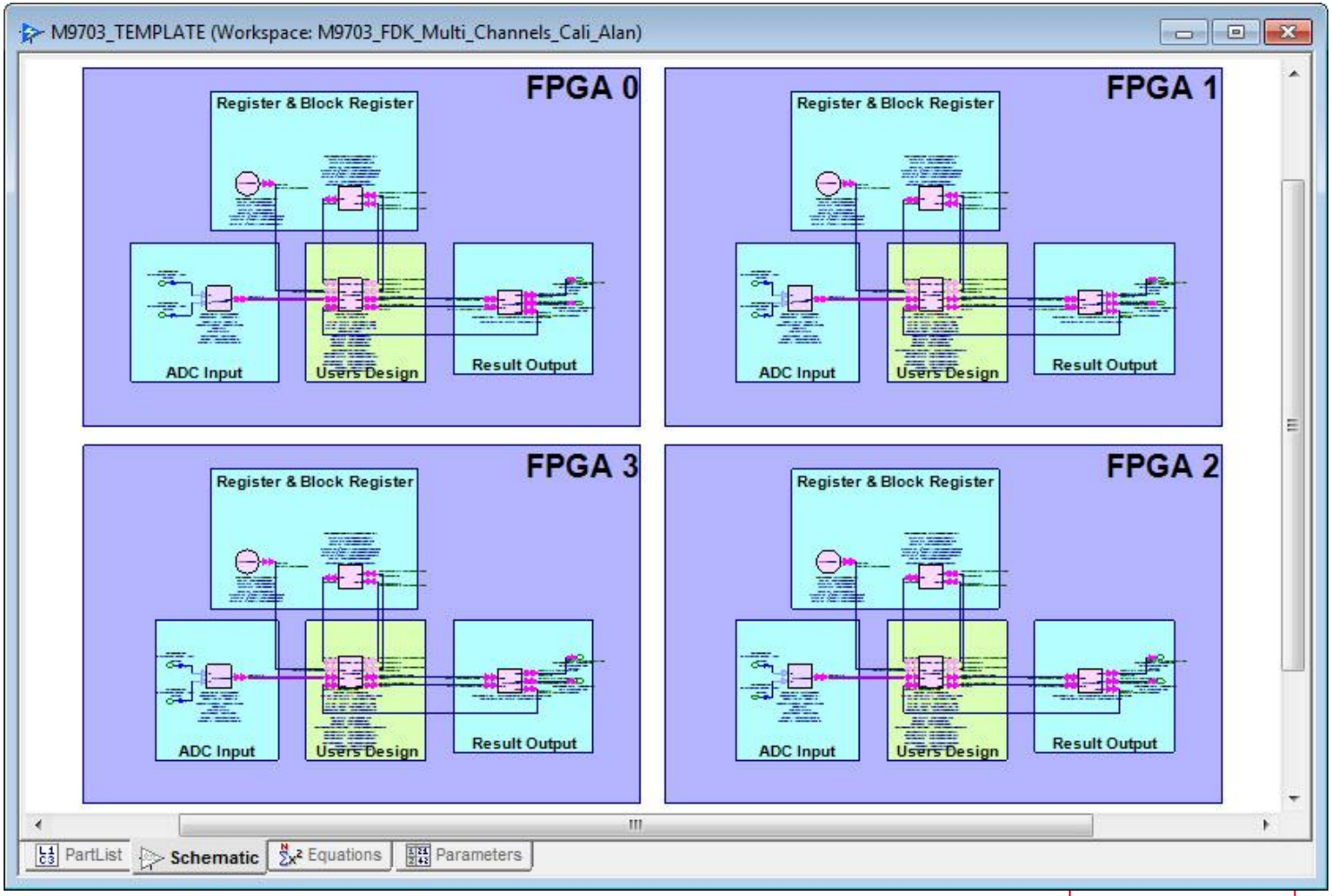
Design entry and software simulation

Top Level Design in SystemVue

- **C++ simulation or C++/HDL mixed simulation if HDL codes or Xilinx IP cores are involved in users' design**
- **Rich resources for testbench creation**
- **Dynamic Data Flow for extracting valid output of users' design**

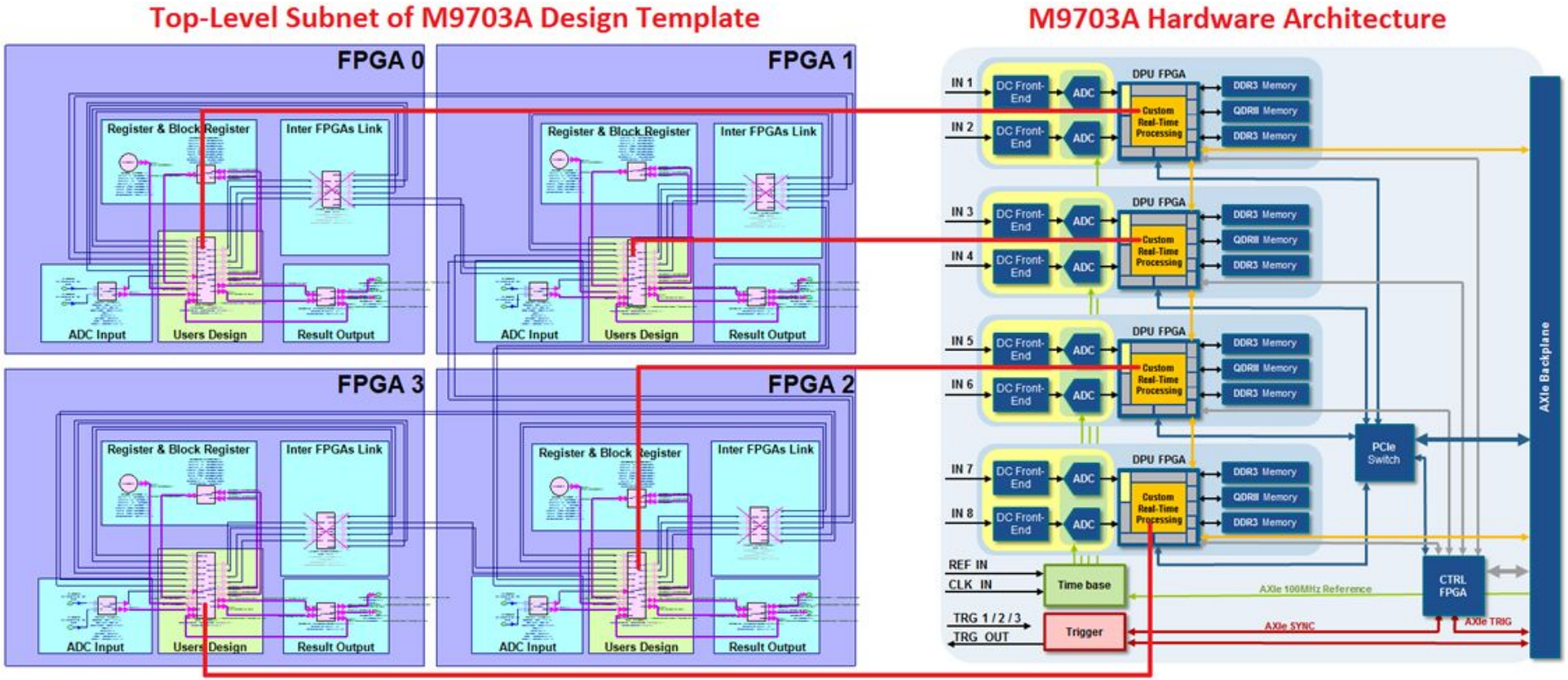
M9703A FPGA Design Flow

Design entry and software simulation



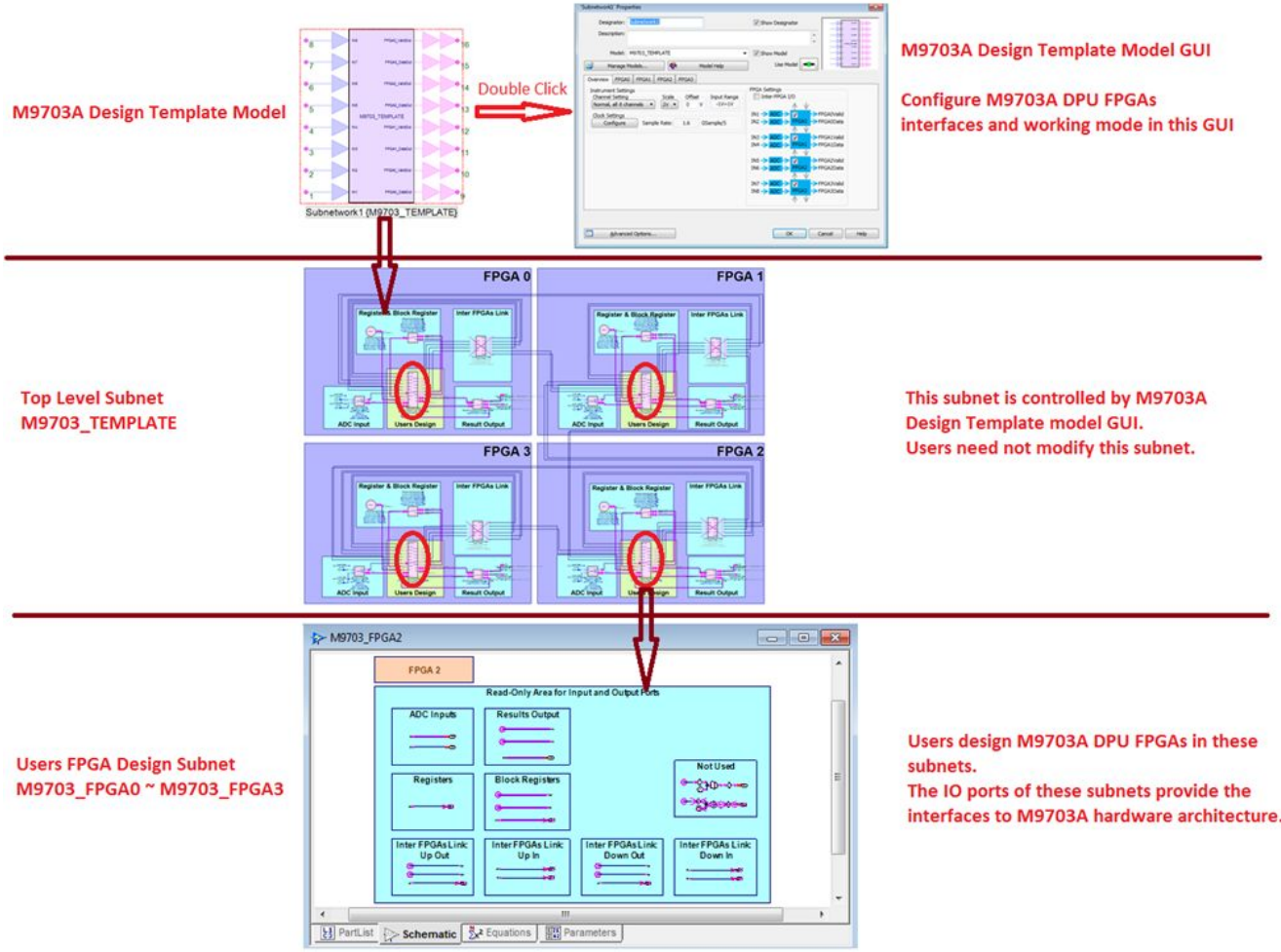
M9703A FPGA Design Flow

Design entry and software simulation



M9703A FPGA Design Flow

Design entry and software simulation



M9703A FPGA Design Flow

Overview

Design entry and software simulation

M9703A FPGA programming file auto generation

M9703A instrument co-simulation with SystemVue

M9703A FPGA Design Flow

Overview

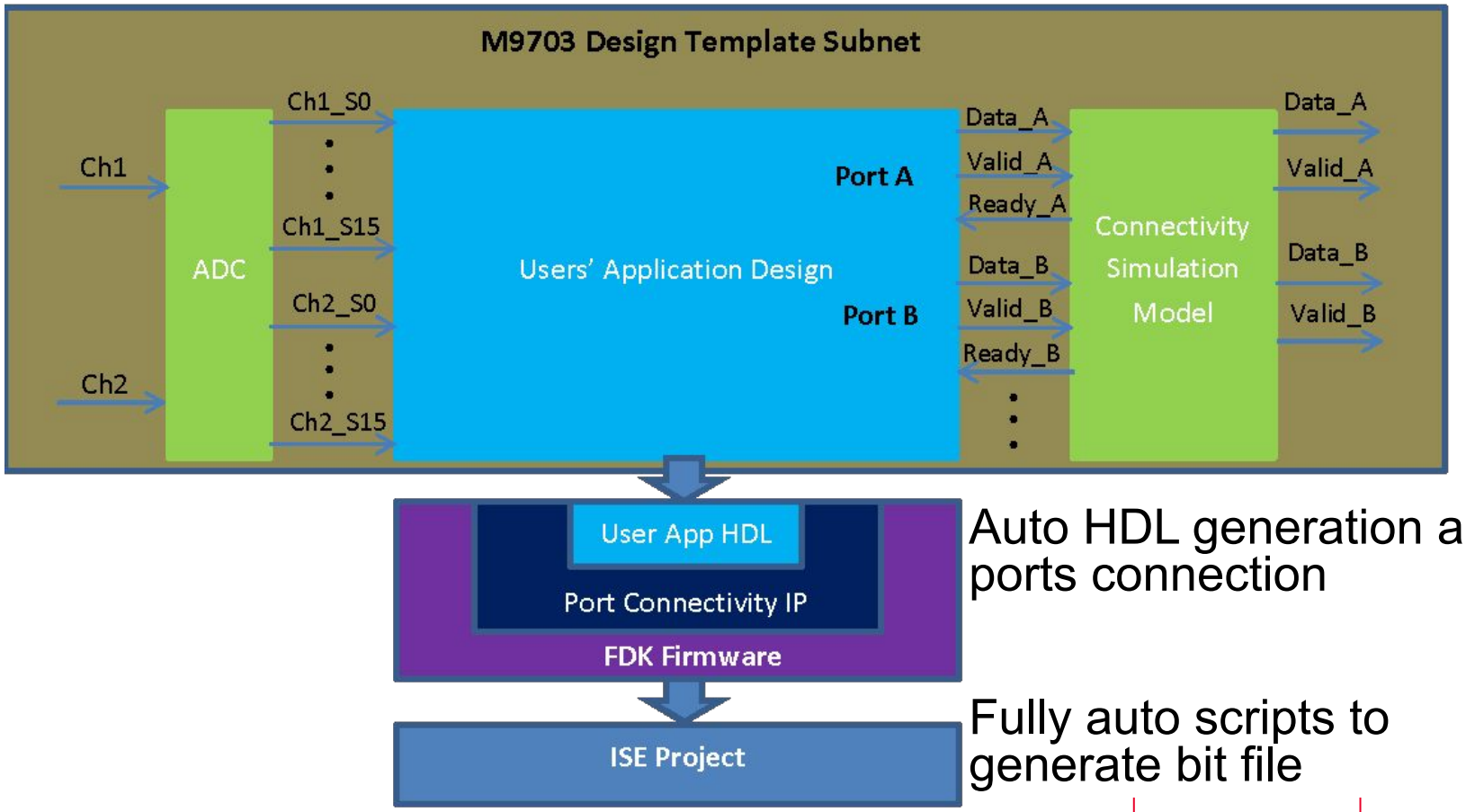
Design entry and software simulation

M9703A FPGA programming file auto generation

M9703A instrument co-simulation with SystemVue

M9703A FPGA Design Flow

M9703A FPGA programming file auto generation



Auto HDL generation and ports connection

Fully auto scripts to generate bit file

M9703A FPGA Design Flow

Overview

Design entry and software simulation

M9703A FPGA programming file auto generation

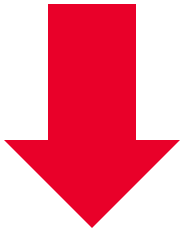
M9703A instrument co-simulation with SystemVue

M9703A FPGA Design Flow

Overview

Design entry and software simulation

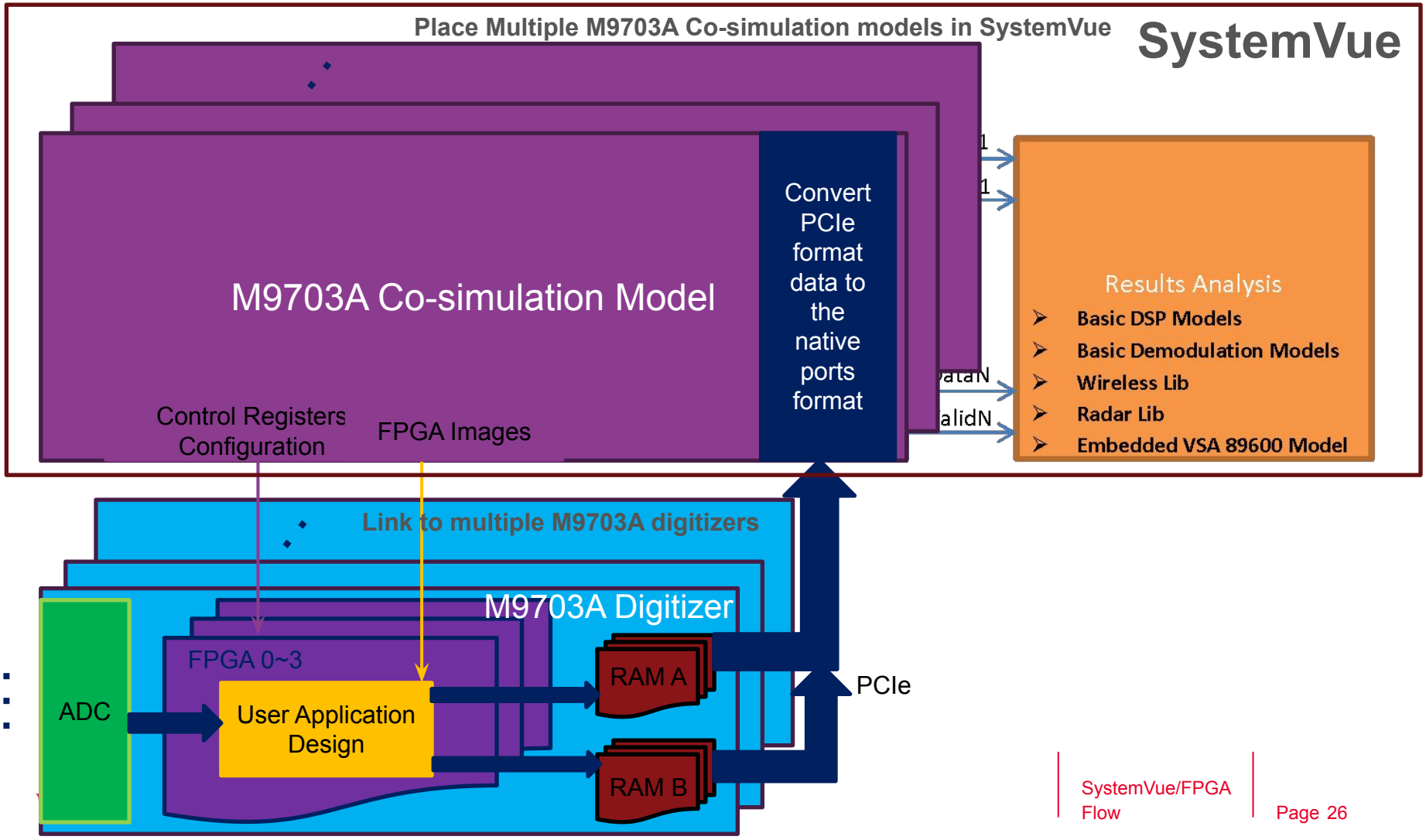
M9703A FPGA programming file auto generation



M9703A instrument co-simulation with SystemVue

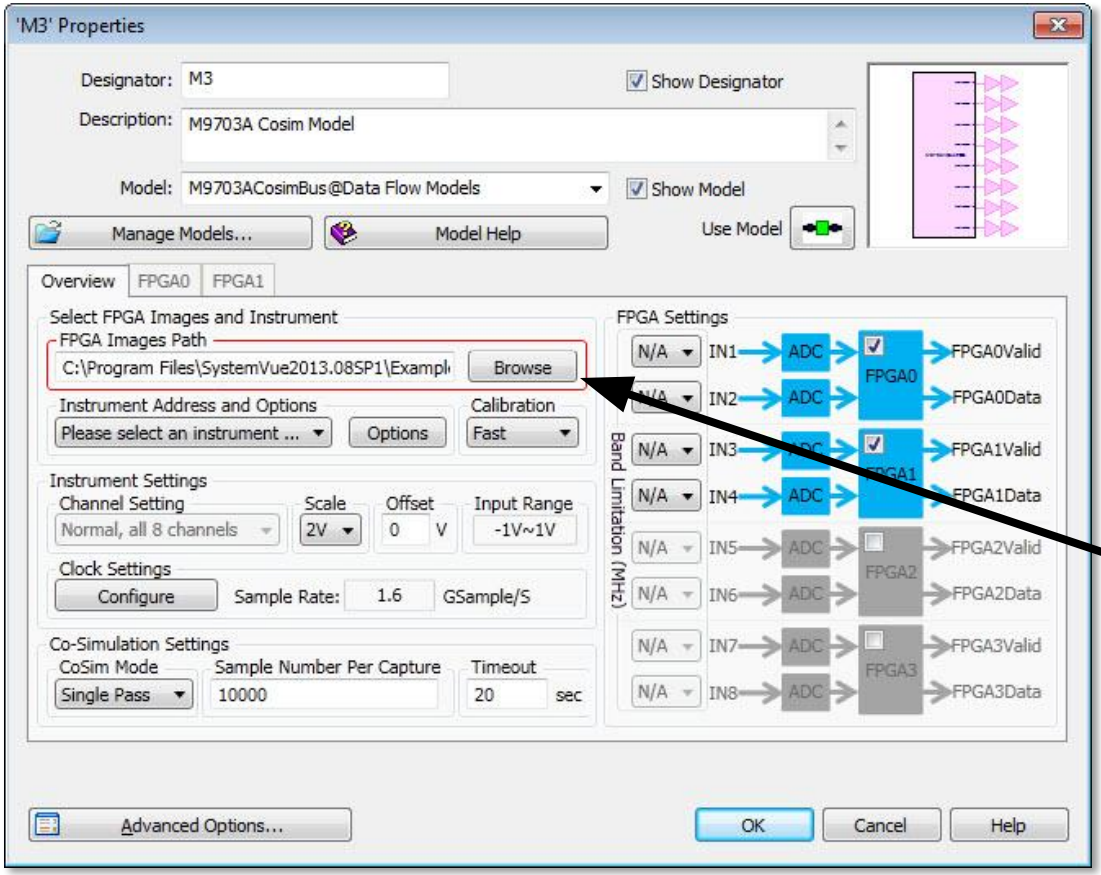
M9703A FPGA Design Flow

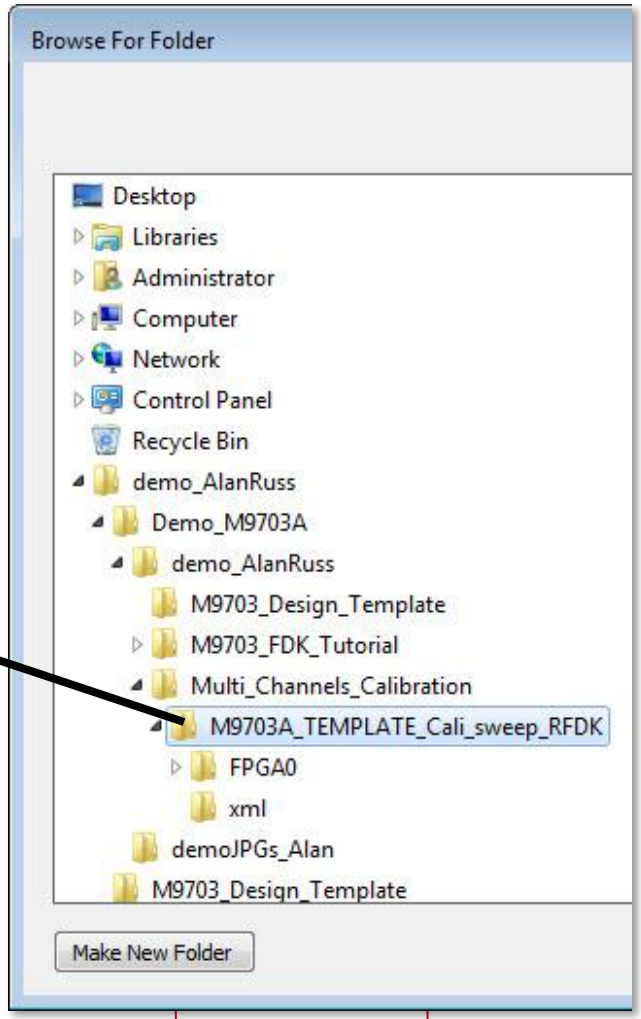
M9703A instrument co-simulation with SystemVue



M9703A FPGA Design Flow

M9703A instrument co-simulation with SystemVue

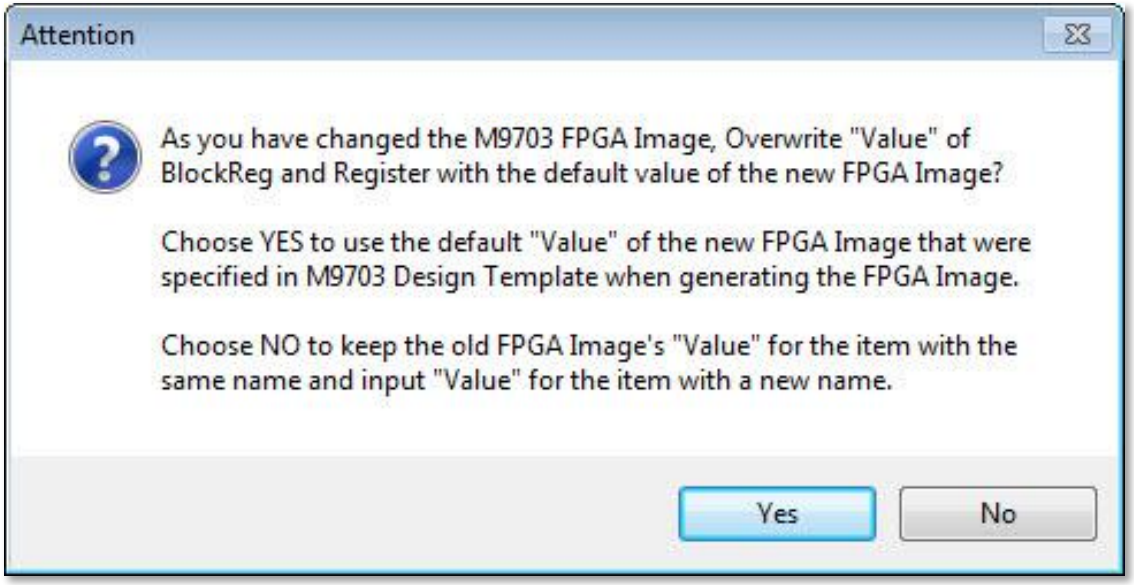




KEYSIGHT TECHNOLOGIES

M9703A FPGA Design Flow

M9703A instrument co-simulation with SystemVue



Realistic Digitizer Application Example

Phase & magnitude correction for multi-channel digitizer

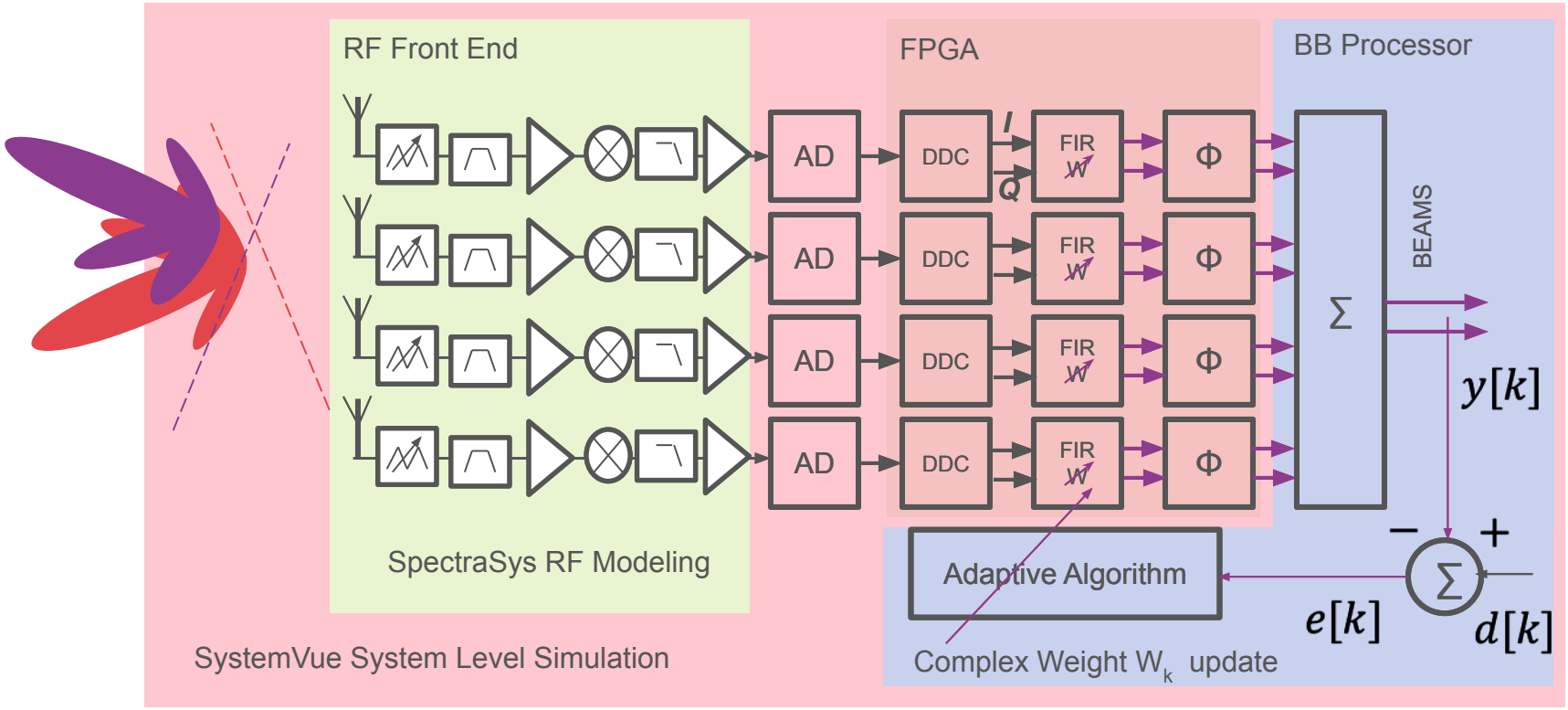


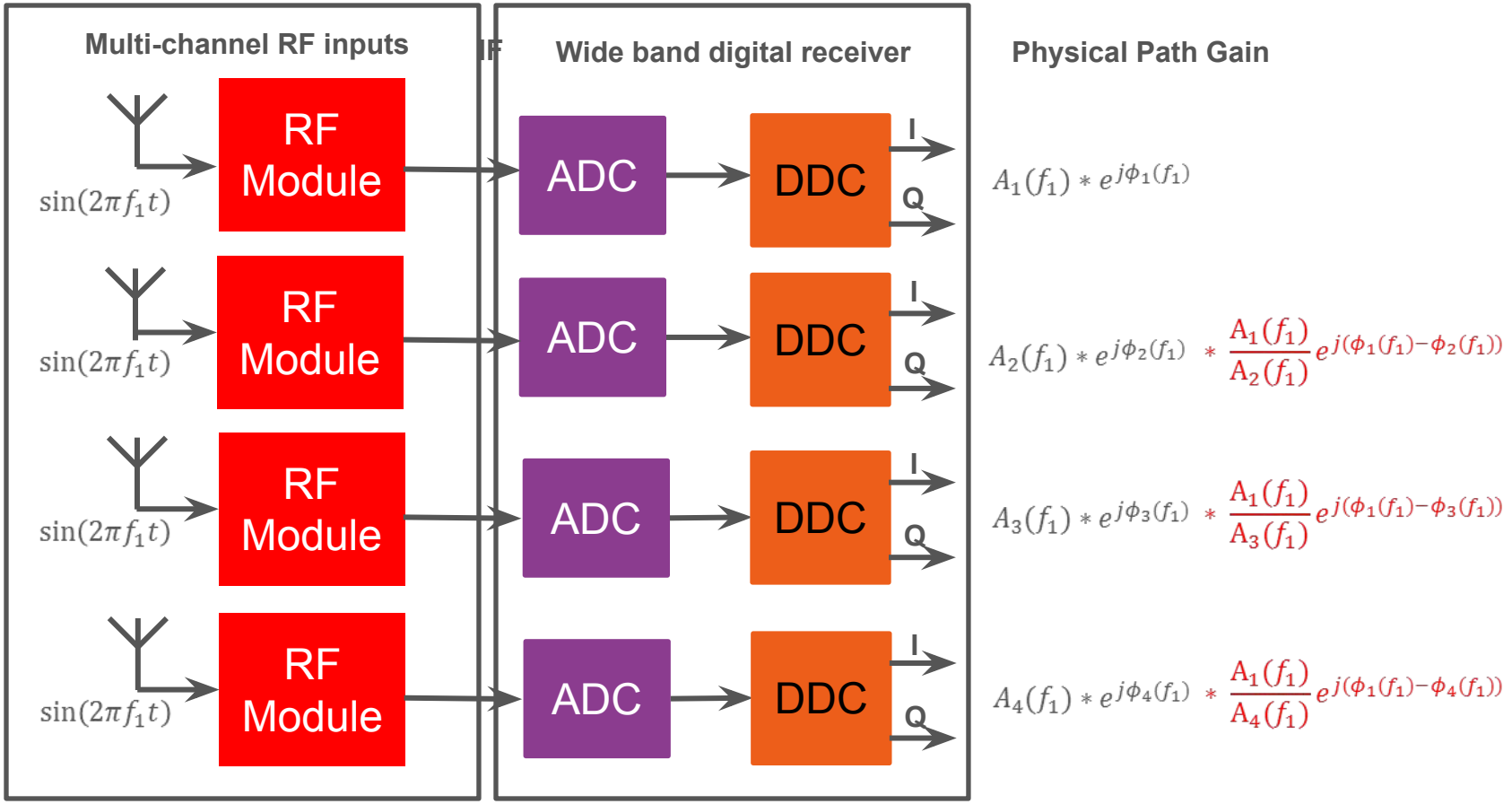
Figure 1. Adaptive Digital Beam Forming Signal Processing

- Hardware implementation for digital down conversion and filtering
- Adaptive beam forming algorithm to update weighting vector on the fly

Realistic Digitizer Application Example

Phase & magnitude correction for multi-channel digitizer

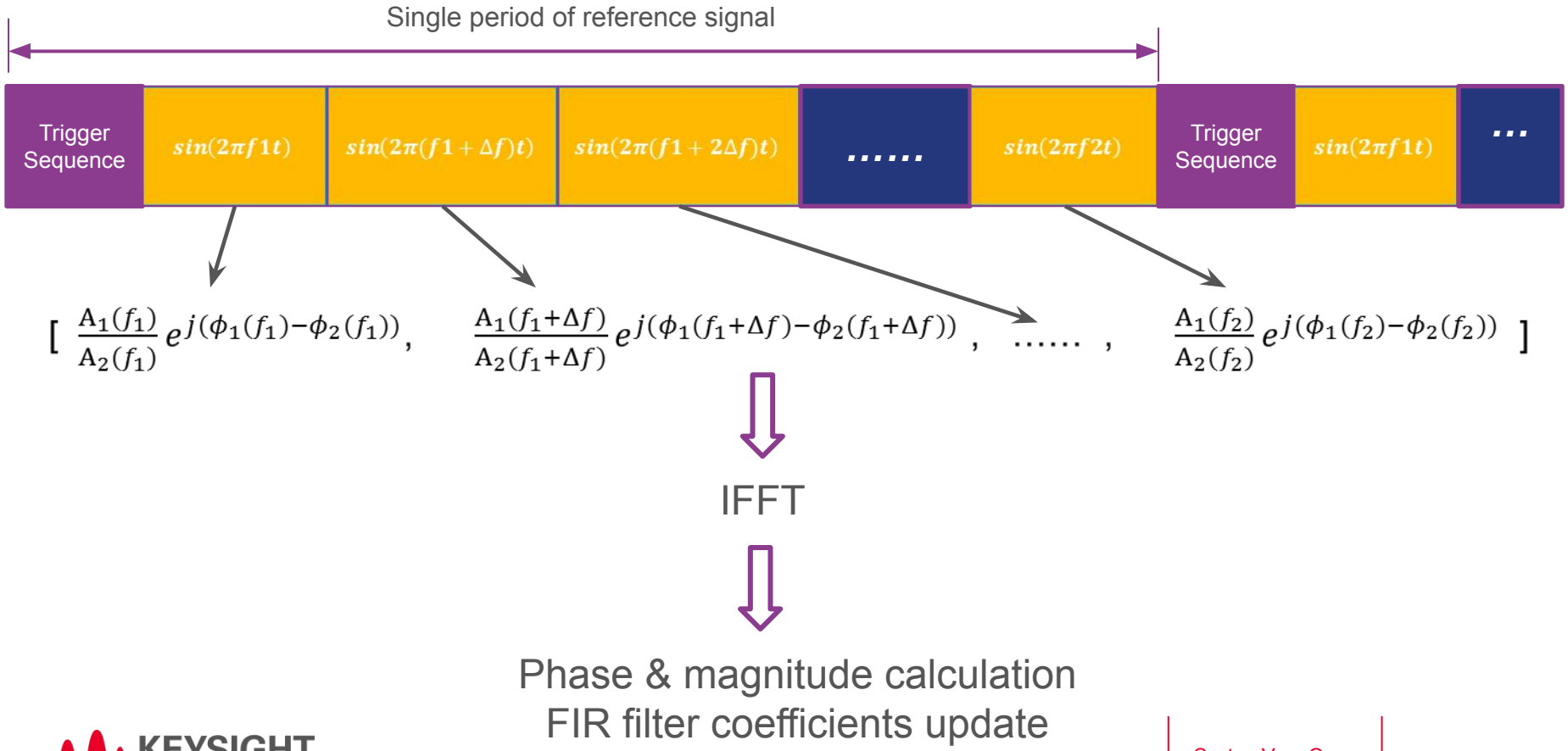
– What is difference between channels?



Realistic Digitizer Application Example

Phase & magnitude correction for multi-channel digitizer

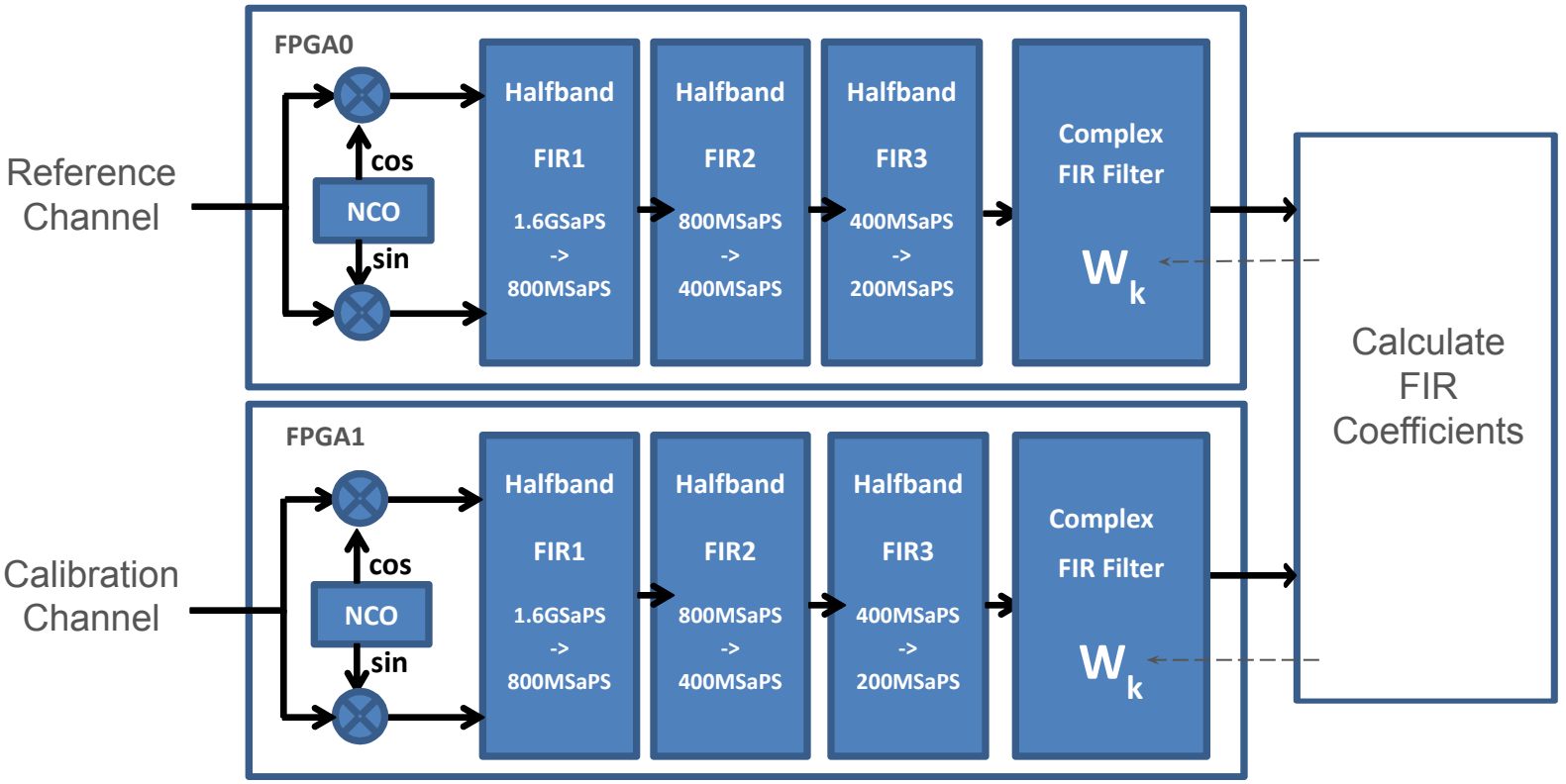
– Signal processing



Realistic Digitizer Application Example

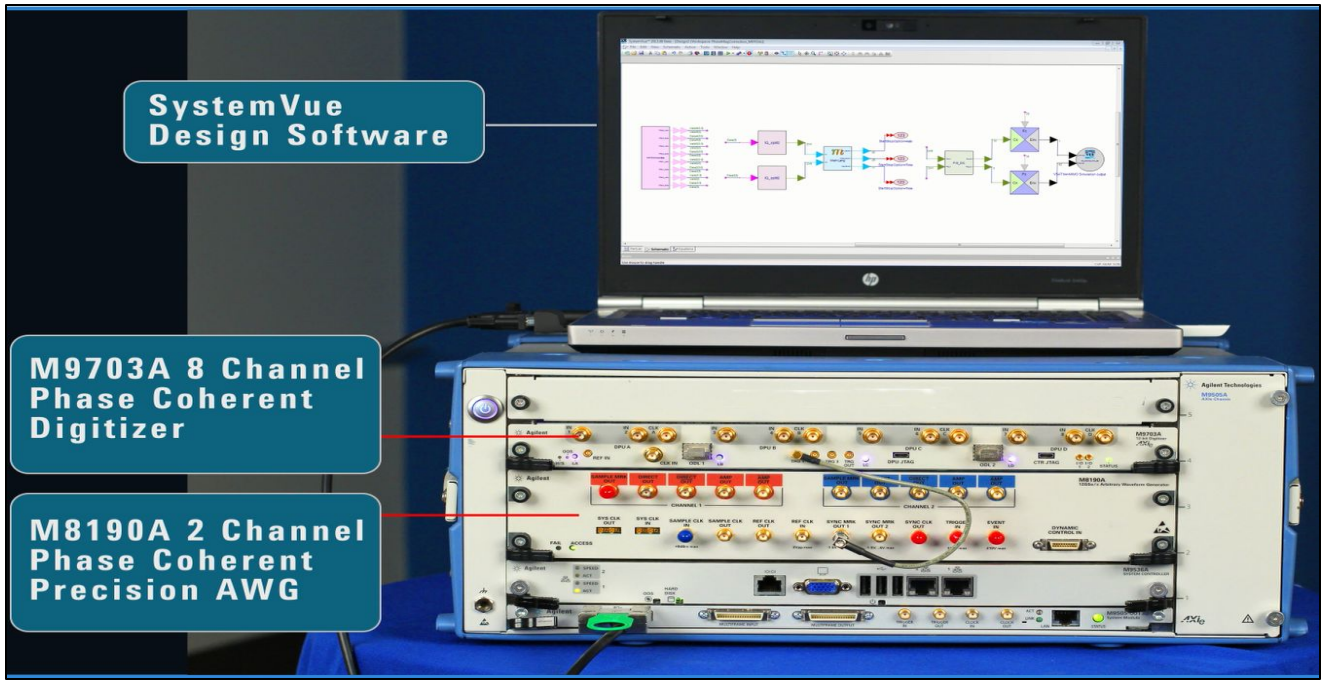
Phase & magnitude correction for multi-channel digitizer

– Block diagram



Realistic Digitizer Application Example

Phase & magnitude correction for multi-channel digitizer



For Simple Video Demo:

- YouTube Video : https://www.youtube.com/watch?v=wrQxkgOPQek

Realistic Digitizer Application Example

Phase & magnitude correction for multi-channel digitizer

Required Hardware:

- M9703 with FDK option to enable its FPGA programming capability
- M9505 AXIe chassis
- M9036 AXIe embedded controller or external PC + PCI Express cable
- M8190A AWG
- 1x2 RF Splitter and RF cables

Required Software:

- SystemVue 2015.01 or later.
- Keysight IO Library
- Keysight MD1 High-Speed Digitizer Instrument Drivers and Soft Front Panel
- Xilinx ISE: version 14.4 or later (This software required only when you want to re-generate bit file by yourself. Bit file already generated and included in demo example)
- 89600 VSA software

Demo II Setup Guide (…What We Did)

Live Demo

M9703A FDK firmware update and License:

- Send serial number of your M9703A demo unit to ZARETTI,CHRISTOPHE (K-Switzerland,ex1) christophe_zaretti@keysight.com

Step 1. Ensure that the required software is installed.

- Install the common software required below, and then item that applies to your upgrade option
  a. Agilent IO Libraries Suite (IOLS)
  Version 16.3 update 2 (or higher) is required for this option
  b. MD1 software version 1.13.7 (or higher).
  1. Available from the Keysight website at : www.keysight.com/find/M9703A
  2. After installation you must reboot the controller and allow the instrument drivers to reinstall.

Step 2. Transfer the new license file to EEPROM

a. Copy the *M9703A_US00075291_DDC_FDK.epr* license file attached to a local folder.
b. Launch the application 'AcqEepromProg.exe', which may be found:
o 32-bit OS: C:\Program Files\Agilent\MD1\bin
o 64-bit OS: C:\Program Files (x86)\Agilent\MD1\bin
c. Select the *M9703A_ US00075291_DDC_FDK.epr* file copied above.
d. If more than one digitizer is present, be sure to select the correct one from the list
e. The EEPROM upgrade process should only take a few seconds.
f. Close the application.

Demo II Setup Guide (…What We Did)

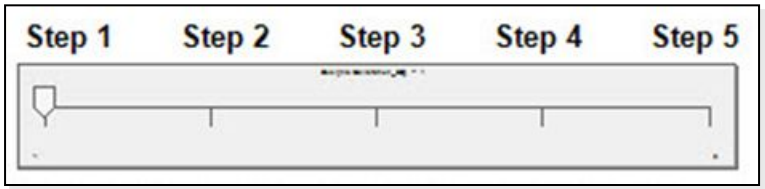
Live Demo

Step 3. Verify the operation of the option upgrade

- You can try to load the default FDK firmware file with your test application using strInitOptions = "Simulate=false, DriverSetup= CAL=0, UserDpuA=M9703ADPULX2FDK.bit, UserDpuB=M9703ADPULX2FDK.bit, UserDpuC=M9703ADPULX2FDK.bit, UserDpuD=M9703ADPULX2FDK.bit, Trace=false", the custom FDK firmware will be loaded.

Realistic Digitizer Application Example

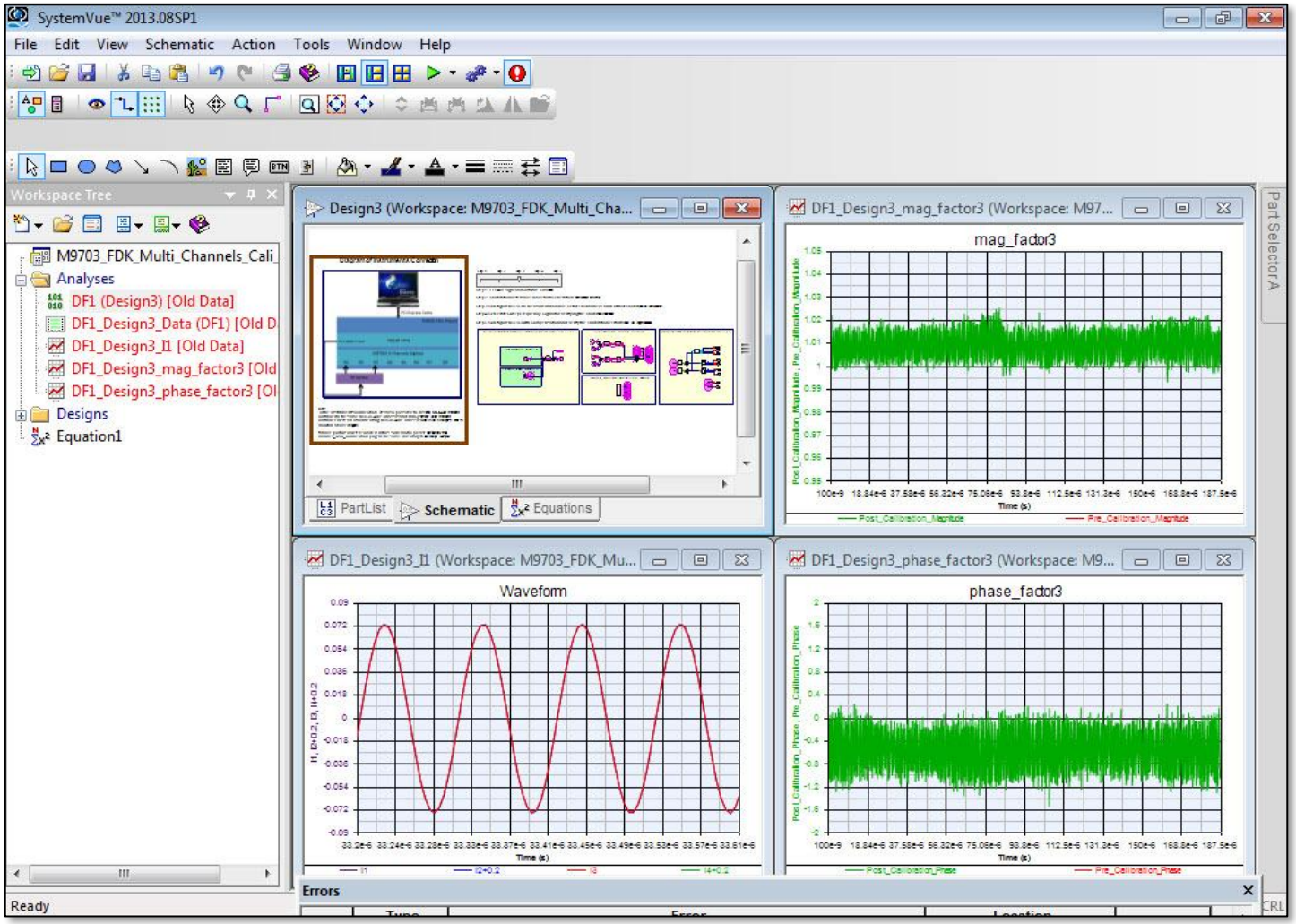
Phase & magnitude correction for multi-channel digitizer



1. SW simulation step only (no HW)
2. Source M8190 configuration
3. M9703 measurement + calculate filter coefficients from reference channel (In1)
4. Source M8190 signal generation
5. M9703 compensation applied to target channel (In3)

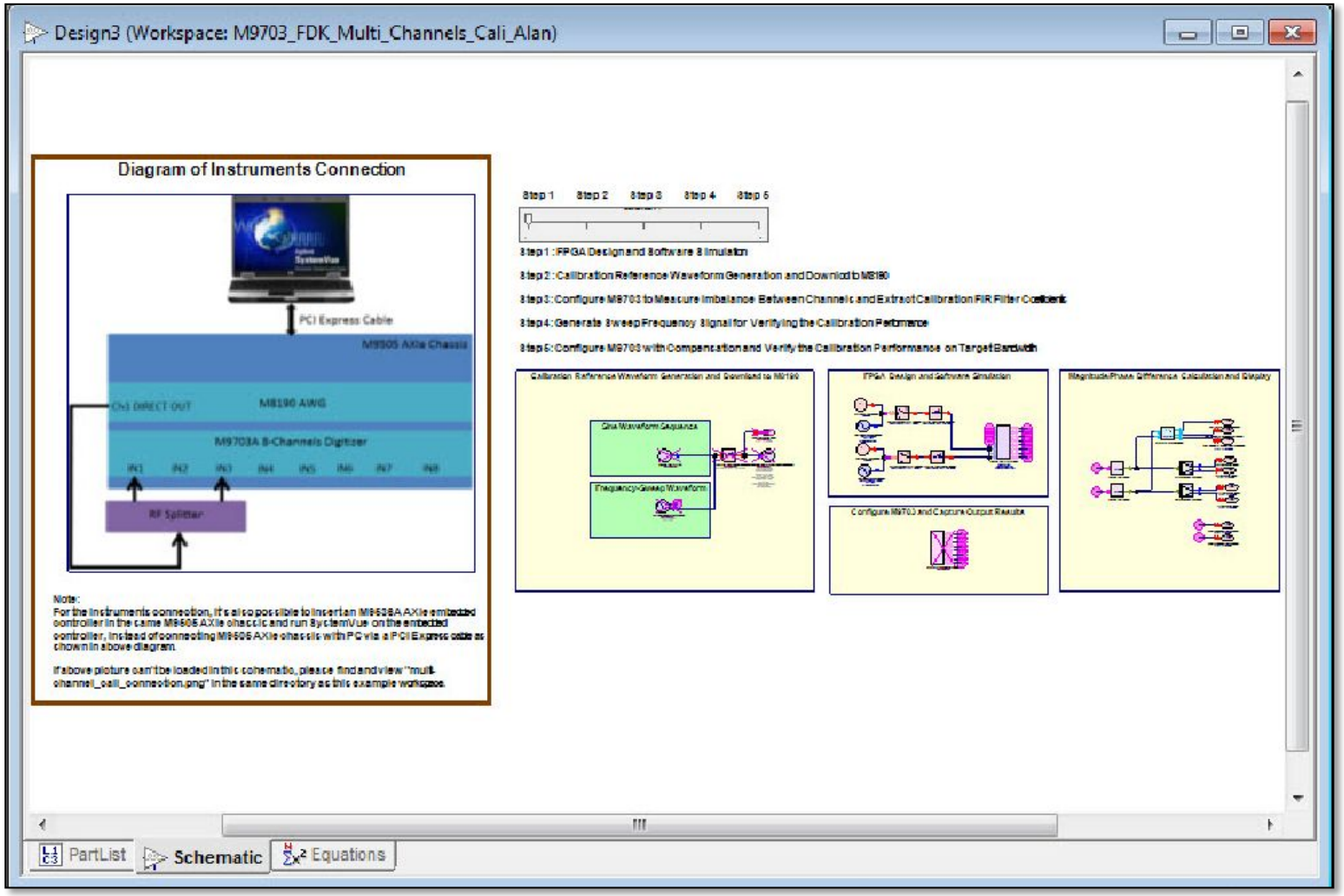
Demo II Setup Guide

SystemVue Design – Signal Imbalance Correction



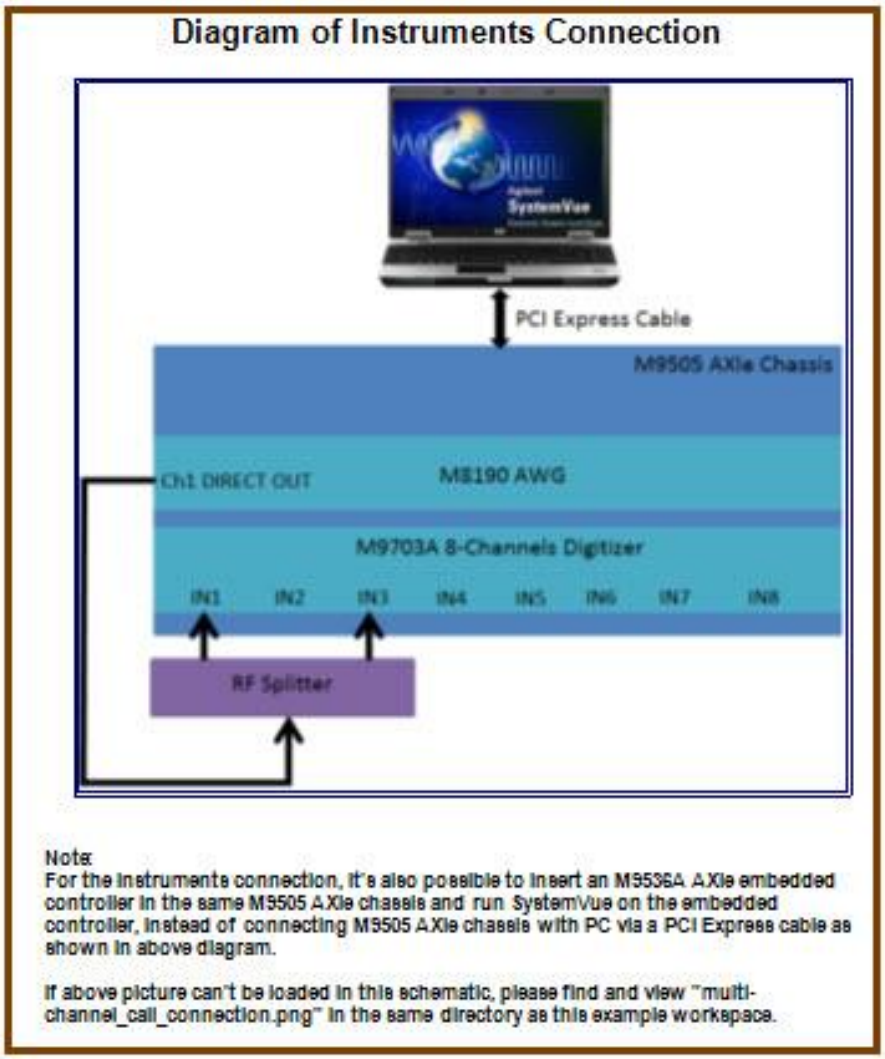
Demo II Setup Guide

SystemVue Design – Top Level Workspace



Demo II Setup Guide

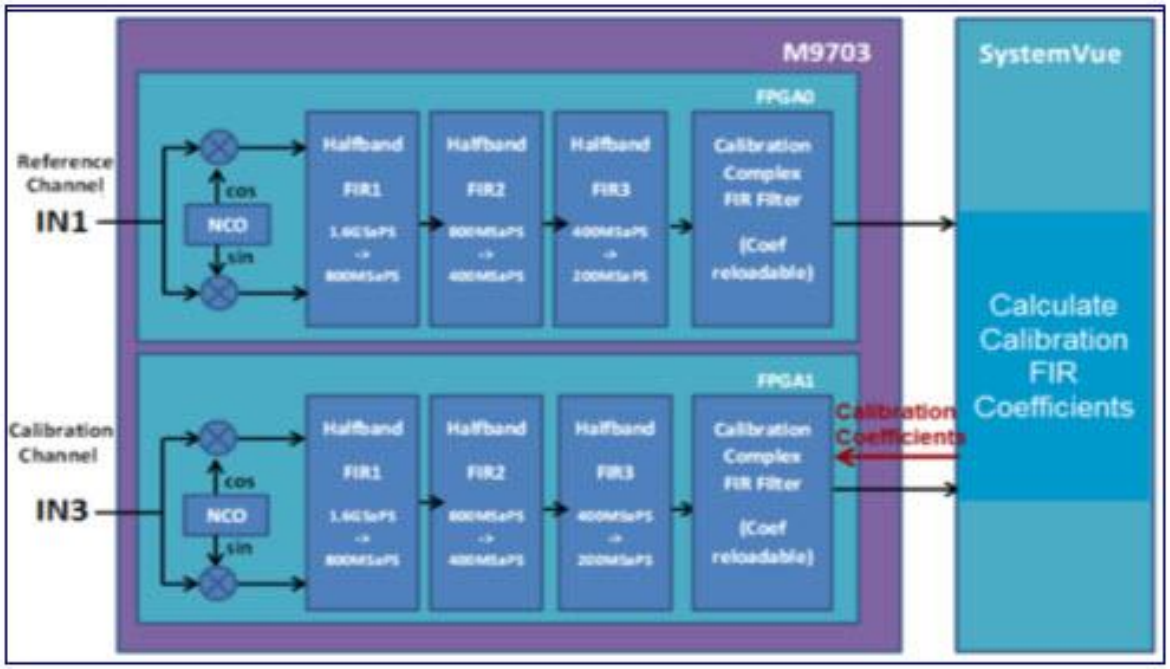
SystemVue Design – Chassis Configuration (+External Splitter)



Demo II Setup Guide

SystemVue Design – M9703A Configuration

Diagram of M9703A FPGA0 and FPGA1 Design

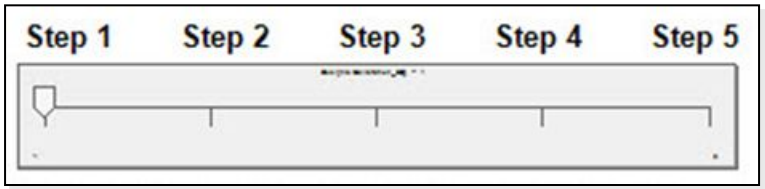


Note:
The FPGA designs and generated FPGA programming files of FPGA0 and FPGA1 are the same. But we can configure different FIR coefficents to the defined BlockRegisters in FPGA0 and FPGA1. Then we can bypass the calibration FIR filter for FPGA0 and compensate IQ imballance via FPGA1's calibration FIR filter.

If above picture can't be loaded in this schematic, please find and view "multi-channel_cali_FPGA_arch.png" in the same directory as this example workspace.

Demo II Setup Guide

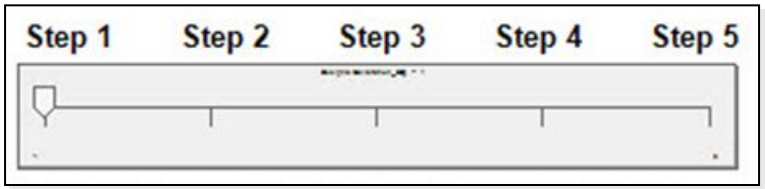
SystemVue Design – 5 Step Signal Correction



1. SW simulation step only (no HW)
2. Source M8190 configuration
3. M9703 measurement + calculate filter coefficients from reference channel (In1)
4. Source M8190 signal generation
5. M9703 compensation applied to target channel (In3)

Demo II Setup Guide

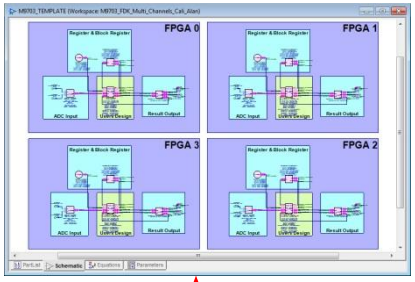
*Cosim **Step 1** – SystemVue Design Only*



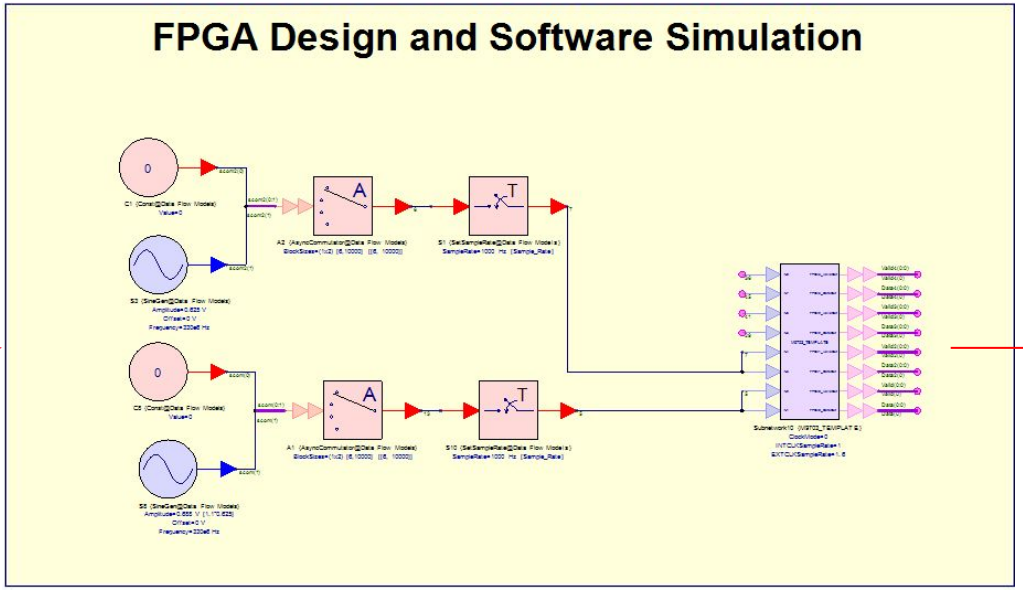
1. SW simulation step only (no HW)
2. Source M8190 configuration
3. M9703 measurement + calculate filter coefficients from reference channel (In1)
4. Source M8190 signal generation
5. M9703 compensation applied to target channel (In3)

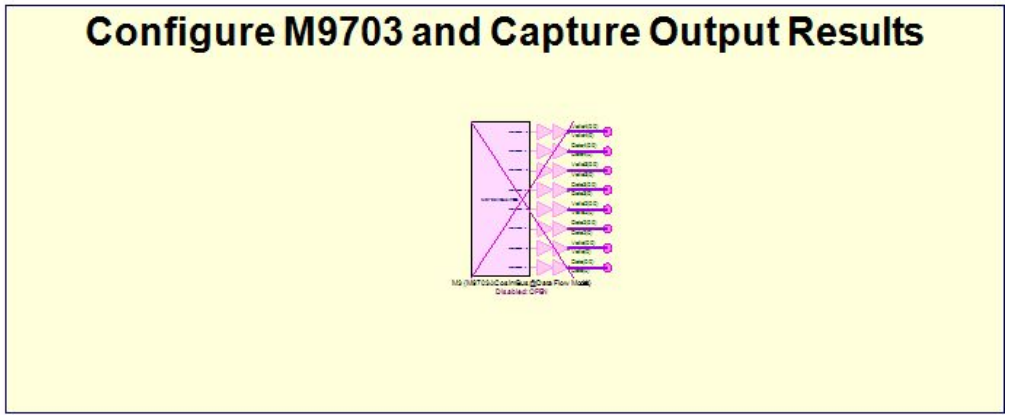
Demo II Setup Guide

*Cosim **Step 1** (no HW) – M9703A Target Setup*



Cosim Only
(no HW)

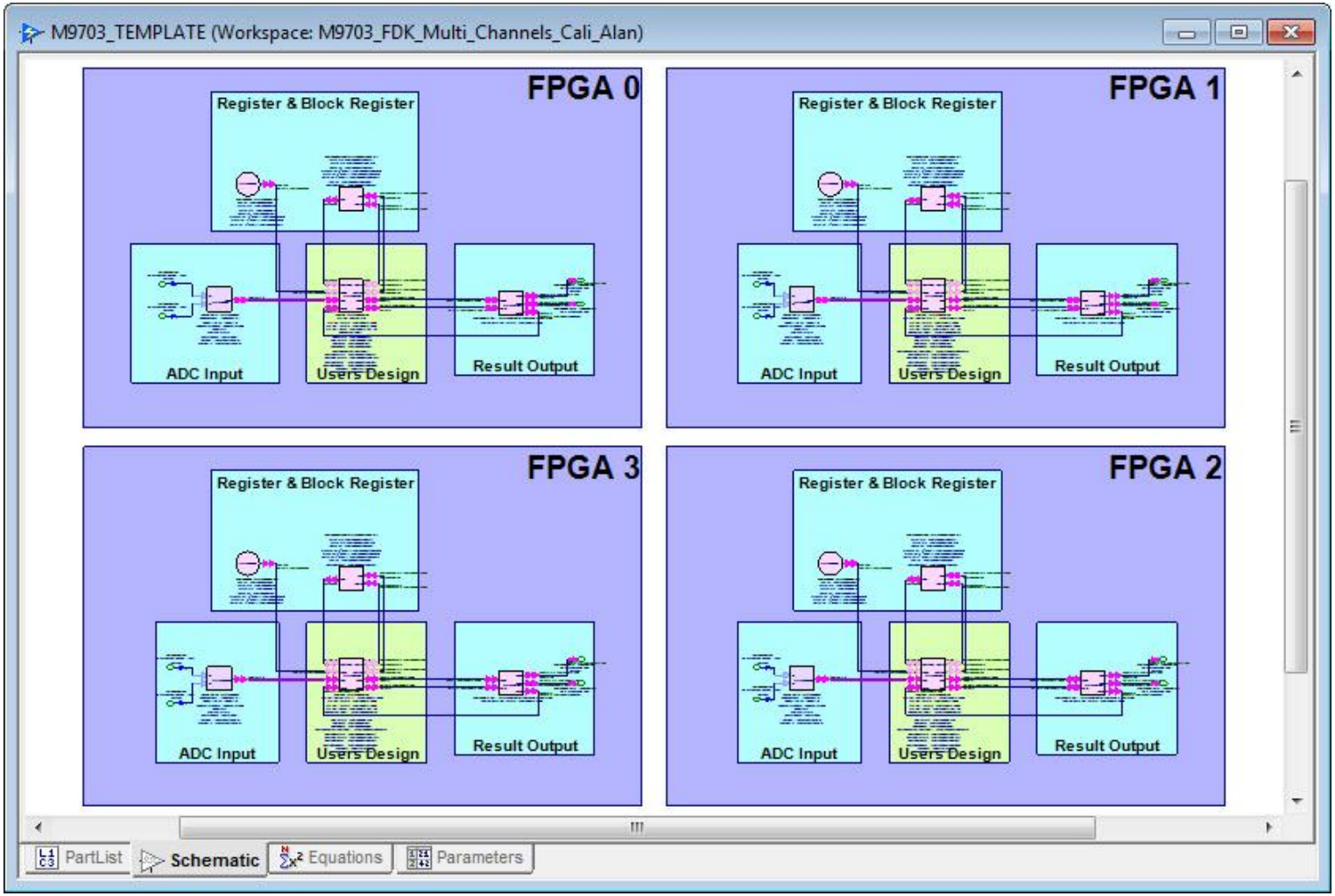




M9703A
FPGA

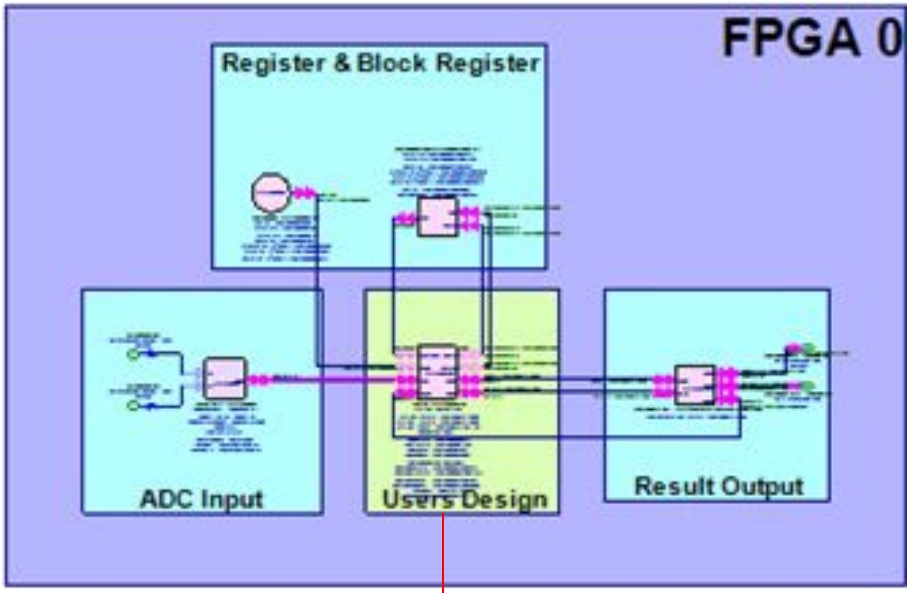
Demo II Setup Guide

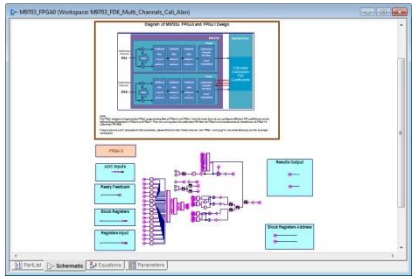
*Cosim **Step 1** (no HW) – M9703A Template*



Demo II Setup Guide

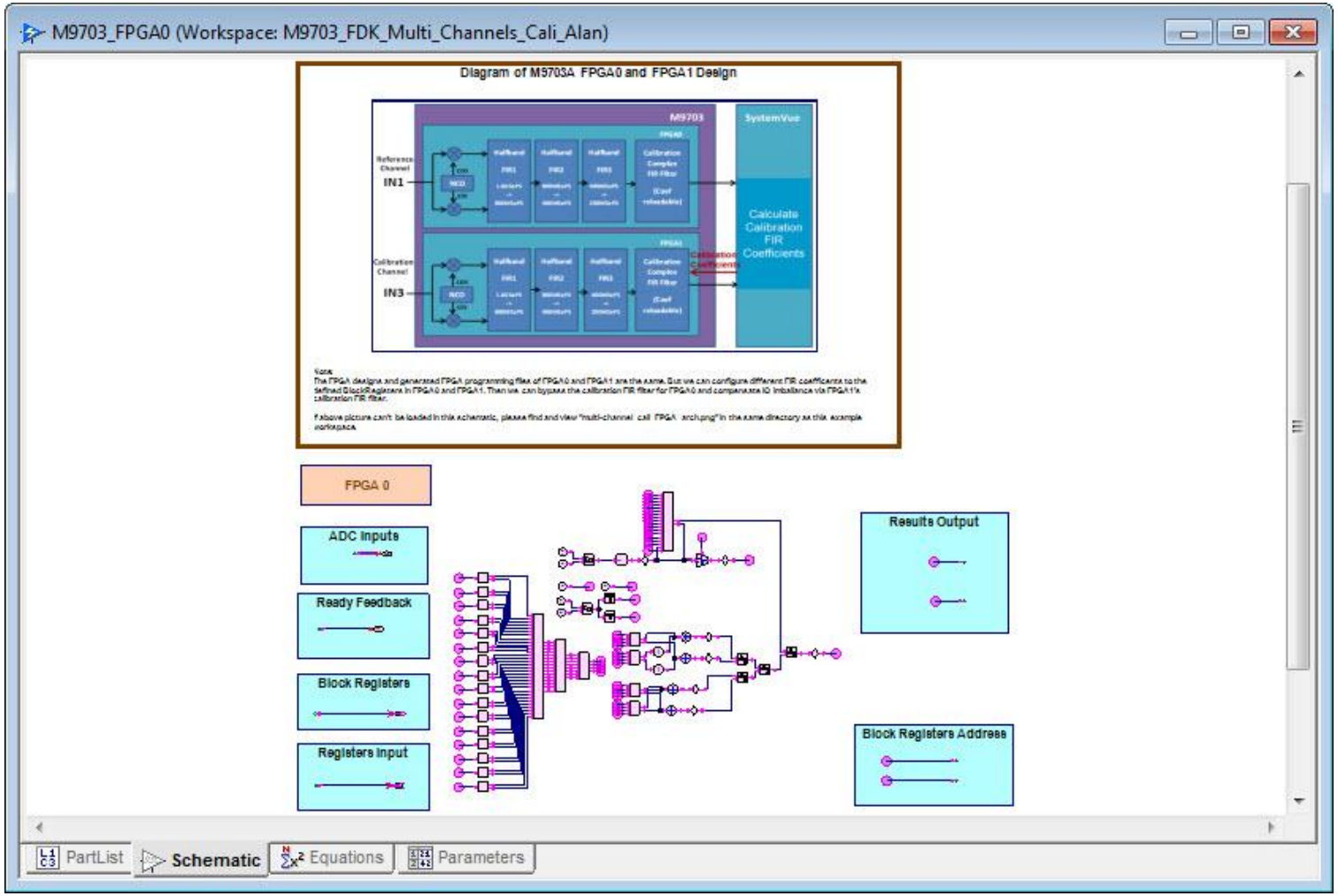
*Cosim **Step 1** (no HW) – M9703A User Design*





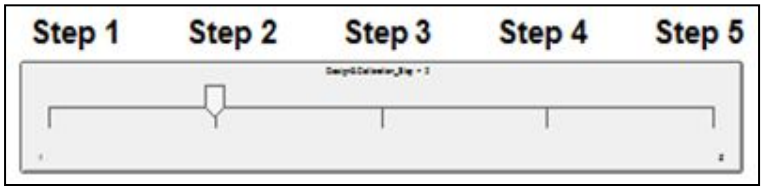
Demo II Setup Guide

*Cosim **Step 1** (no HW) – M9703A User Design*



Demo II Setup Guide

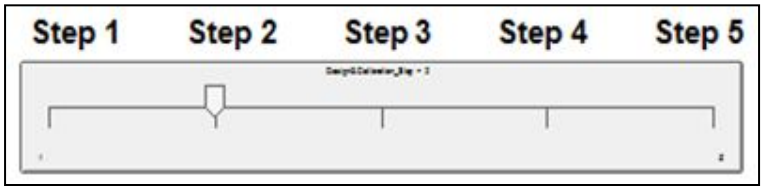
*Cosim **Step 2** – Source Configuration*

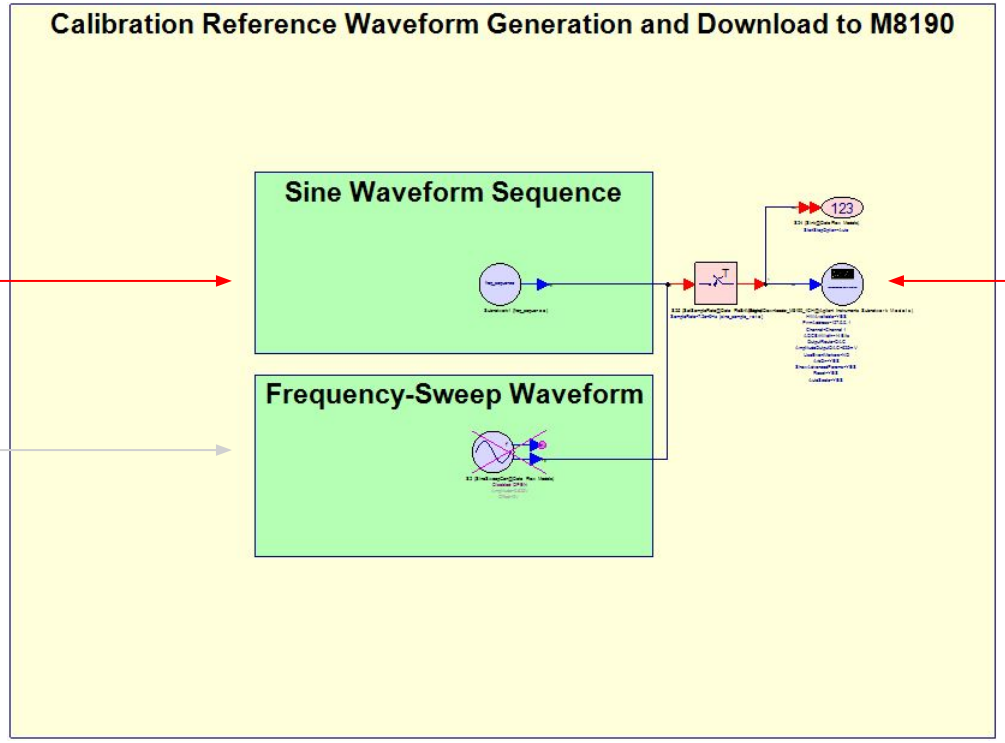


1. SW simulation step only (no HW)
2. Source M8190 configuration
3. M9703 measurement + calculate filter coefficients from reference channel (In1)
4. Source M8190 signal generation
5. M9703 compensation applied to target channel (In3)

Demo II Setup Guide

*Cosim **Step 2** – M8190 Source Setup*





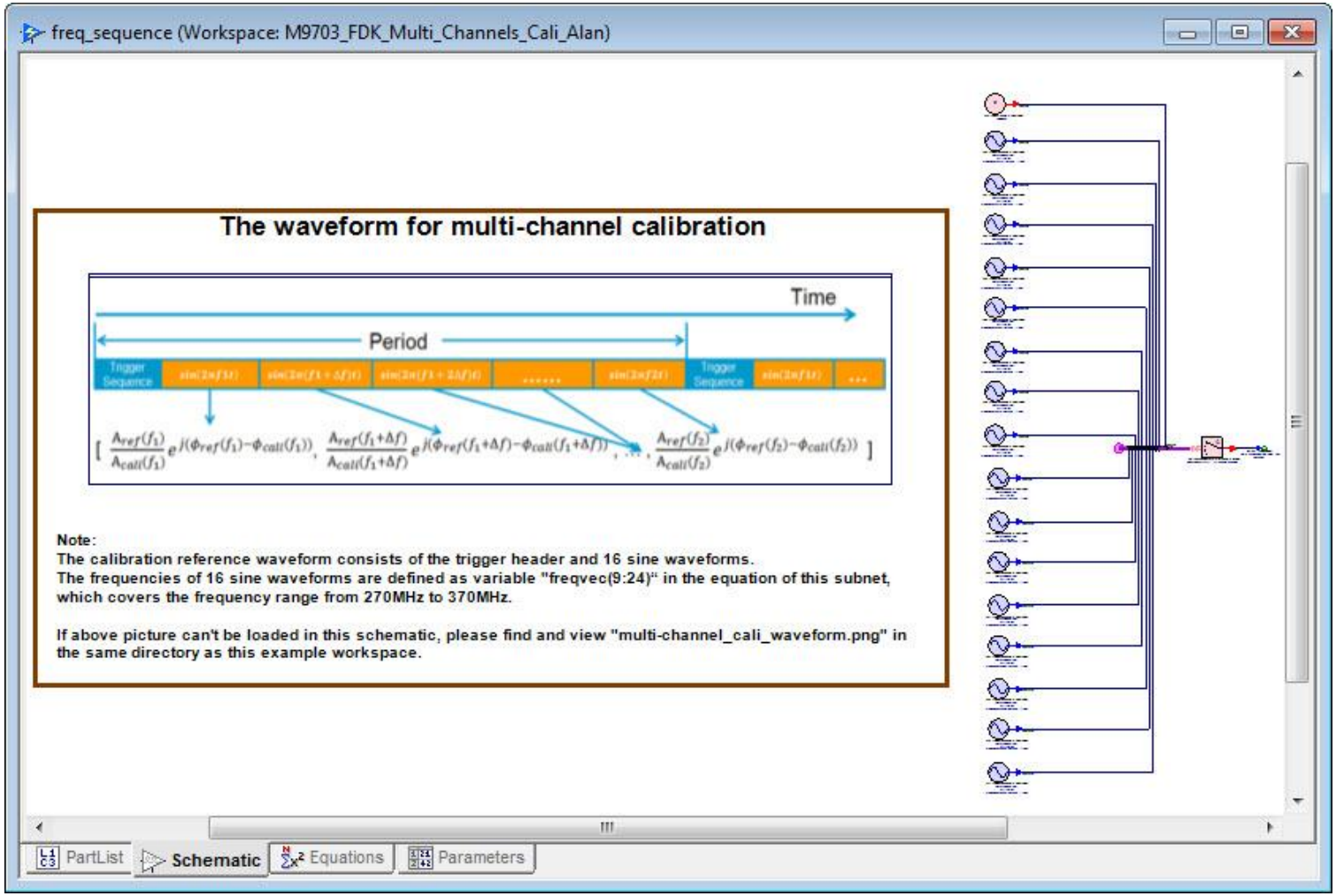
15 Sinusoid Sources (Step 2)

Chirped Source (Step 4)

M8190 Source

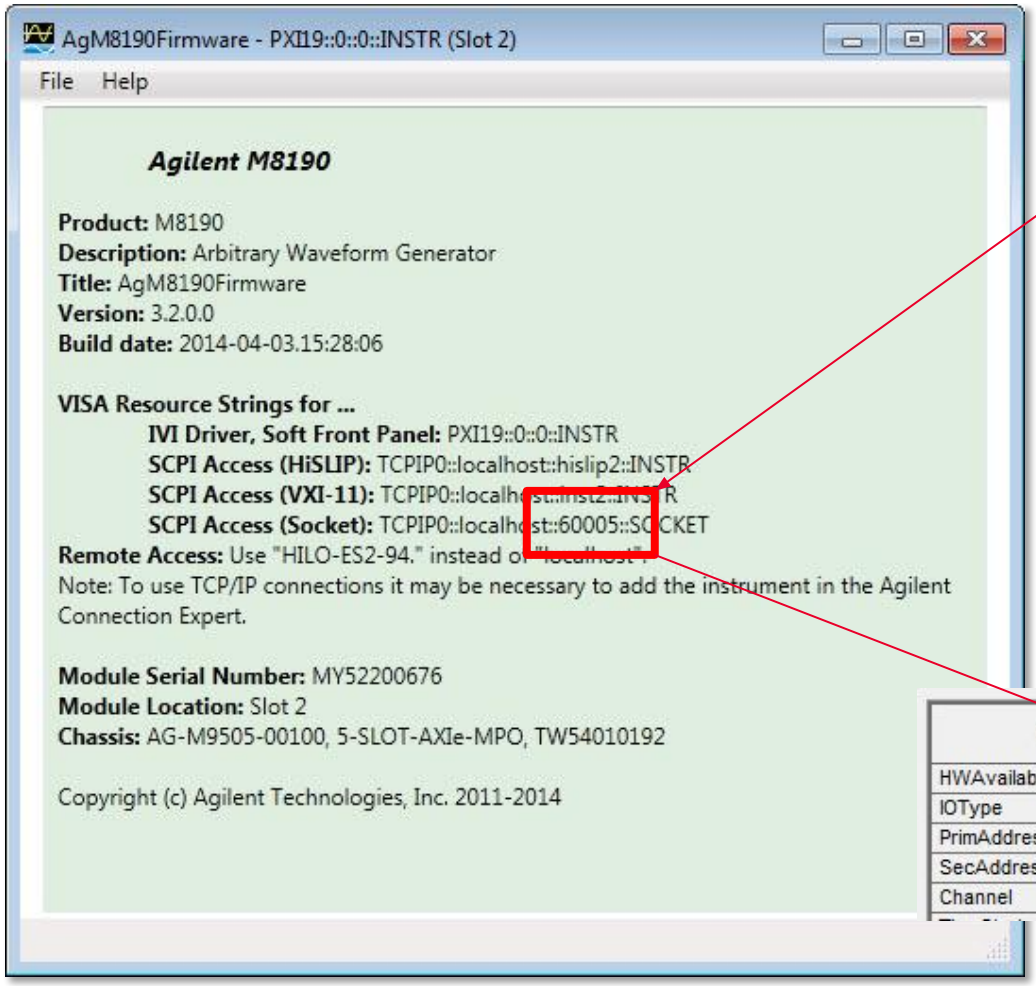
Demo II Setup Guide

*Cosim **Step 2** – Download 15 Sinusoid Sources, BW =100 MHz*

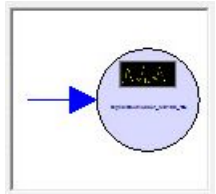


Demo II Setup Guide

*Cosim **Step 2** – M8190 Address Declarations*



M8190A Secondary Address
60005 (Cleared)

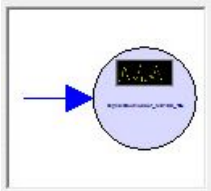


Name	Value	Units
HWAvailable	1:YES	( )
IOType	LAN	( )
PrimAddress		( )
SecAddress	60005	( )
Channel	1:Channel 1	( )

Demo II Setup Guide

*Cosim **Step 2** – M8190 LAN Connectivity*

M8190A Primary Address
127.0.0.1 (Error)



Errors

	Type	Error	Location	
1	Error	Sink 'Design3__S4.S1': Error on line 119: Unable to connect to '127.0.0.1'.	Part 'S1' in Design 'SignalDownloader_M8190_1CH'	n/a
2	Warning	Symbol "AutoSymDF" (Subnetwork21) is missing Port 3. If this is an automatic symbol, perhaps the associated model/subcircuit has port-numbering issues; ports	CSchematic '' in Design 'M9703_FPGA0'	Show

☑ Automatically Display Errors ☐ Show Graph and Table Errors (10) Clear All Errors

Errors

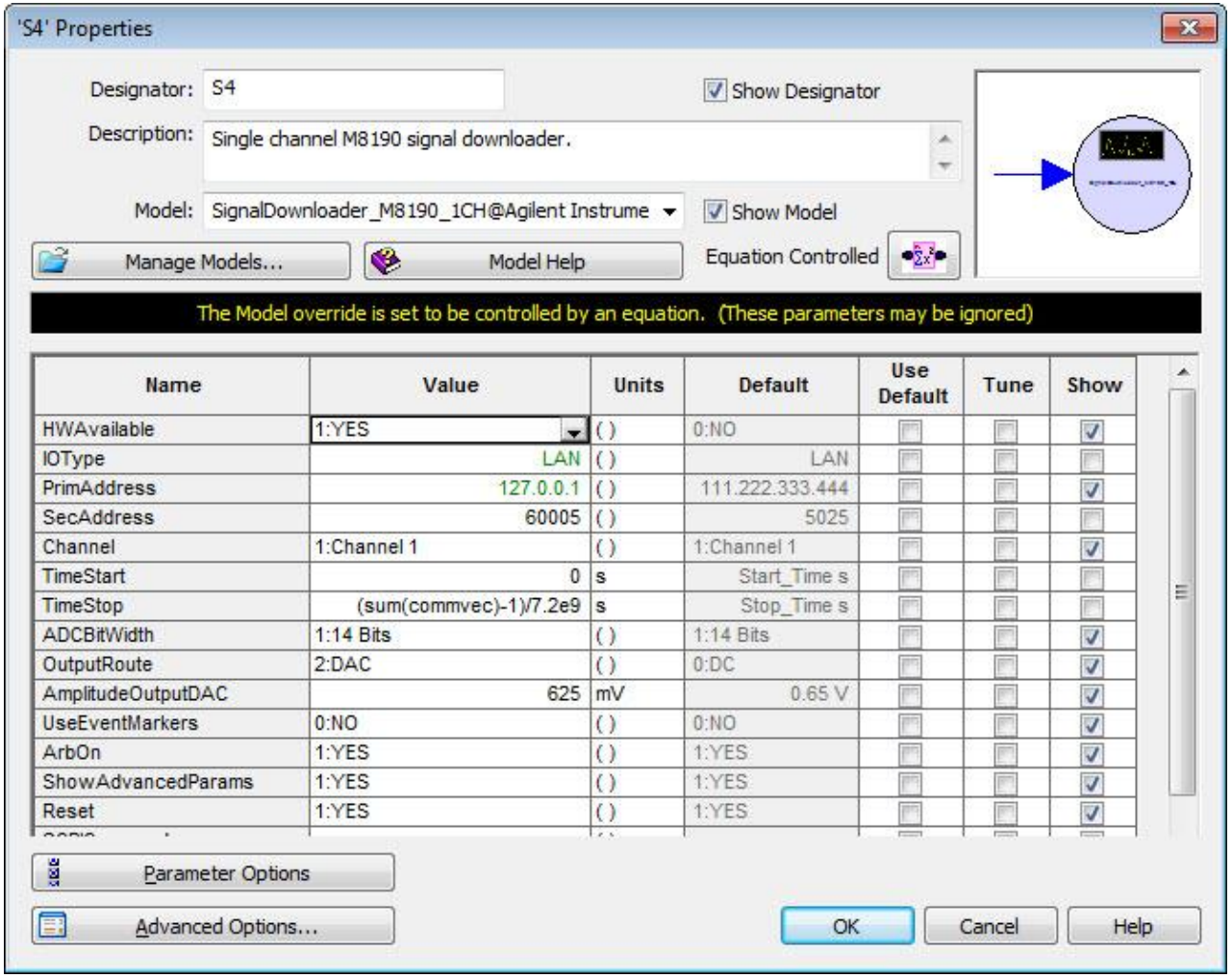
	Type	Error	Location	
1	Warning	Symbol "AutoSymDF" (Subnetwork21) is missing Port 3. If this is an automatic symbol, perhaps the associated model/subcircuit has port-numbering issues; ports should start at 1 and be consecutively numbered (no skipping).	CSchematic '' in Design 'M9703_FPGA0'	Show
2	Warning	Symbol "AutoSymDF" (Subnetwork23) is missing Port 3. If this is an automatic symbol, perhaps the associated model/subcircuit has port-numbering issues; ports	CSchematic '' in Design 'M9703_FPGA0'	Show

☑ Automatically Display Errors ☐ Show Graph and Table Errors (10) Clear All Errors

M8190A Secondary Address
60005 (Cleared)

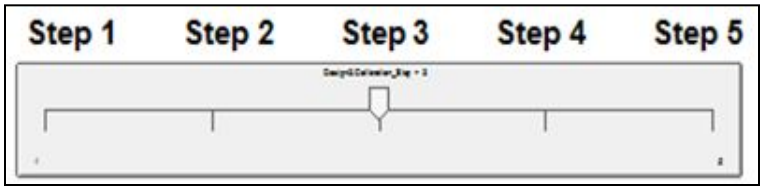
Demo II Setup Guide

*Cosim **Step 2** – M8190 Signal Downloader UI*



Demo II Setup Guide

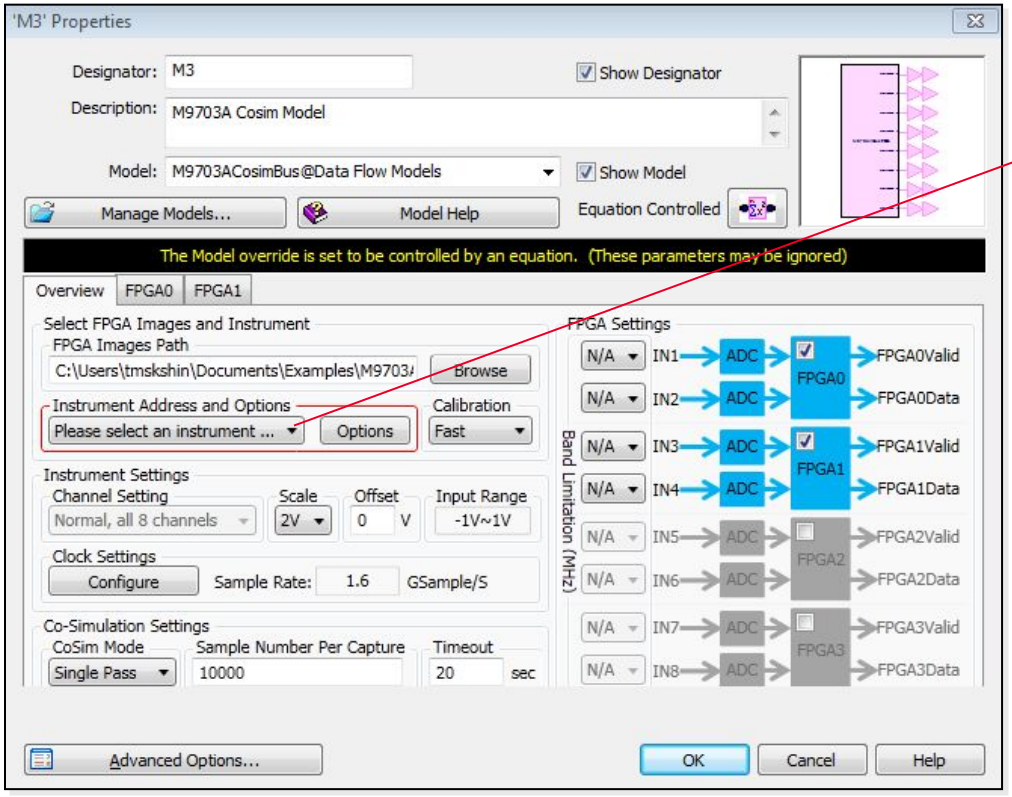
*Cosim **Step 3** – Reference Channel (Uncorrected) Measurement*



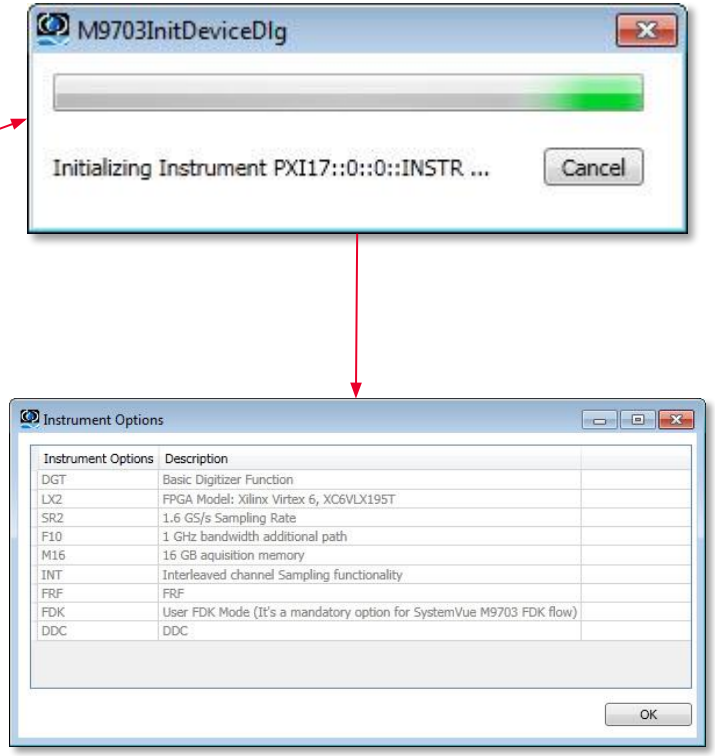
1. SW simulation step only (no HW)
2. Source M8190 configuration
3. M9703 measurement + calculate filter coefficients from reference channel (In1)
4. Source M8190 signal generation
5. M9703 compensation applied to target channel (In3)

Demo II Setup Guide

*Cosim **Step 3** – M9703A Setup & UI Parameters*



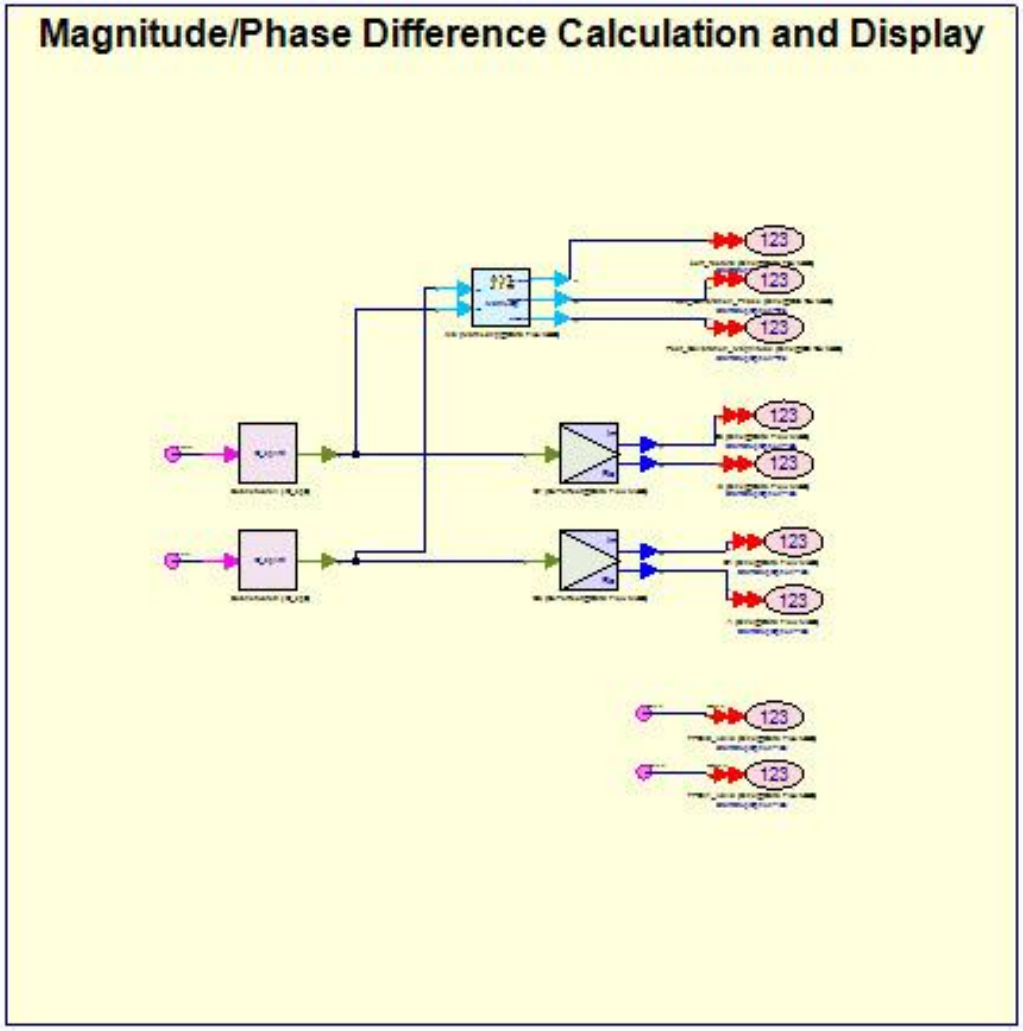
M9703 Cosim Parameters



M9703 Connection and Options

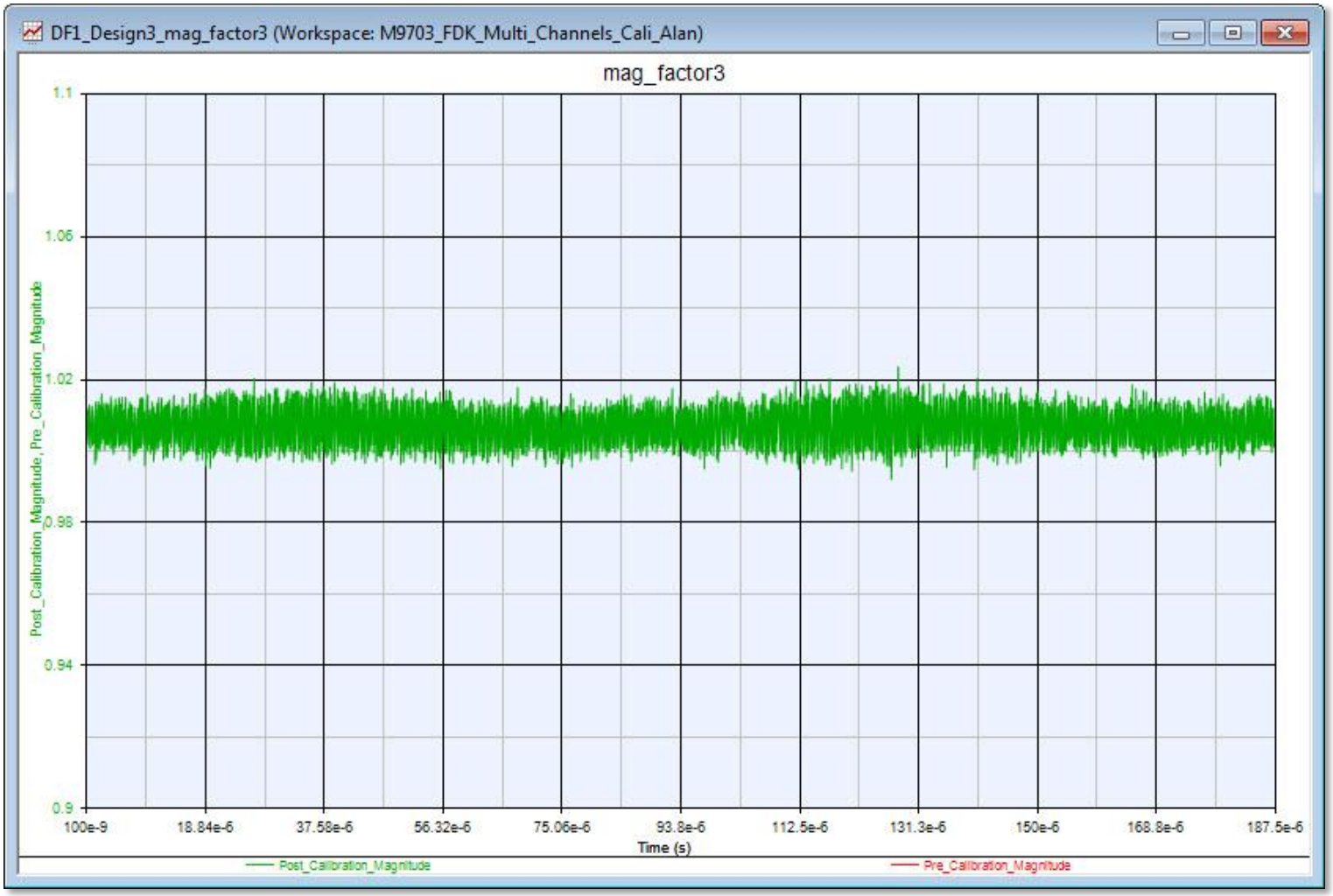
Demo II Setup Guide

*Cosim **Step 3** – Reference Channel (In1) Measurement Calculation*



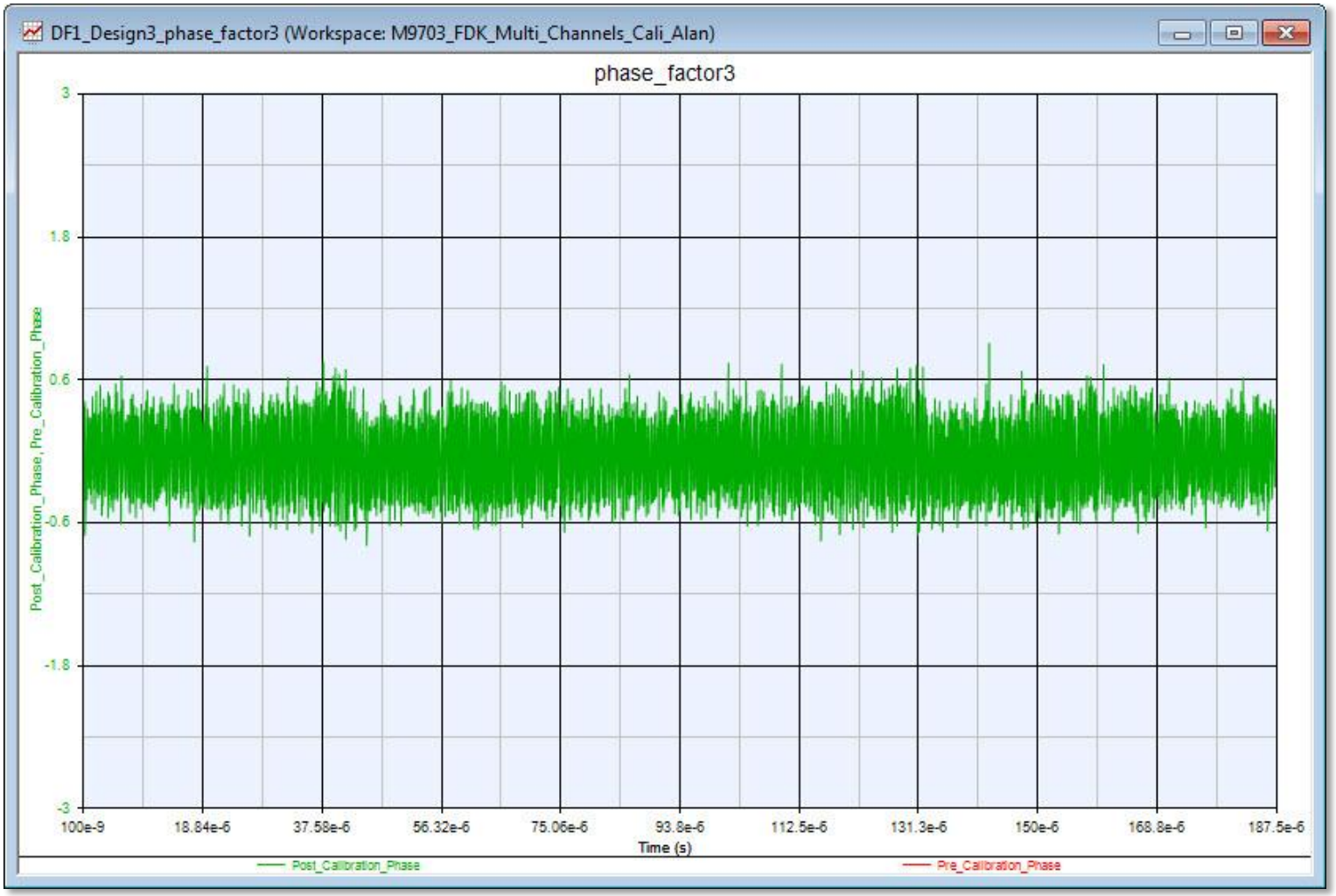
Demo II Setup Guide

*Cosim **Step 3** – Reference Channel (In1) Magnitude*



Demo II Setup Guide

*Cosim **Step 3** – Reference Channel (In1) Phase*



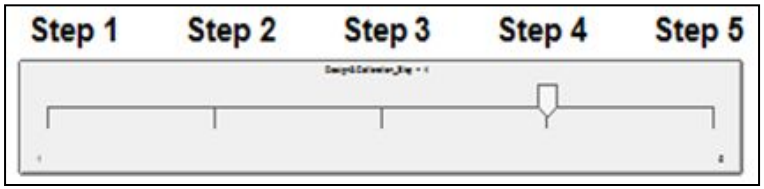
Demo II Setup Guide

*Cosim **Step 3**(1) – Configure M9703A and Capture Results (VSA)*

Note (1): Separate VSA enabled workspace, not req'd.

Demo II Setup Guide

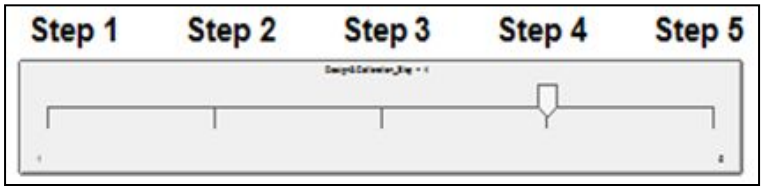
*Cosim **Step 4** – Source Configuration*

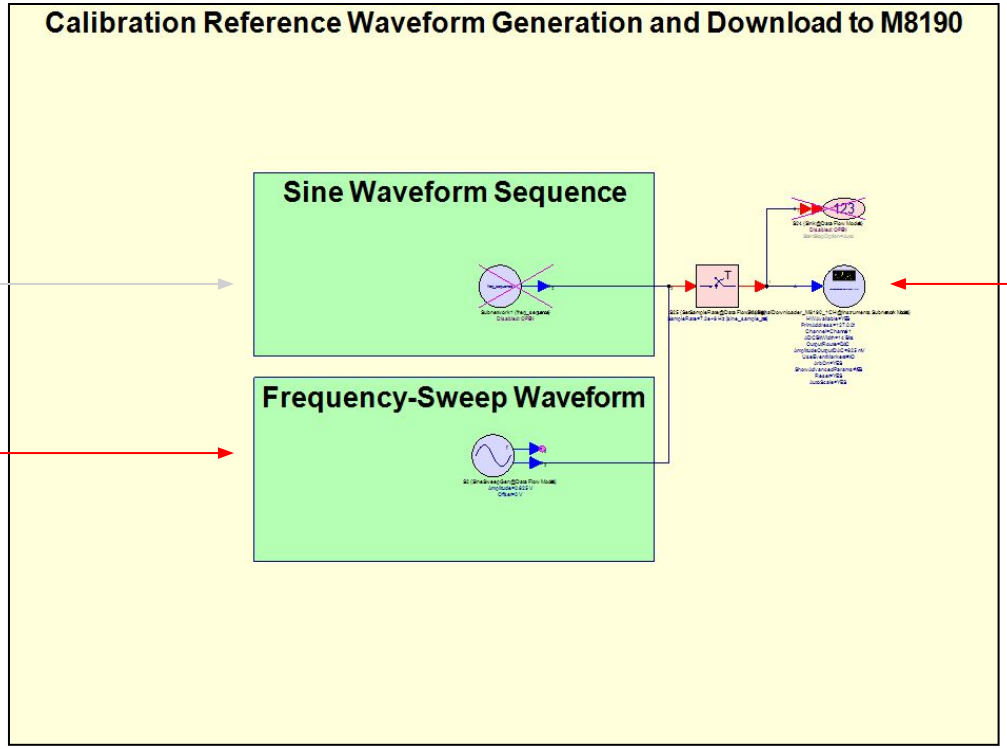


1. SW simulation step only (no HW)
2. Source M8190 configuration
3. M9703 measurement + calculate filter coefficients for reference channel (In1)
4. Source M8190 signal generation
5. M9703 compensation applied to target channel (In3)

Demo II Setup Guide

*Cosim **Step 4** – M8190 Source Setup*





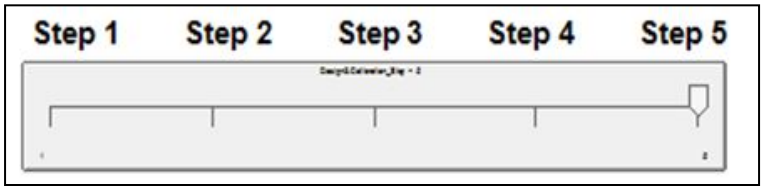
Sinusoid Sources
(Step 2)

Chirped Source
(Step 4)

M8190
Source

Demo II Setup Guide

*Cosim **Step 5** – Target Channel (Corrected) Measurement*

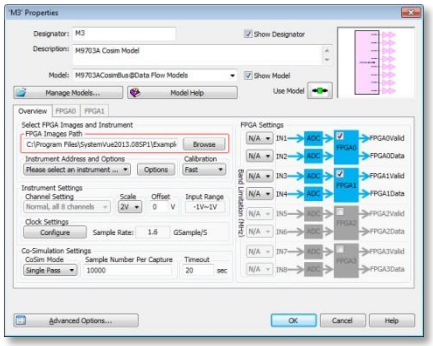


1. SW simulation step only (no HW)
2. Source M8190 configuration
3. M9703 measurement + calculate filter coefficients for reference channel (In1)
4. Source M8190 signal generation
5. M9703 compensation applied to target channel (In3)

Demo II Setup Guide

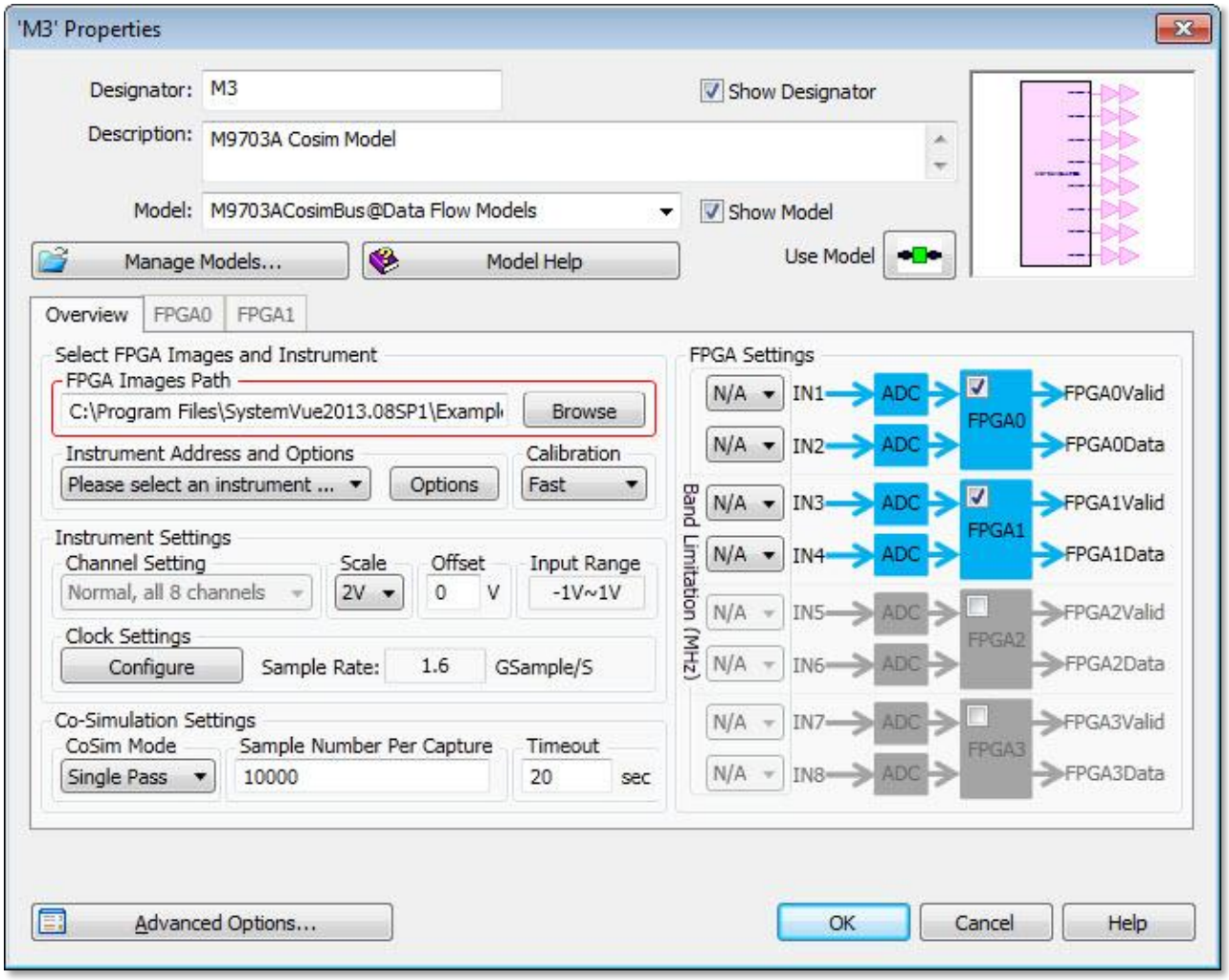
*Cosim **Step 5** – M9703A Cosim Model*

Configure M9703 and Capture Output Results



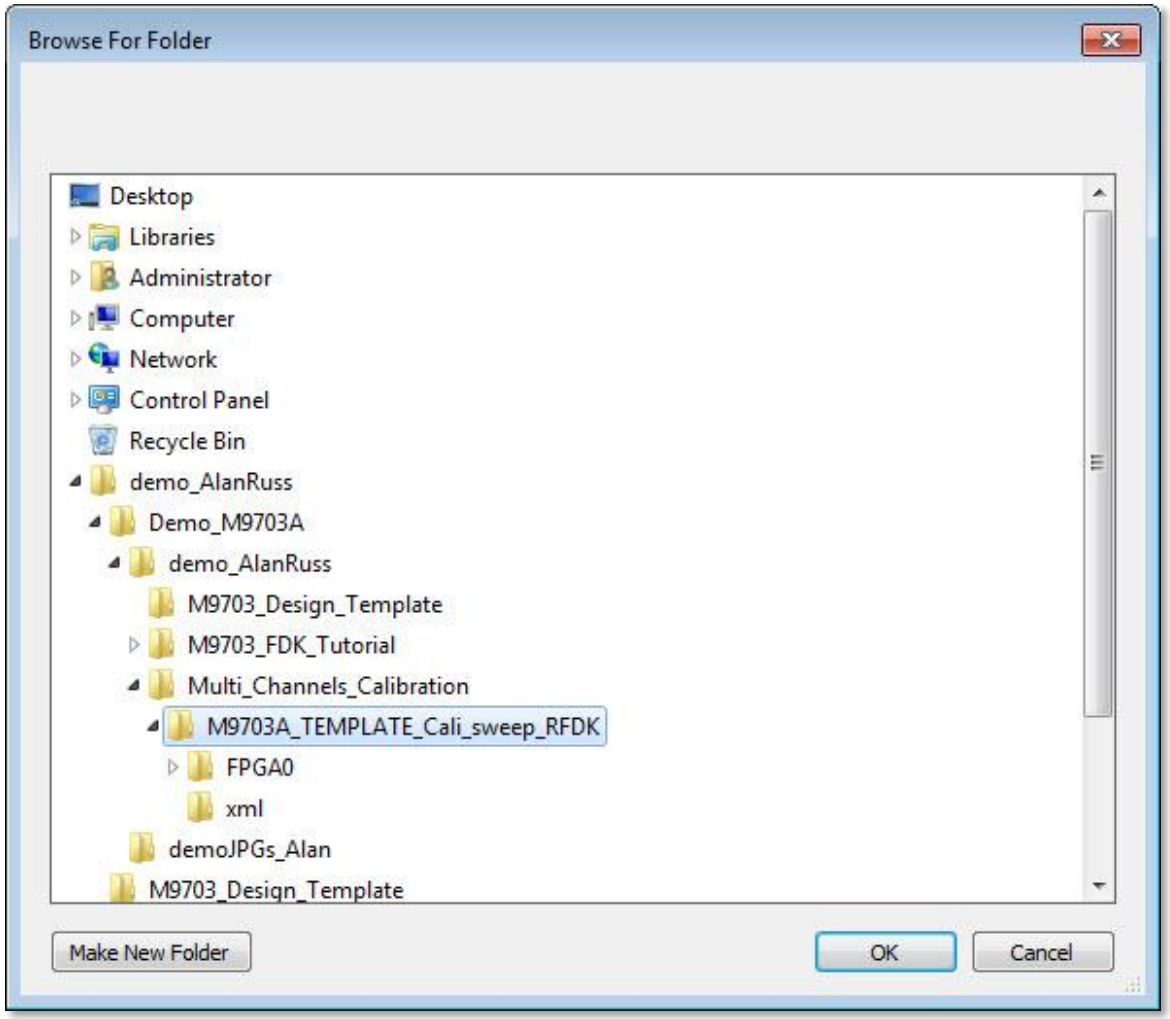
Demo II Setup Guide

*Cosim **Step 5** – M9703A UI Parameters (Setup Errors)*



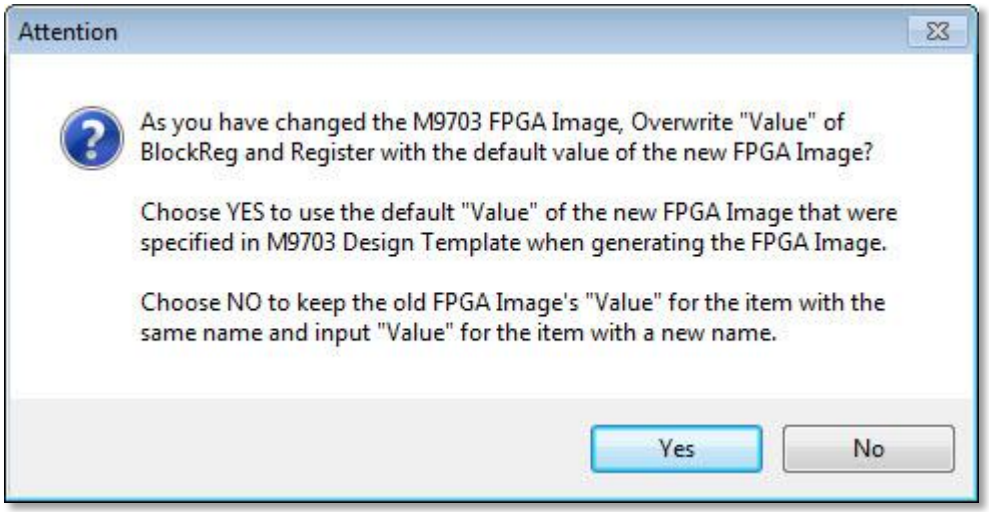
Demo II Setup Guide

*Cosim **Step 5** – M9703A FPGA Path Correction*



Demo II Setup Guide

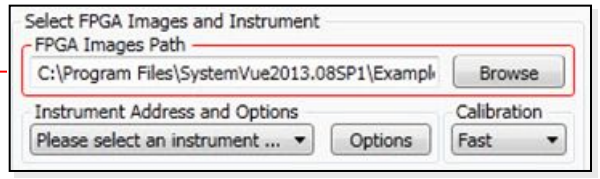
*Cosim **Step 5** – M9703A FPGA Path Correction Message*

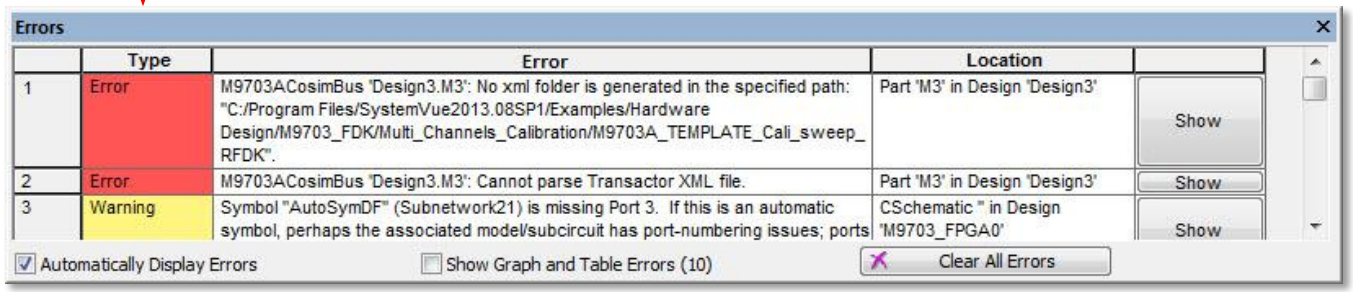


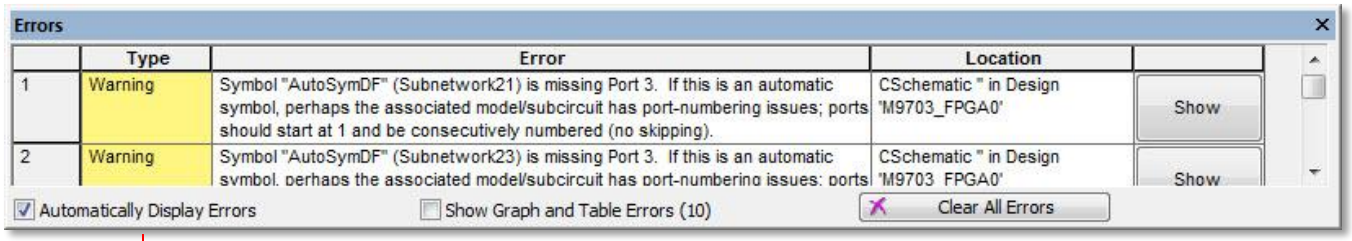
Demo II Setup Guide

*Cosim **Step 5** – M9703A FPGA Setup Errors*

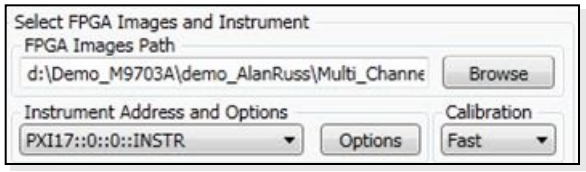
Default Path (Error)







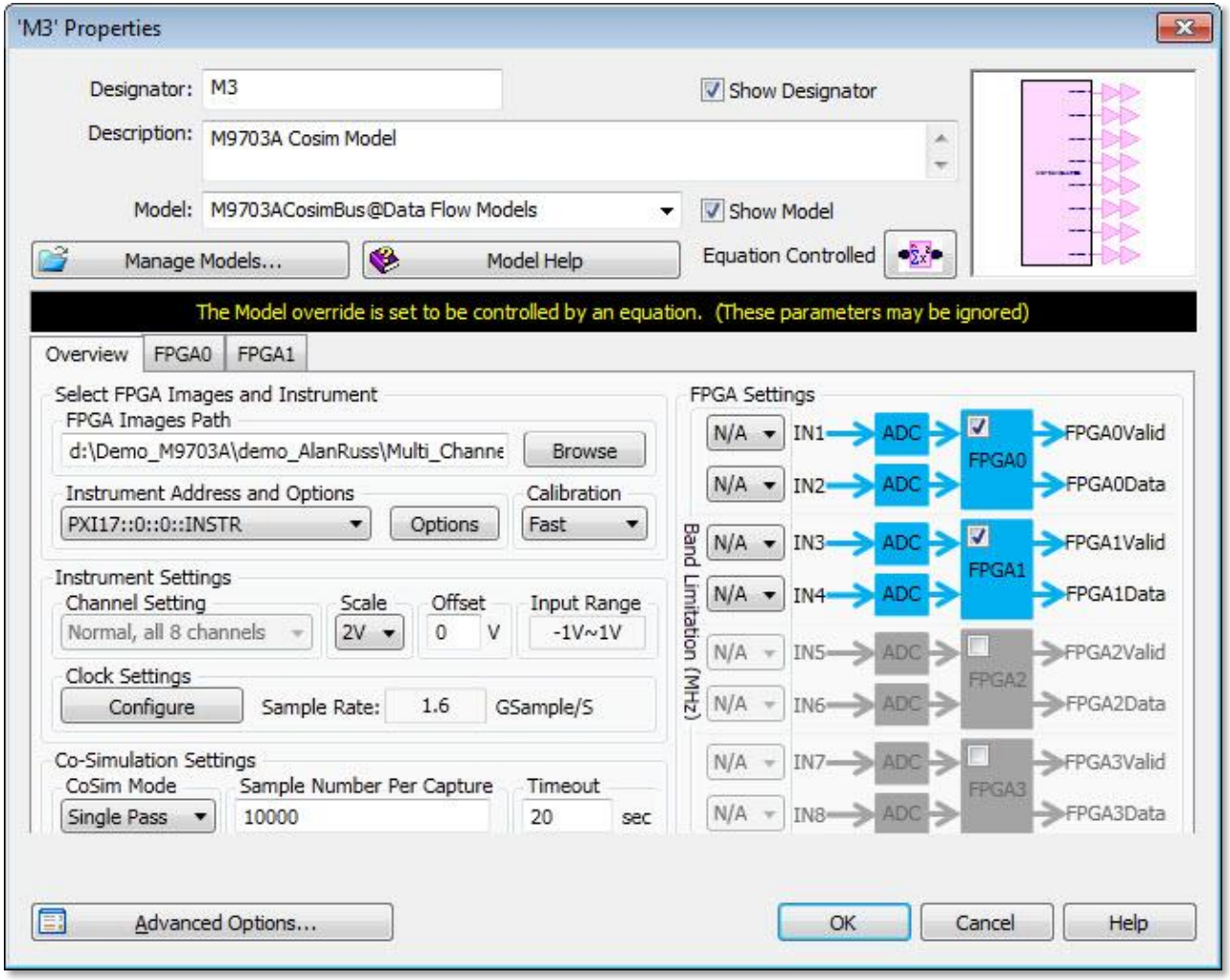
User Path (Cleared)



Note: Drive letter must be lowercase.

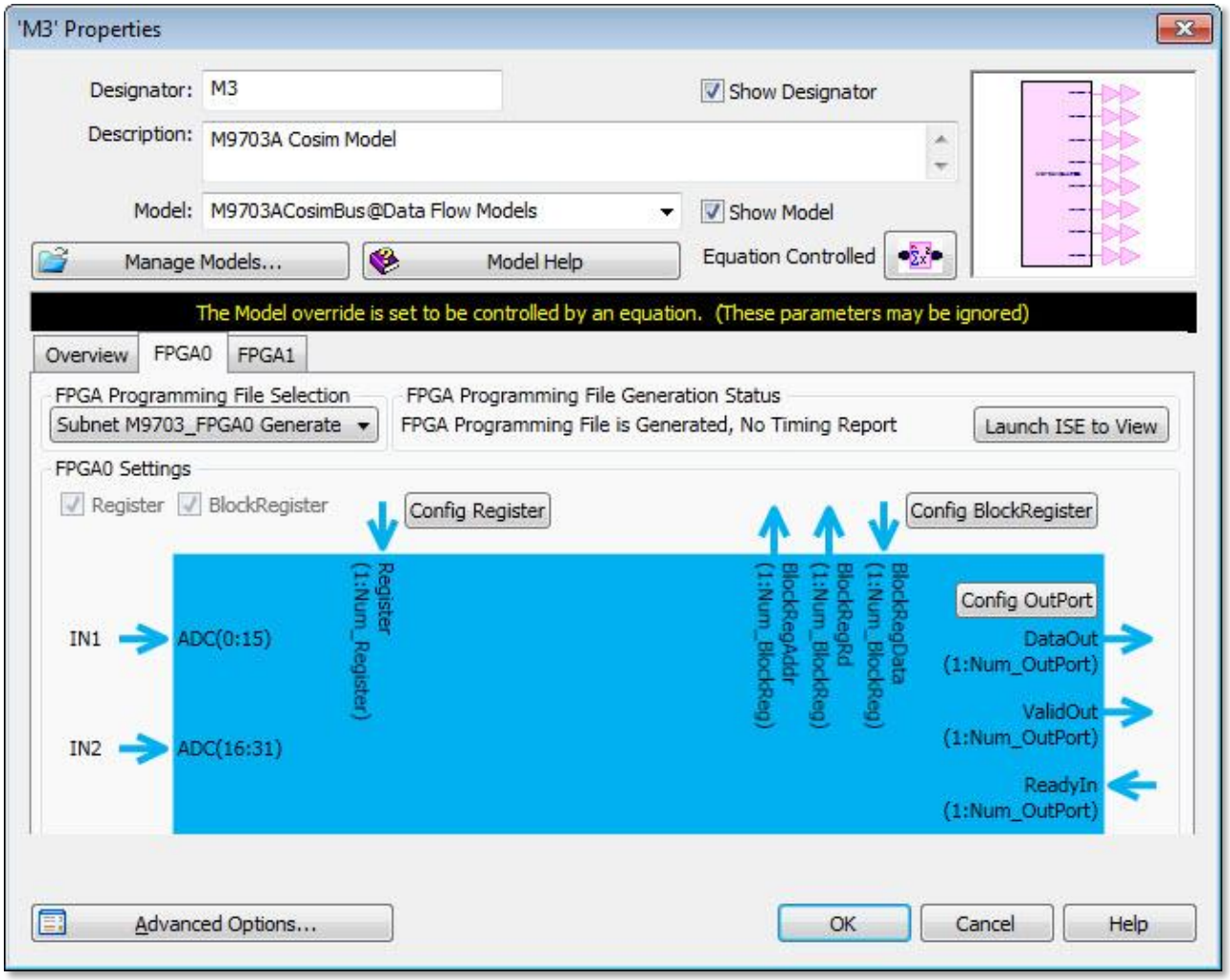
Demo II Setup Guide

*Cosim **Step 5** – M9703A FPGA Setup Errors (Cleared)*



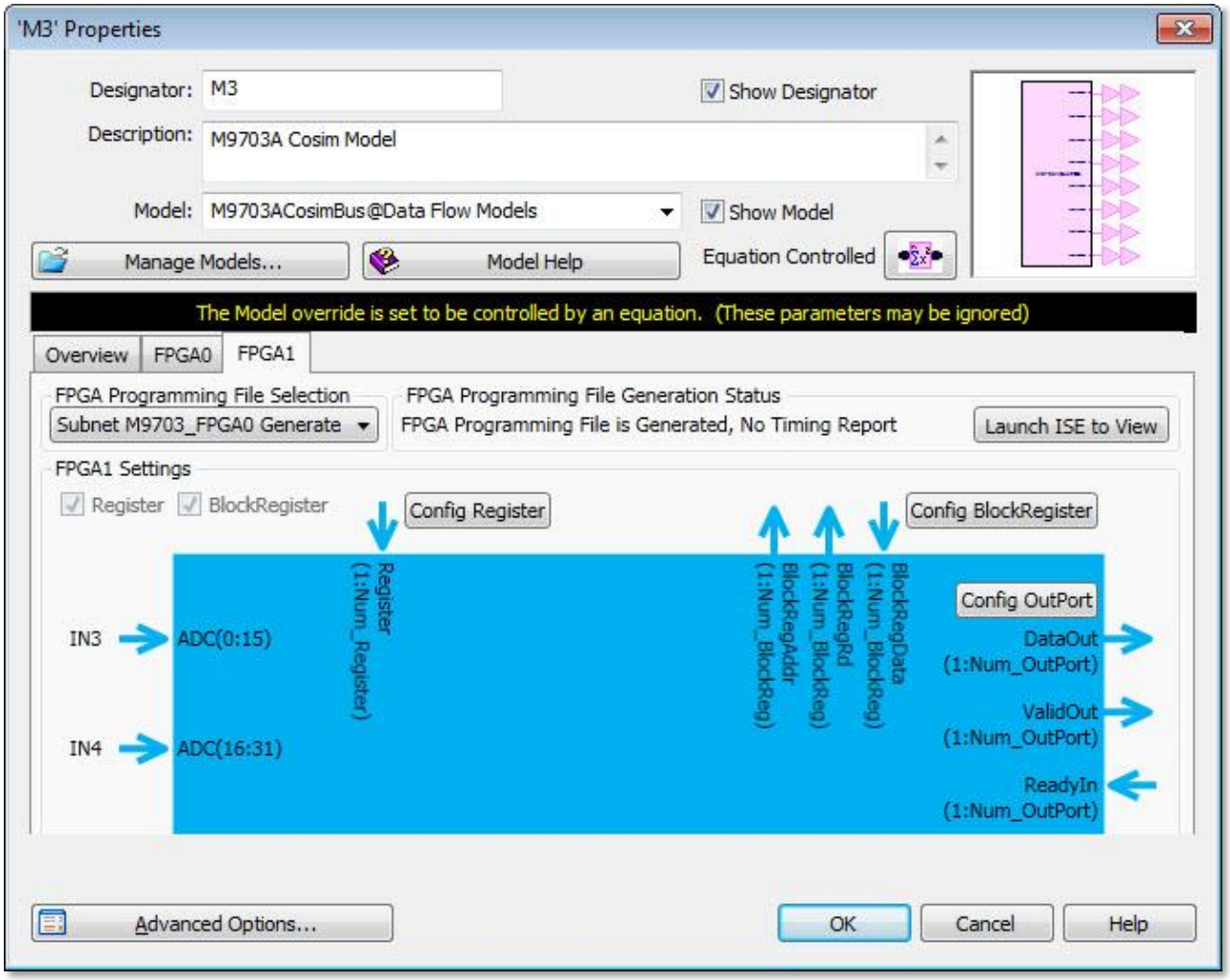
Demo II Setup Guide

*Cosim **Step 5** – M9703A FPGA(0) Programming UI*



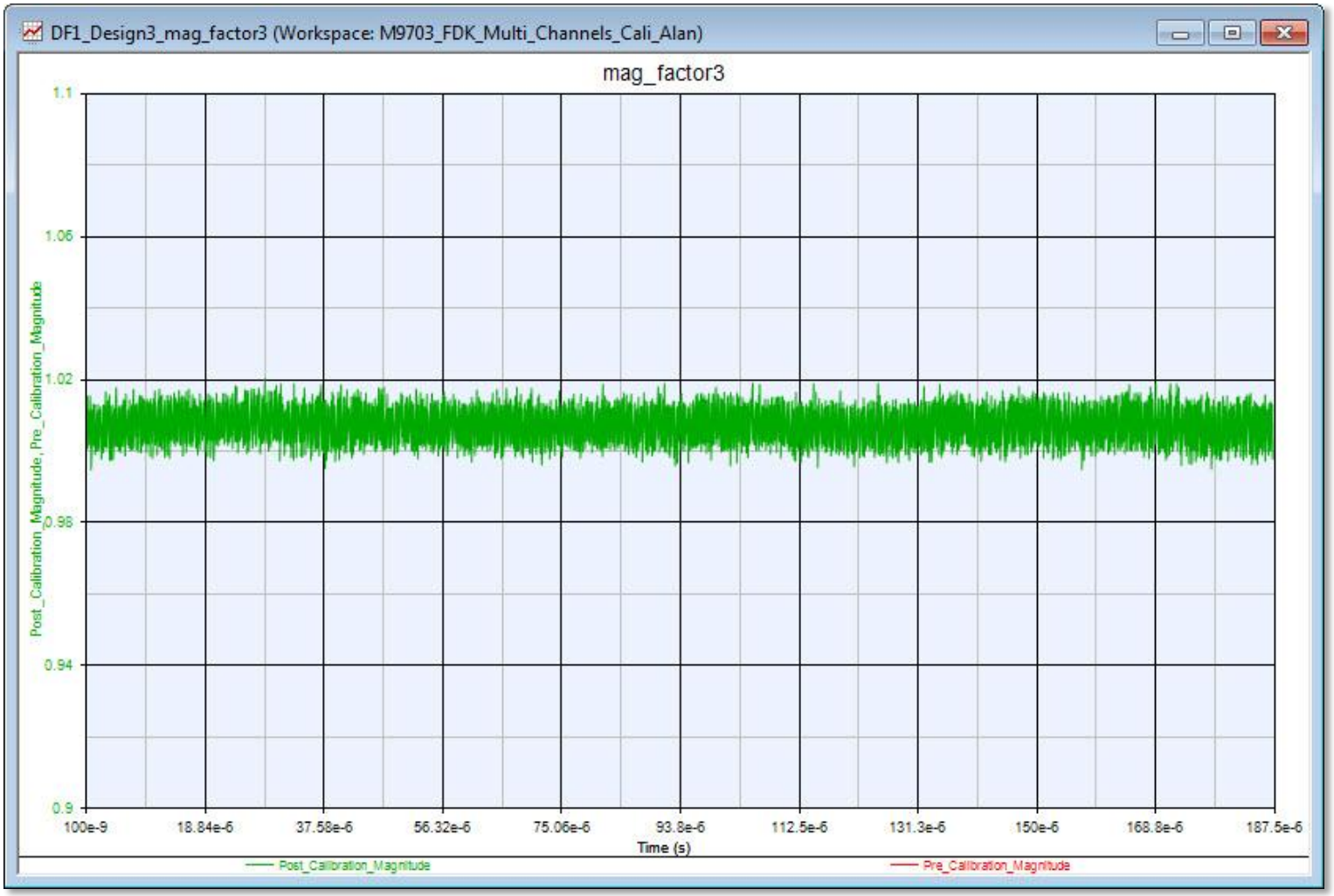
Demo II Setup Guide

*Cosim **Step 5** – M9703A FPGA(1) Programming UI*



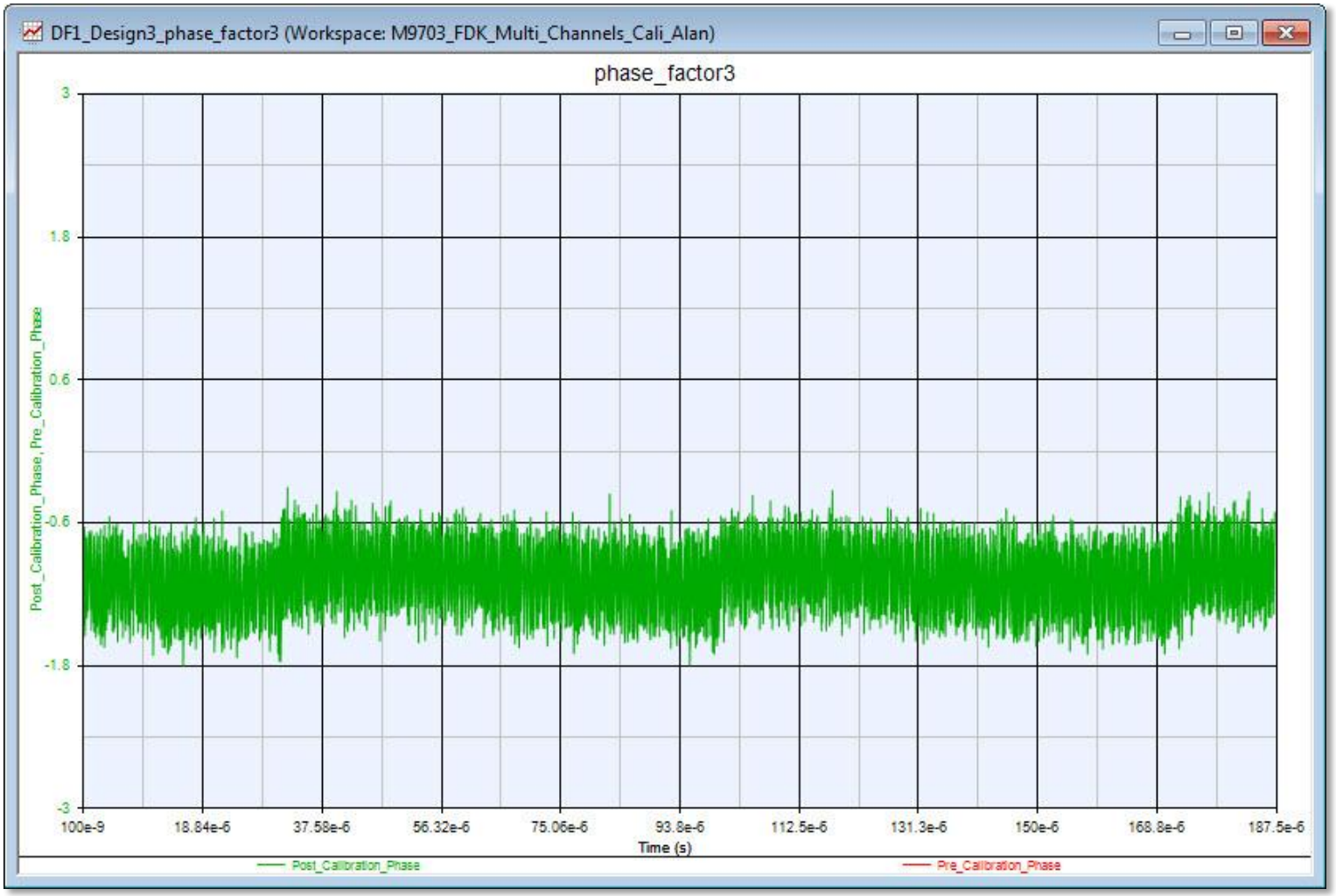
Demo II Setup Guide

*Cosim **Step 5** – Corrected Channel (In3) Magnitude*



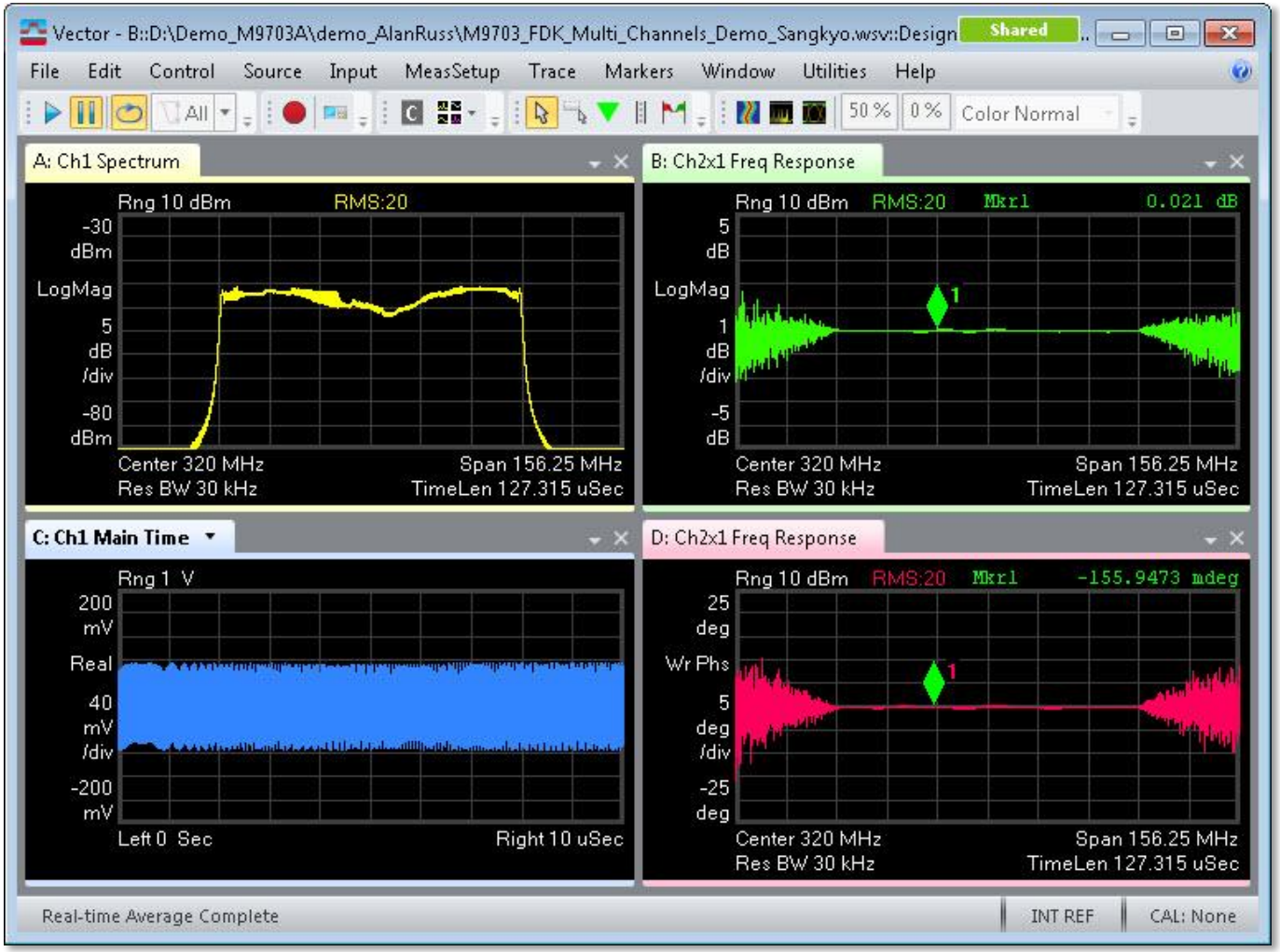
Demo II Setup Guide

*Cosim **Step 5** – Corrected Channel (In3) Phase*



Demo II Setup Guide

*Cosim **Step 5**(1) – Configure M9703A and Capture Results (VSA)*



Note (1): Separate VSA enabled workspace, not req'd.

Summary

- Introduction to SystemVue hardware design kit
- General SystemVue hardware design flow
- Integrated FPGA design flow demo for M9703A digitizer

Thank you

Questions

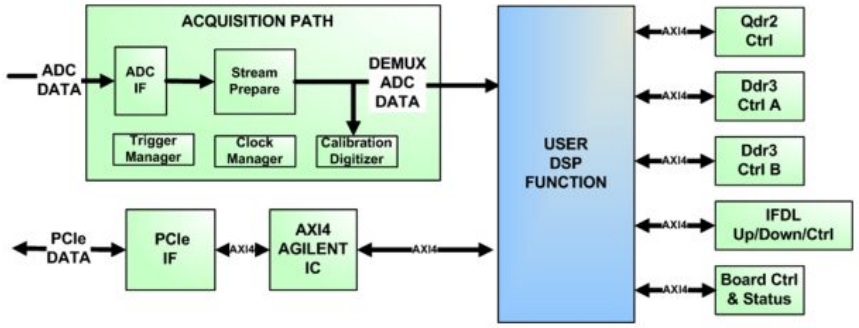
yahia_tachwali@keysight.com

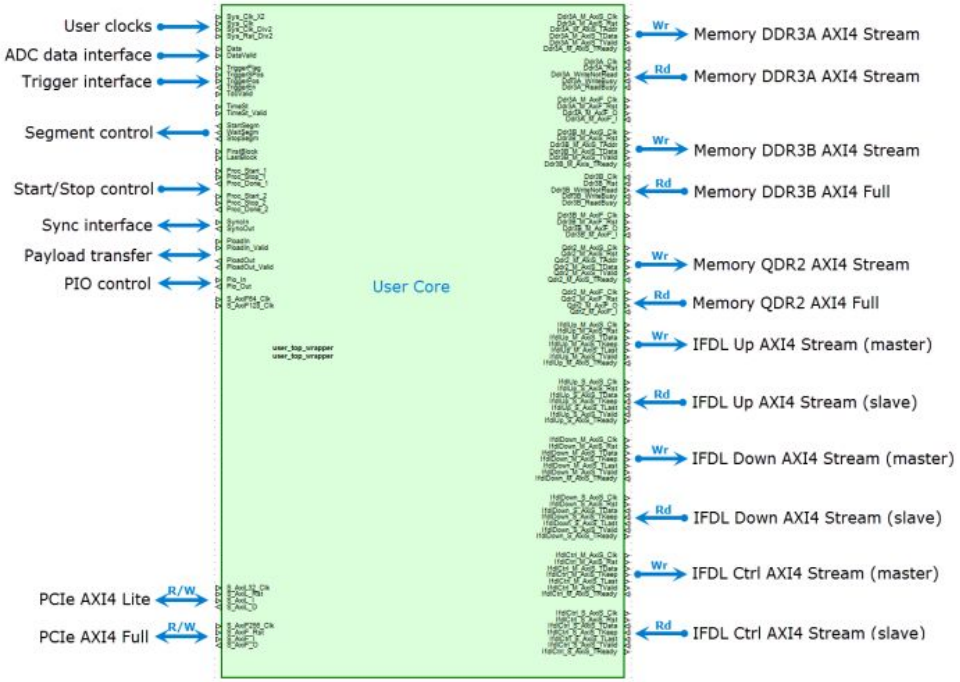
Backup

M9703A DPU FPGA user core interface

DPU FPGA User Core Interface:

- ADC data stream input
  - ✔ Parallel input
- Two DDR3 memory
  - ✔ WR: AXI4-Stream
  - ✔ RD: AXI4-Full
- QDRII memory
  - ✔ WR: AXI4-Stream
  - ✔ RD: AXI4-Full
- PCIe connectivity with backplane via PCIe switch
  - ✔ AXI4-Full
  - ✔ AXI4-Lite
- Inter FPGAs data stream connectivity
  - ✔ AXI4-Stream

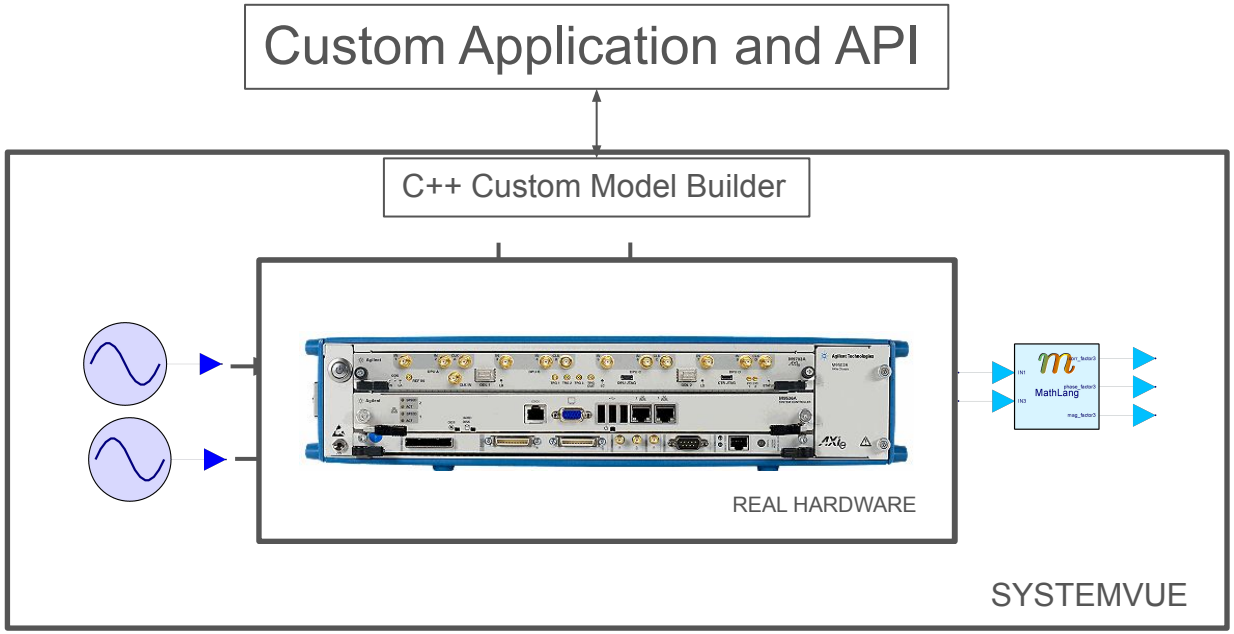




KEYSIGHT TECHNOLOGIES

Early development of Firmware/Software API's

Before HW arrives



- Basic module configuration and control.
- Low-level functions for register-based I/O.
- Low-level functions for block-transfers to and from the FPGA and associated memories.
- Higher-level APIs for controlling the FPGA

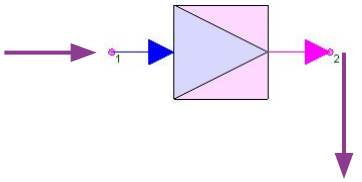
Standard Conforming Baseband

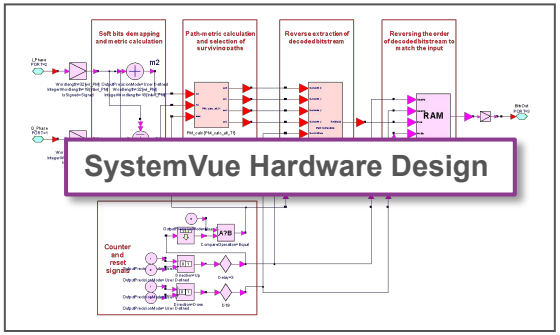
Stimulus and response metrology

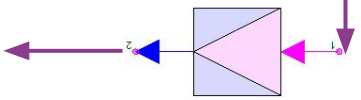
SystemVue **"Baseband Verification"** Libraries

3G/4G MOBILITY	NETWORKING
LTE-Advanced (Rel 10) LTE (Rel 8,9) WCDMA, HSPA+, CDMA, CDMA2000 GSM, EDGE	WiMAX / 802.15e WLAN /802.11abgn/ac 60GHz 802.11ad *Custom OFDM*
LOCAL CONNECTIVITY	**BROADCAST & SATCOMM**
WPAN / 802.15.3c 802.11ad *Zigbee / 802.15.4* *Bluetooth*	DVB-S2/T2, ISDB-T General Digital Modem GNSS *sat nav*
Available with W1461BP core environment	**DEFENSE**
	RADAR: PD, UWB, FMCW, SAR, DAR, SFR, MIMO, Phased Array

Data type conversion
Floating/Fixed Point

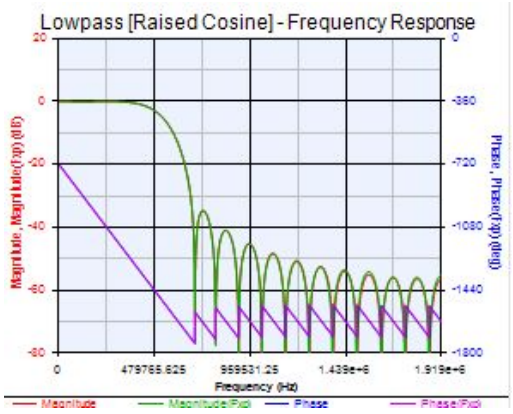


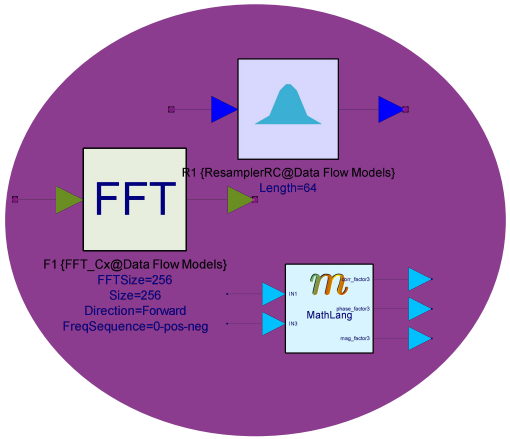


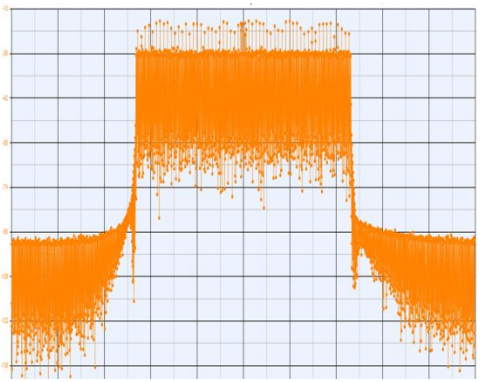


Simplify complex post analysis

- *Fixed to floating point data conversion*
- *FFT, Filtering, Re-sampling*
- *Time / Frequency domain conversion and plotting*
- *Send out data from SystemVue to user application for further processing and display*

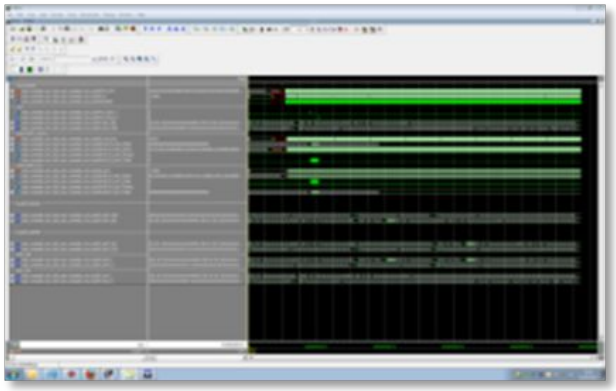




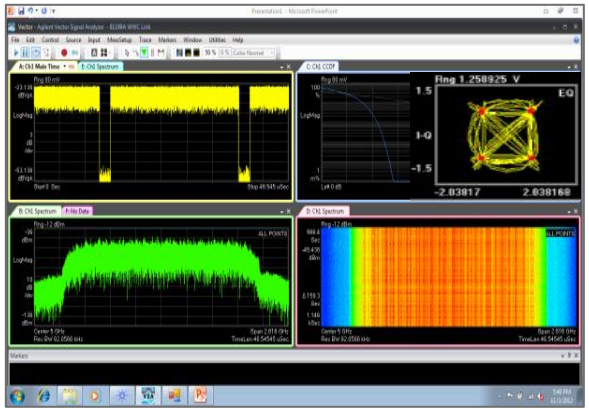


Overcome function test limitation of a timing based simulator

- Traditional analog functions are being moved to DSP - *DUC, DDC, DDS, Beam Former*, etc…
- Need more than timing & logic analysis
- How many FPGA designer can see vector analysis results during HDL coding and verification in traditional design flow?



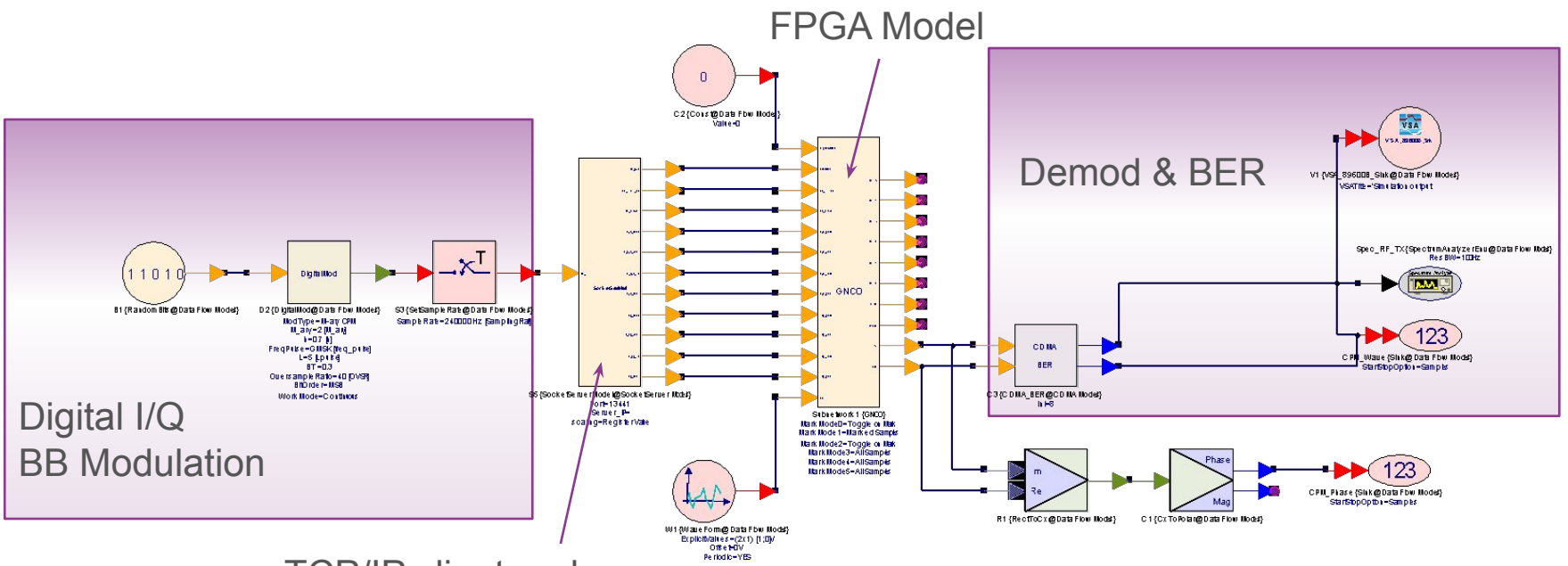
RTL Simulator



Keysight 89600 Vector Analysis Software

Real world system level simulation

Measurement and verification of an FPGA model requiring complex metrics in the presence of real world impairments.



A Realistic Example

Magnitude and phase calibration for multi-channels

Enhanced FPGA architecture with inter FPGA data transfer