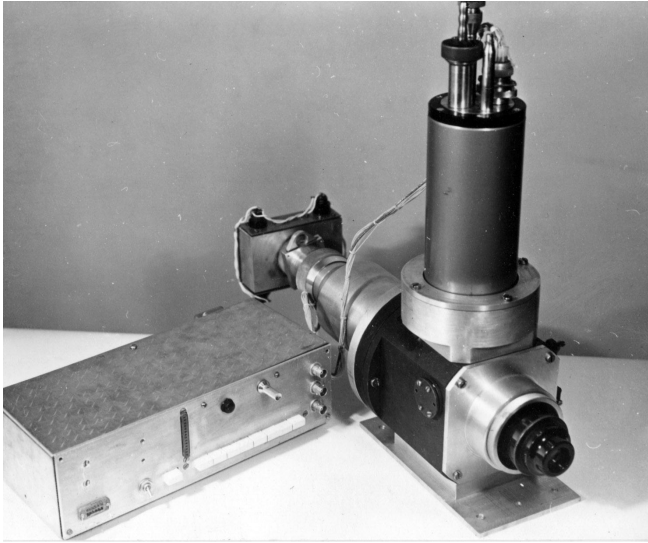


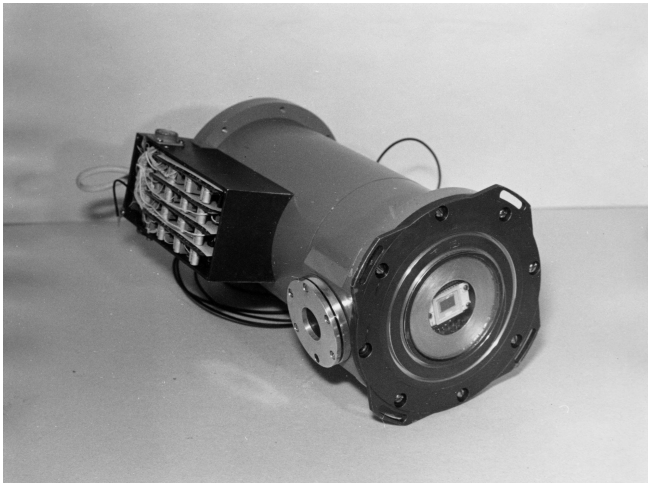
Advanced Design Lab: CCD History

Special Astrophysical Observatory, 2005

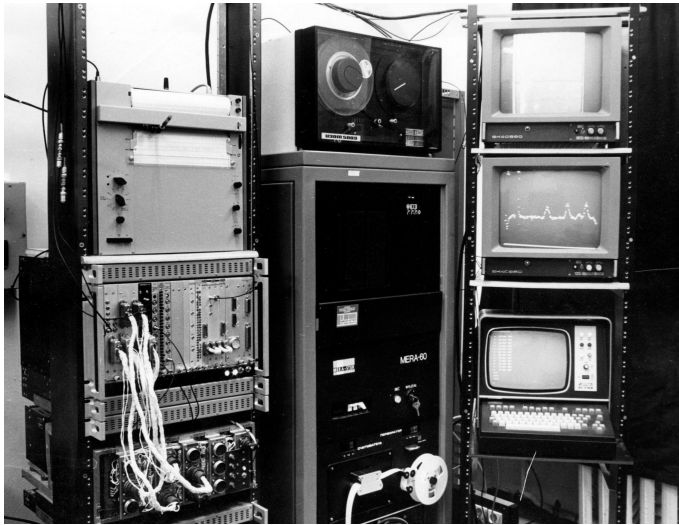
- Development of four generations of CCD Controllers
- Development of LN2 Cameras for various observation purposes
- Production of about 30 CCD Systems for 6-m telescope and other observatories
- Research and development of methods of CCD readout noise minimizing and photometric precision maximizing
- Investigation and testing of numerous SITe, E2V, Lick, TI, Atmel and others CCDs
- Climatic testing of CCD systems



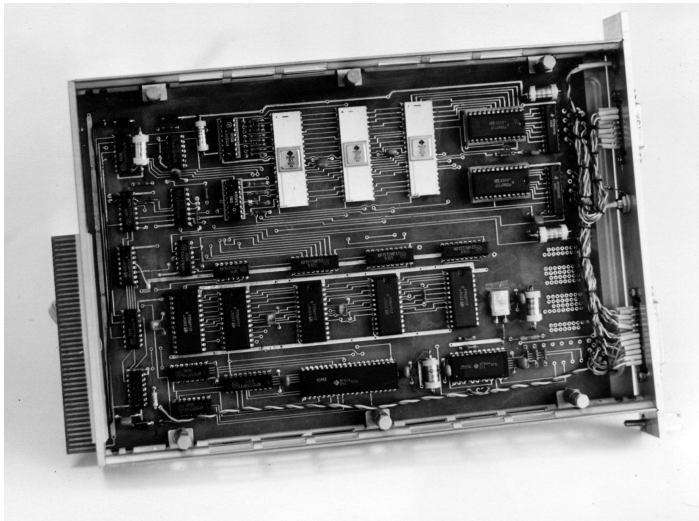
- **1981.** The first CCD Camera with 320 x 288 front illuminated surface channel CCD



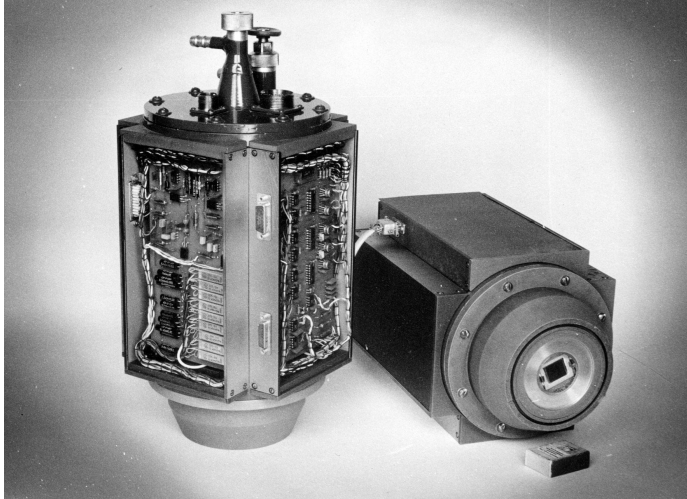
- **1984.** CCD Camera with 512 x 576 front illuminated surface channel CCD



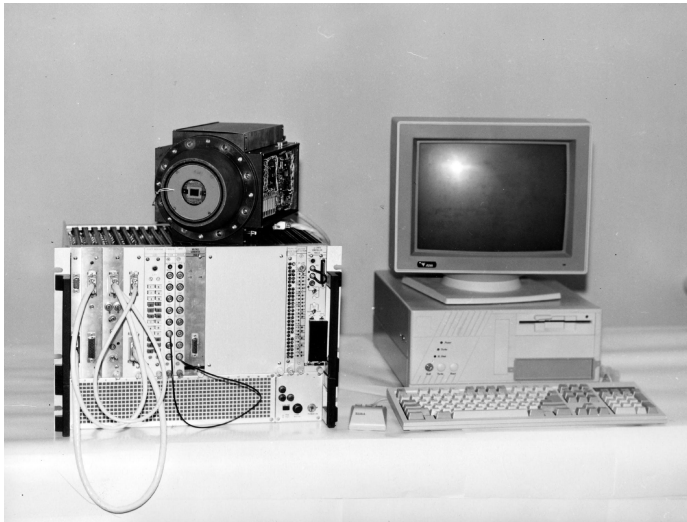
- **1984.** Generation I CCD Controller with control computer



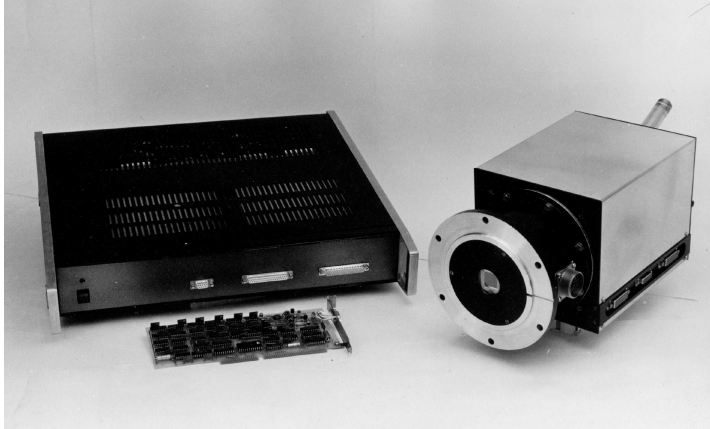
- **1985.** First application of bit-slice processor in Generation II CCD Controller



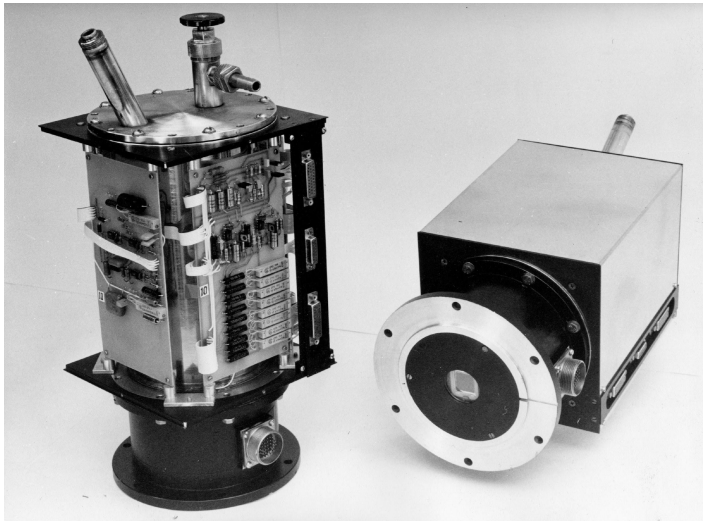
- **1985.** LN2 CCD Camera with 520 x 580 front illuminated CCD with buried channel



- **1985.** Generation II CCD Controller based on bit-slice processor



- **1994.** Generation III CCD Controller with embedded Intel 8080 microcomputer



- **1994.** LN2 CCD Cameras with 1K x 1K and 2K x 2K CCDs



- **2000.** DINACON - New Generation DSP based CCD Controller for ultra low noise and high precision imaging



- **2000.** LN2 Dewars for up to 4K x 4K CCDs

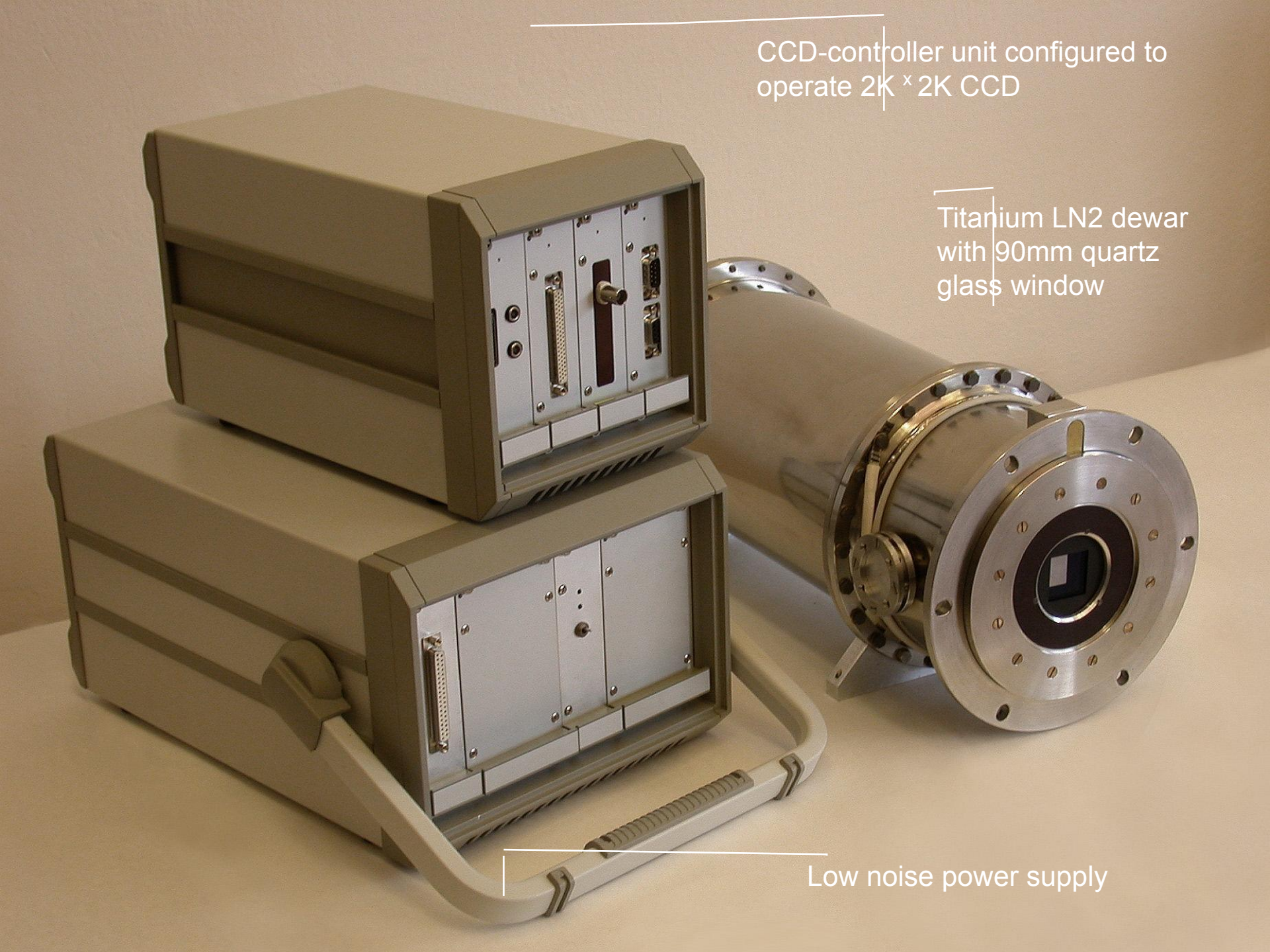
Novelty

- Optimal filtering of video signal
- Digital correction of bias and gain instabilities and non-linearity
- Flexible multiprocessor architecture with multitasking RTOS

Advantages

- Minimum readout noise
- Very high stability and linearity of CCD System transfer characteristic
- High dynamical range
- Easy to control the complex mosaic and infrared detectors

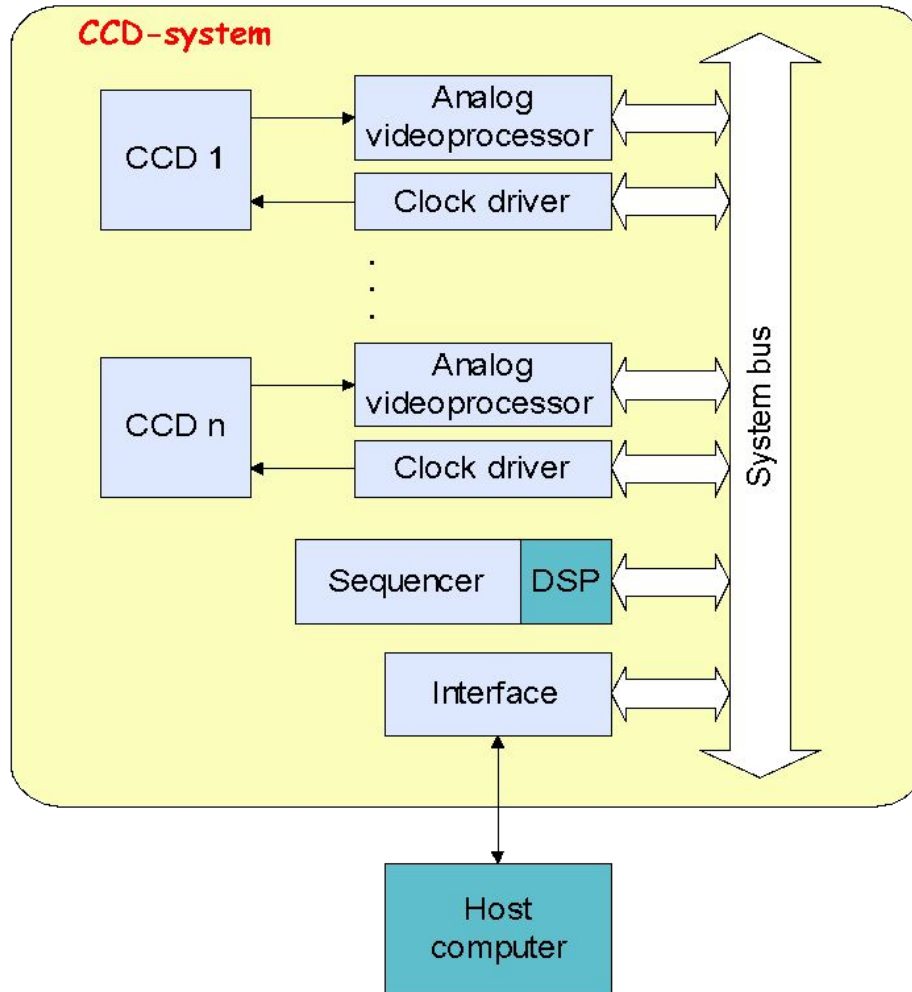
Generation IV CCD controller DINACON: DSP based Intelligent Array Controller



CCD-controller unit configured to
operate $2K \times 2K$ CCD

Titanium LN2 dewar
with 90mm quartz
glass window

Low noise power supply

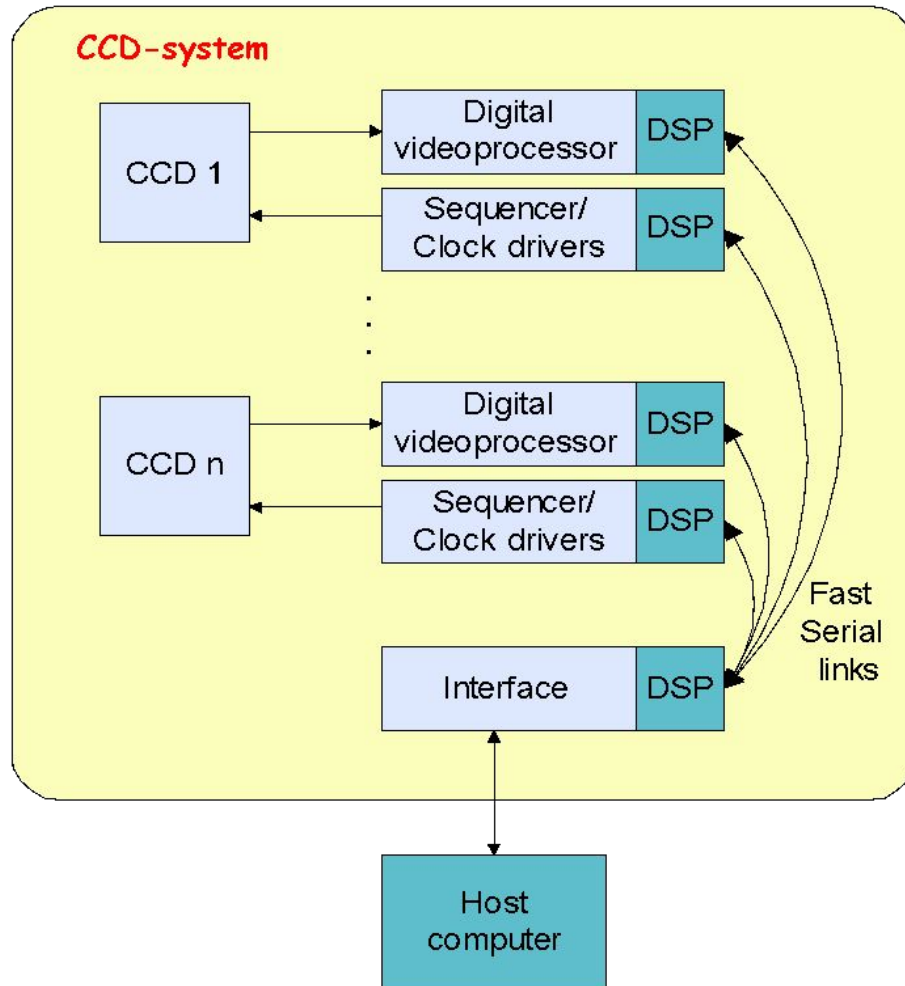


Advantages

- relative simplicity
- multichannel operations

Limitations

- incomplete noise filtering
- noisy system bus
- limited number of channels ($n < 16$)
- low level of flexibility and intelligent functions

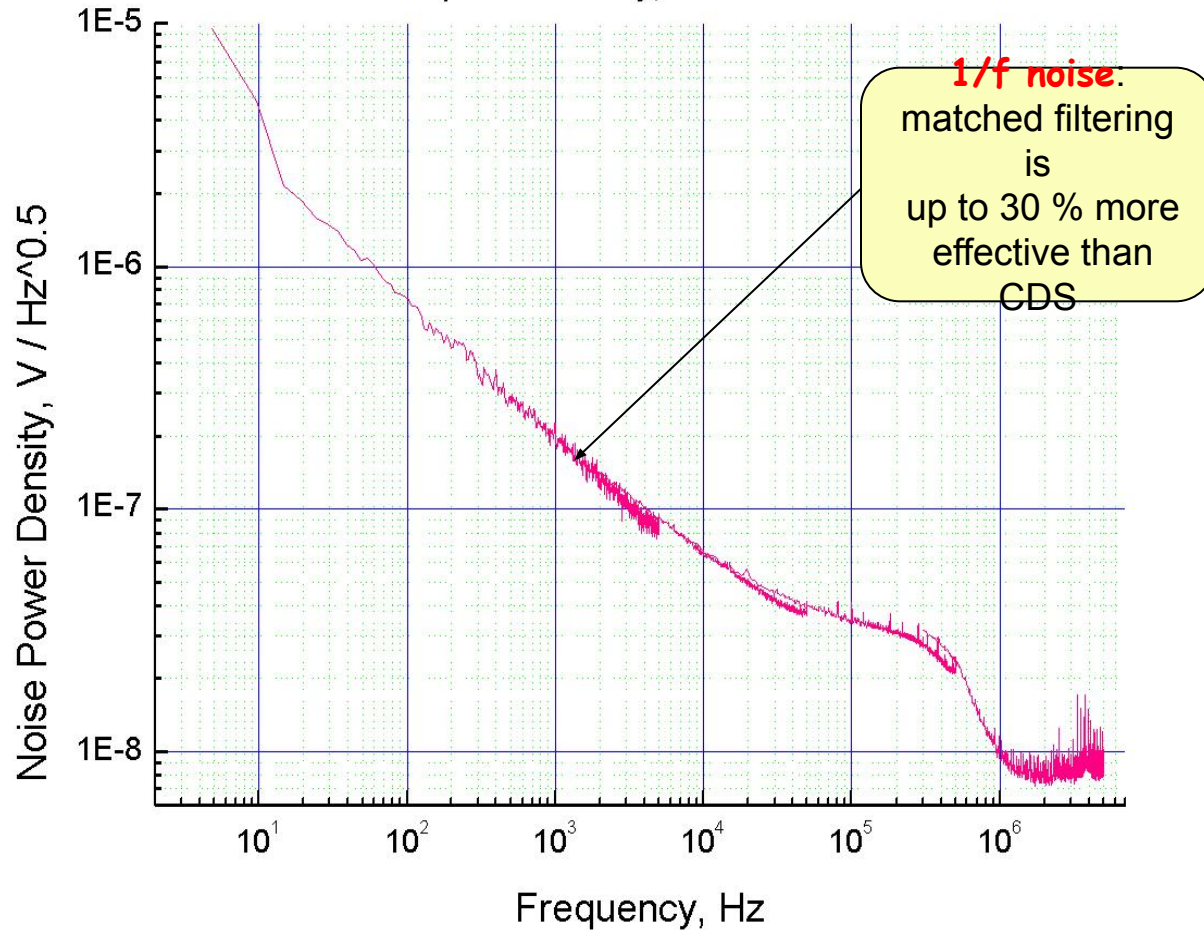


Advantages

- ultralow noise through matched filtering
- no noisy system bus
- higher precision and accuracy
- flexible star- or tree-type topology
- number of channels up to 32
- high level of intelligent functions

Why need matched filtering?

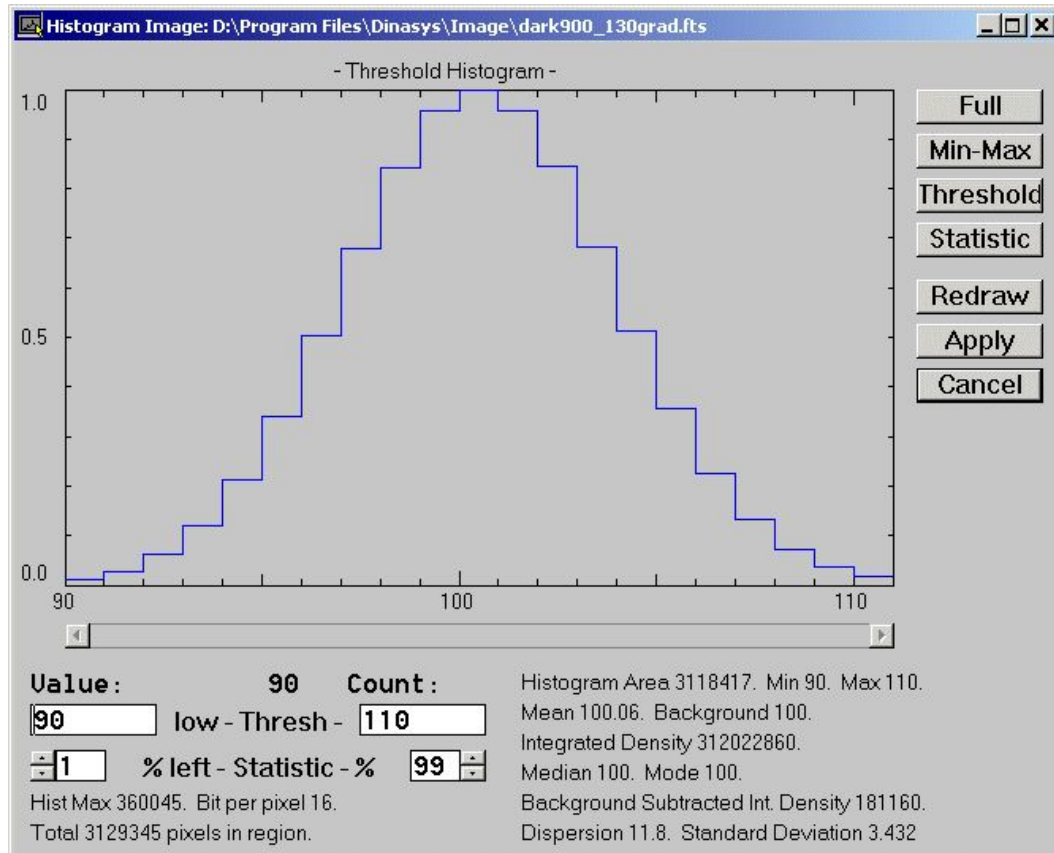
DINACAM EEV CCD42-40 2K x 2K
Noise power density, Node A



- Readout noise reduction: $2.5 \text{ e} \rightarrow 1.7 \text{ e}$
- Photometric instability: $0.03\% / 24 \text{ h}$
- Nonlinearity reduction: $1.00\% \rightarrow 0.03\%$

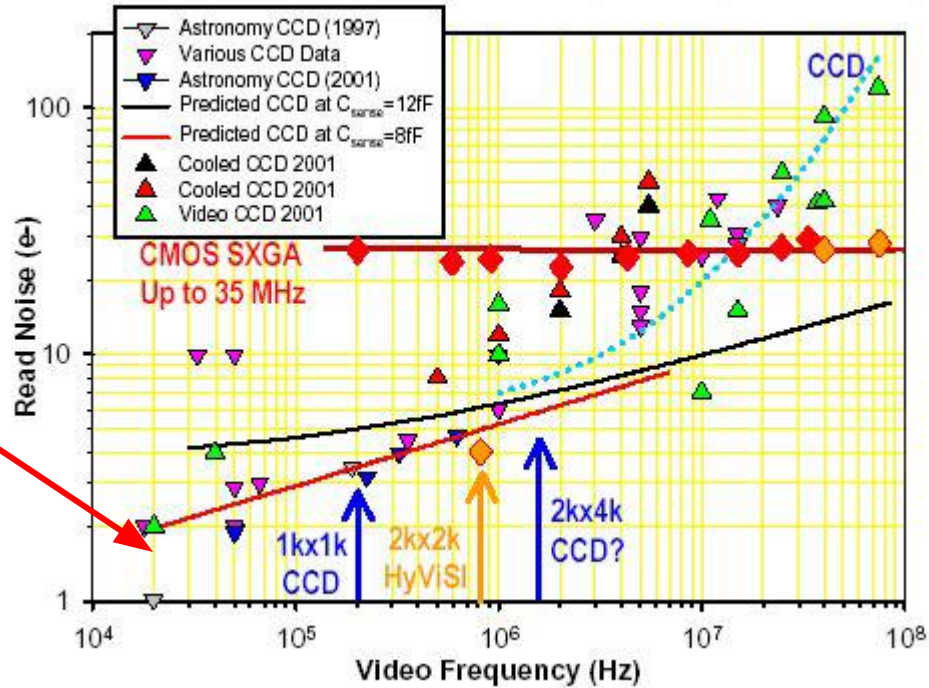
Literature:

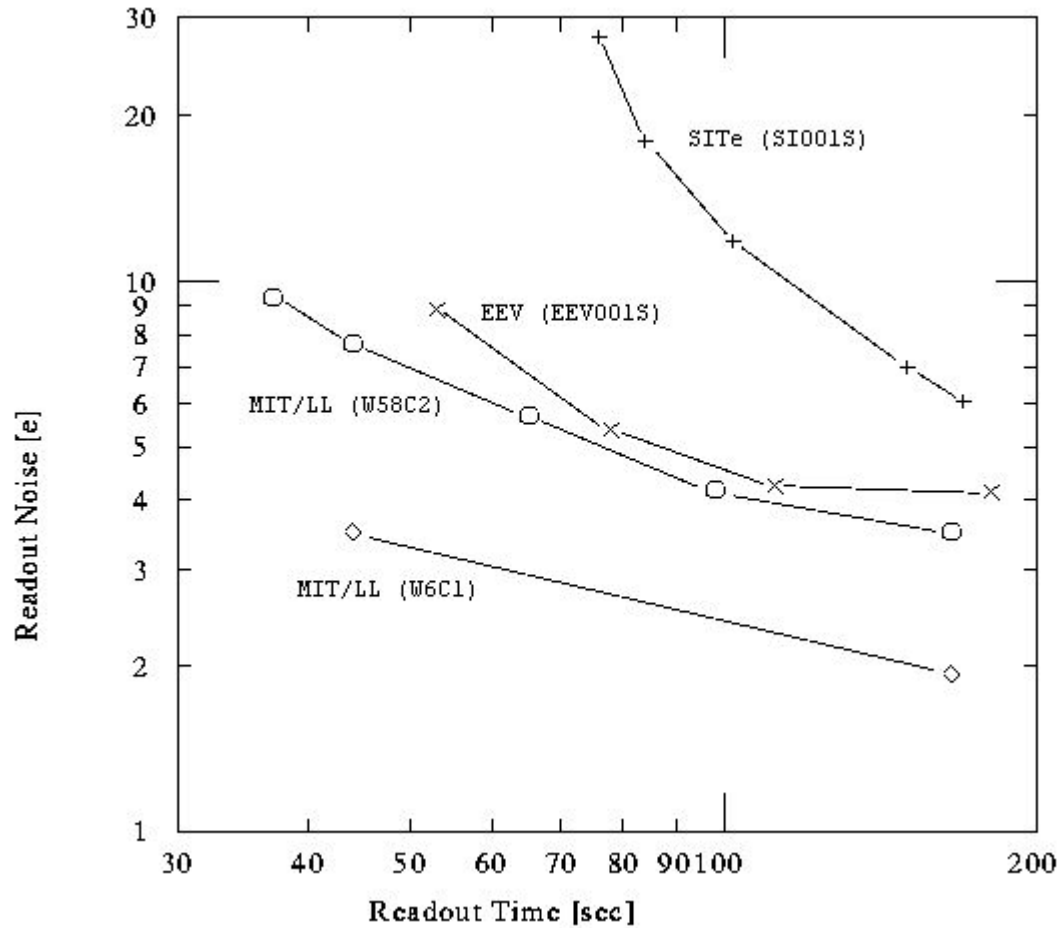
- Buffington et al., 1990:
Instability = 0,3 % , $\Delta t = 10 \text{ h}$, at room temperature
- Robinson et al., 1995:
Instability = 0,5 % , $\Delta t = 10 \text{ days}$, at stabilized temperature

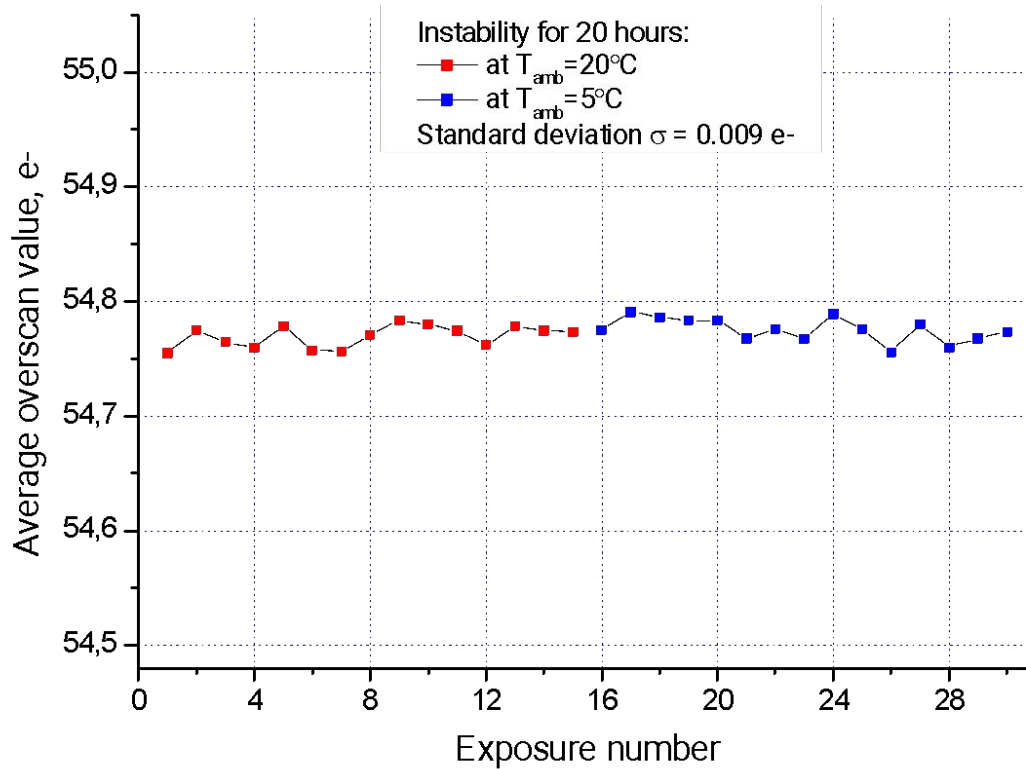


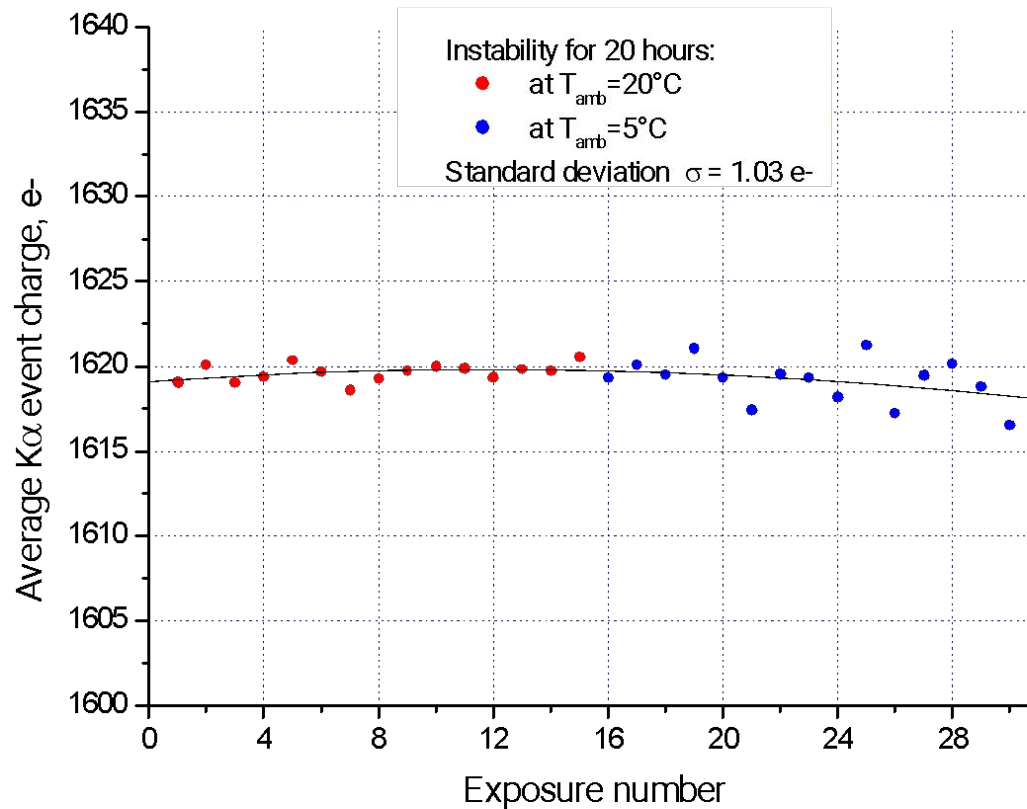
- ADU = 0.5 e
- Readout rate = 18 kHz
- Noise = 1.7 e

SAO's
CCD 42-40

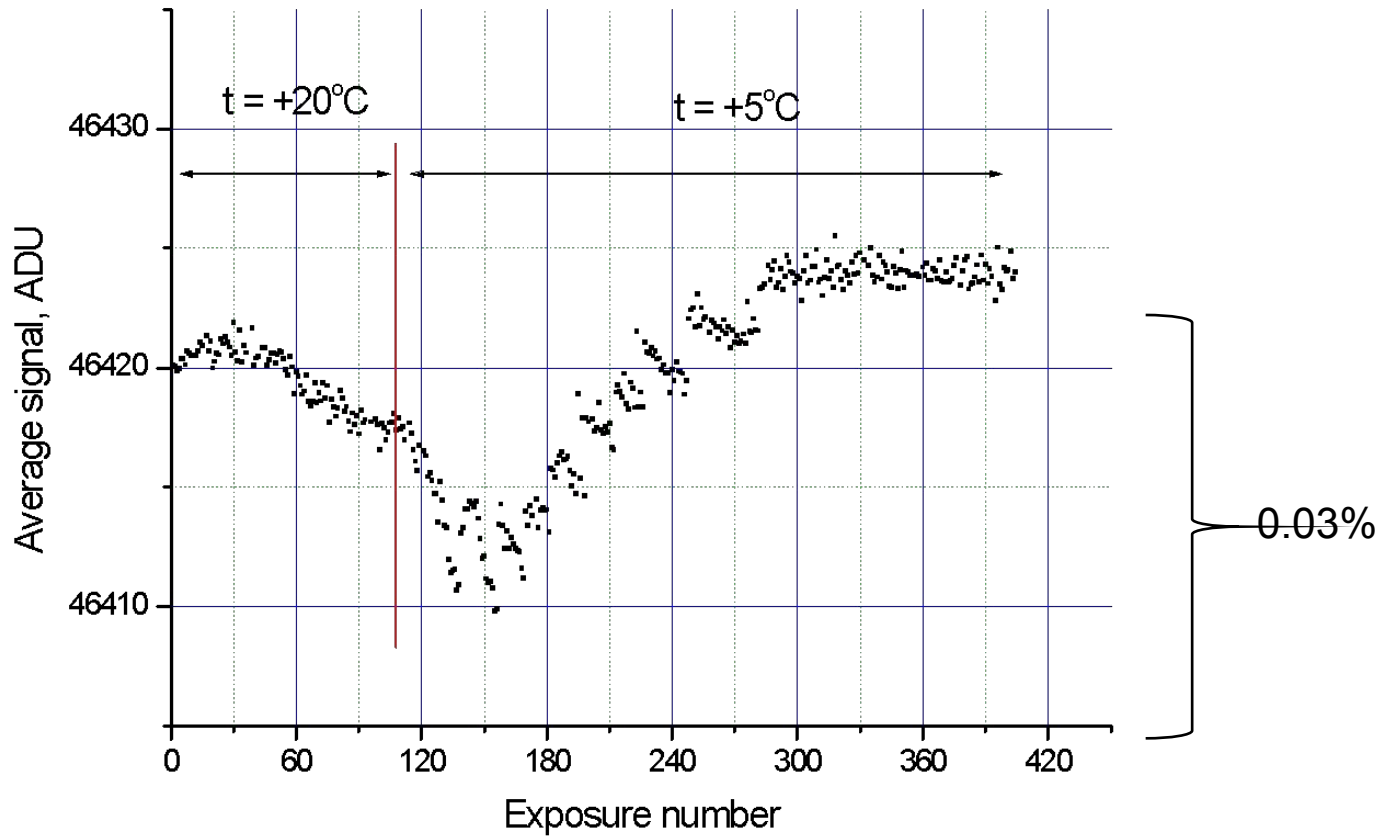




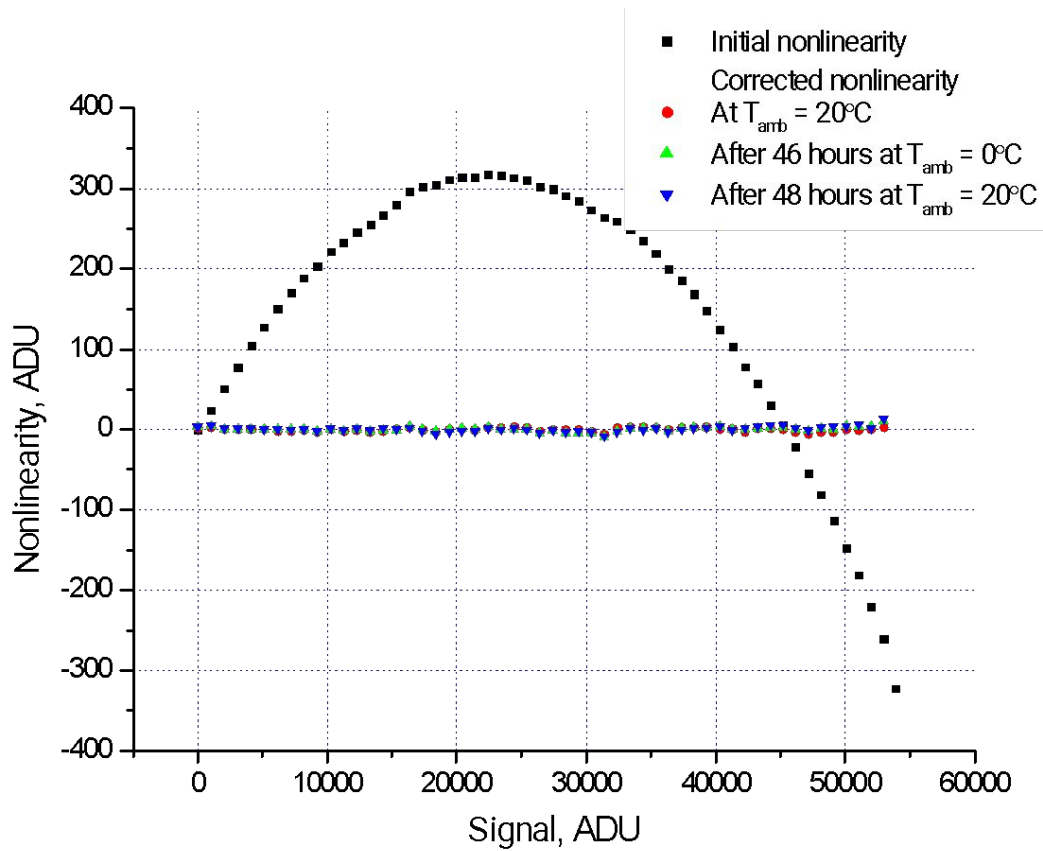




Gain instability at 1620 electrons level measured by means of Fe55

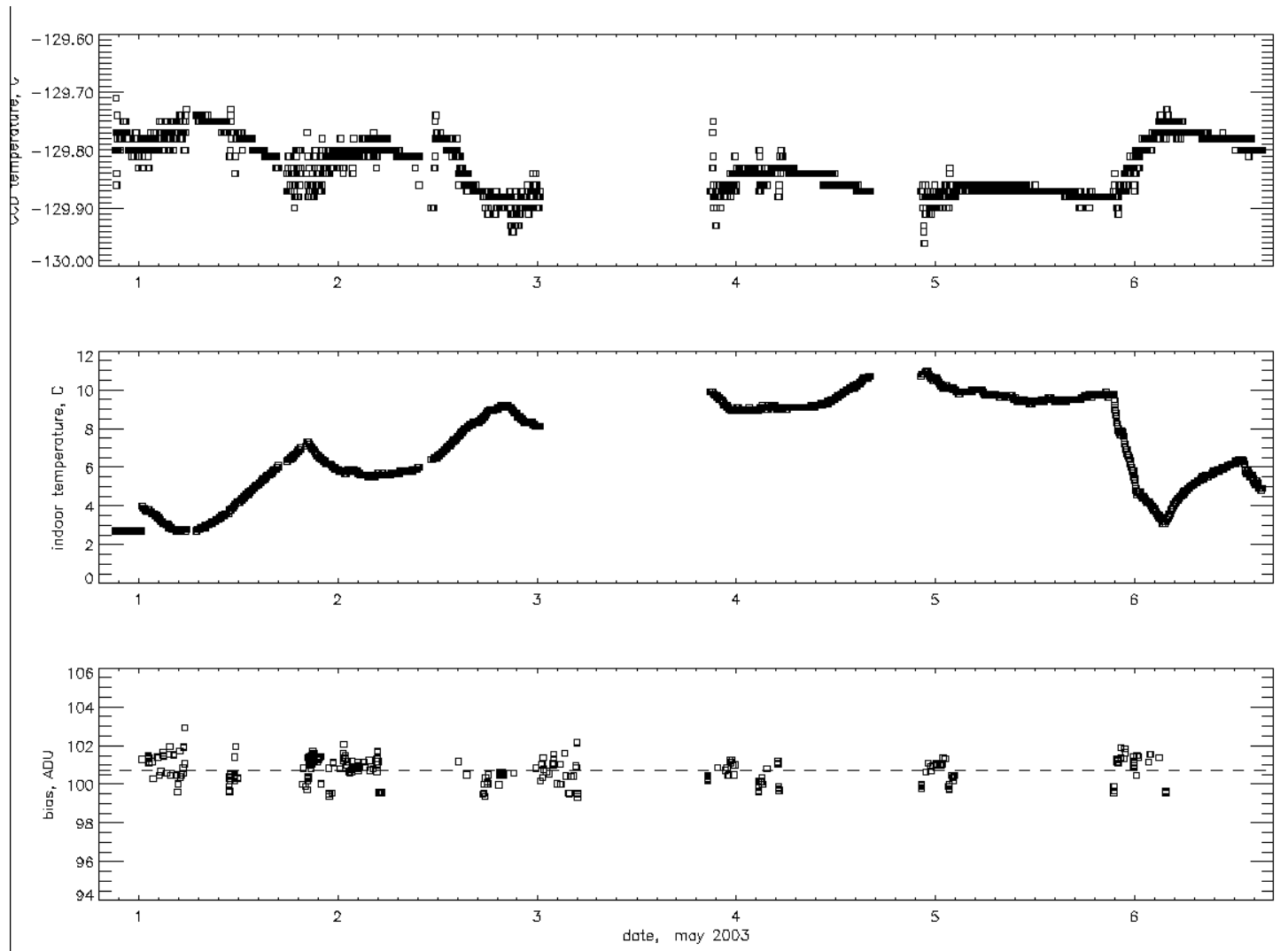


Gain instability measured by means of stable light source



DINACON: Instabilities on telescope

SAO

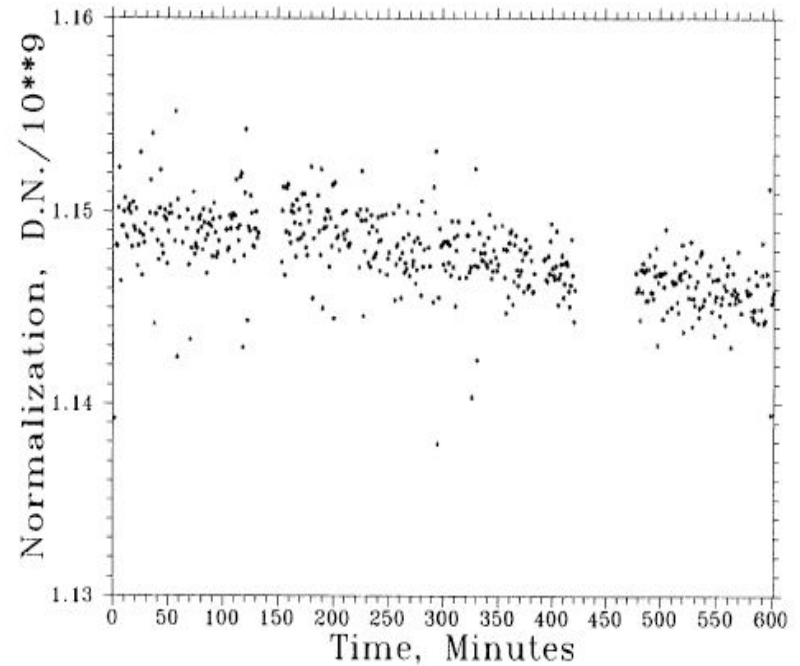
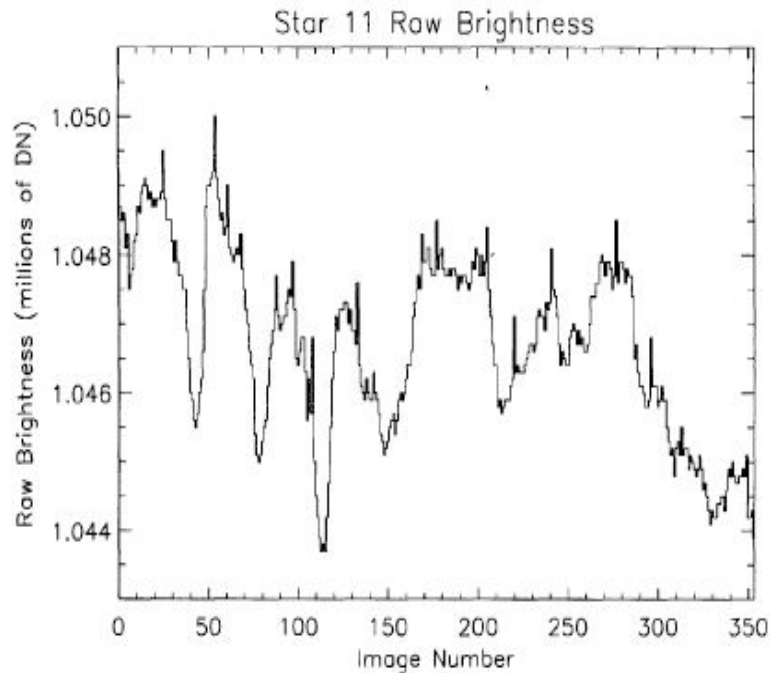


Gain instability: the best results

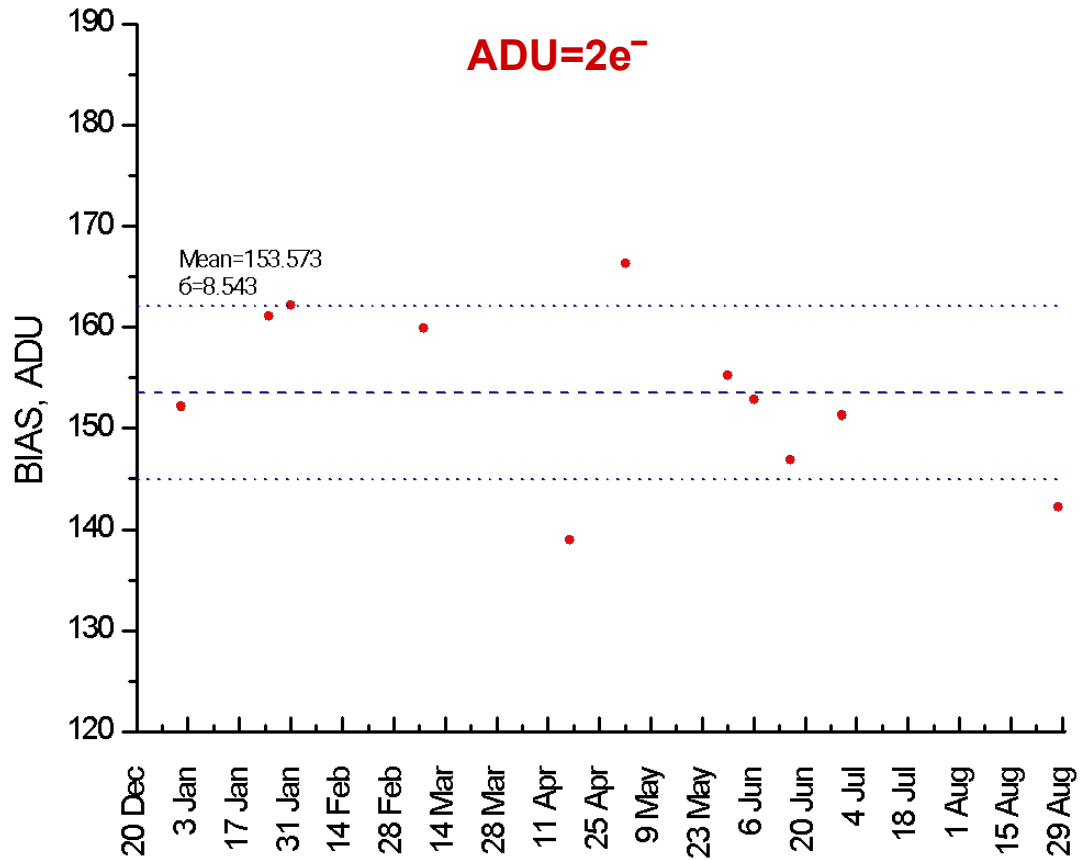
SAO

Robinson et al, 1995: 0.6% p-p
Conditions: room temperature

Buffington et al, 1990: 0.8% p-p
Conditions: stabilized temperature



ESO's FIERA: Long-term bias instability



Instability during 8 months is about 60 electrons p-p

CCD Controllers Comparison

SAO

	SDSU-II (SDSU)	FIERA (ESO)	Arcon (NOAO)	DINACON I (SAO)
Architecture				
Embedded computer	no	yes	no	no
Processor type	DSP56002, 24 bit, 40 ns/instr.	TMS320C40, 32 bit, 20 ns/instr.	TRAM , 16/32 bit, 50 ns/instr.	ADSP2160, 32 bit, 25 ns/instr.
Multiprocessing	no	2 processors	yes	yes
Topology	-	linear	star	star or tree
Interprocessor connections	-	common bus	4 port/processor, 20 bit/s/port	5 port/processor, 160 Mbit/s/port
External communications	SCSI 12 MB/s, fiber 5 MB/s	fiber 128 MB/s	fiber 4 MB/s	fiber 10 MB/s, Ethernet 1 MB/s
Embedded memory	32 KB	-	-	8 MB
Signal processing				
Type of signal processing	analog	analog	analog	digital
Number of ports (videochannels)	1 – 32	2-32	4-16	2 - 64
Dynamical range, bit	16	16 (21)	16	18 - 20
Max. pixel rate, Mpixel/s/port	1.0	2.0 (5.5)	0.4	2.5
Internal noise (at 1 Mpixel/s), e-	-	1.3	-	< 1
Buffer memory, MB/port	external	-	0.064	8
Transfer characteristic correction	no	no	no	yes
Detector control				
Max. number of channels	16	16	4	32
Time resolution, ns	40	20	40	25
Amplitude resolution, bit	12	16	-	12
Control clocks per channel	24	-	28	48
Bias voltages per channel	8	-	16	20

CCD Controllers Comparison

SAO

Property	SDSU-II (SDSU)	FIERA (ESO)	Arcon (NOAO)	DINACON (SAO)
Controller architecture				
Modularity	+	+	+	+
Expandability	+	+	-	+
Detector control				
Program setting of clock parameters	+	+	+	+
Clock telemetry	-	+	-	+
Program setting of output stage mode	-	-	-	+
Telemetry of output stage mode	-	-	-	+
Program setting of CCD temperature	+	+	+	+
Telemetry of CCD temperature	+	+	+	+
Programming of optional storing and readout modes	-	-	-	+
Videoprocessing				
Multichannel processing	+	+	+	+
Digital matched noise filtering	-	-	-	+
Measuring of noise spectrum of output stage	-	-	-	+
Auto-calibration and correction of transfer function of video channel	-	-	-	+
Extended dynamic range of video-channel (> 16 бит)	-	+	-	+

- System controller with communication adapter
- Sequencer with drivers
- Videoprocessor
- Peripheral controller

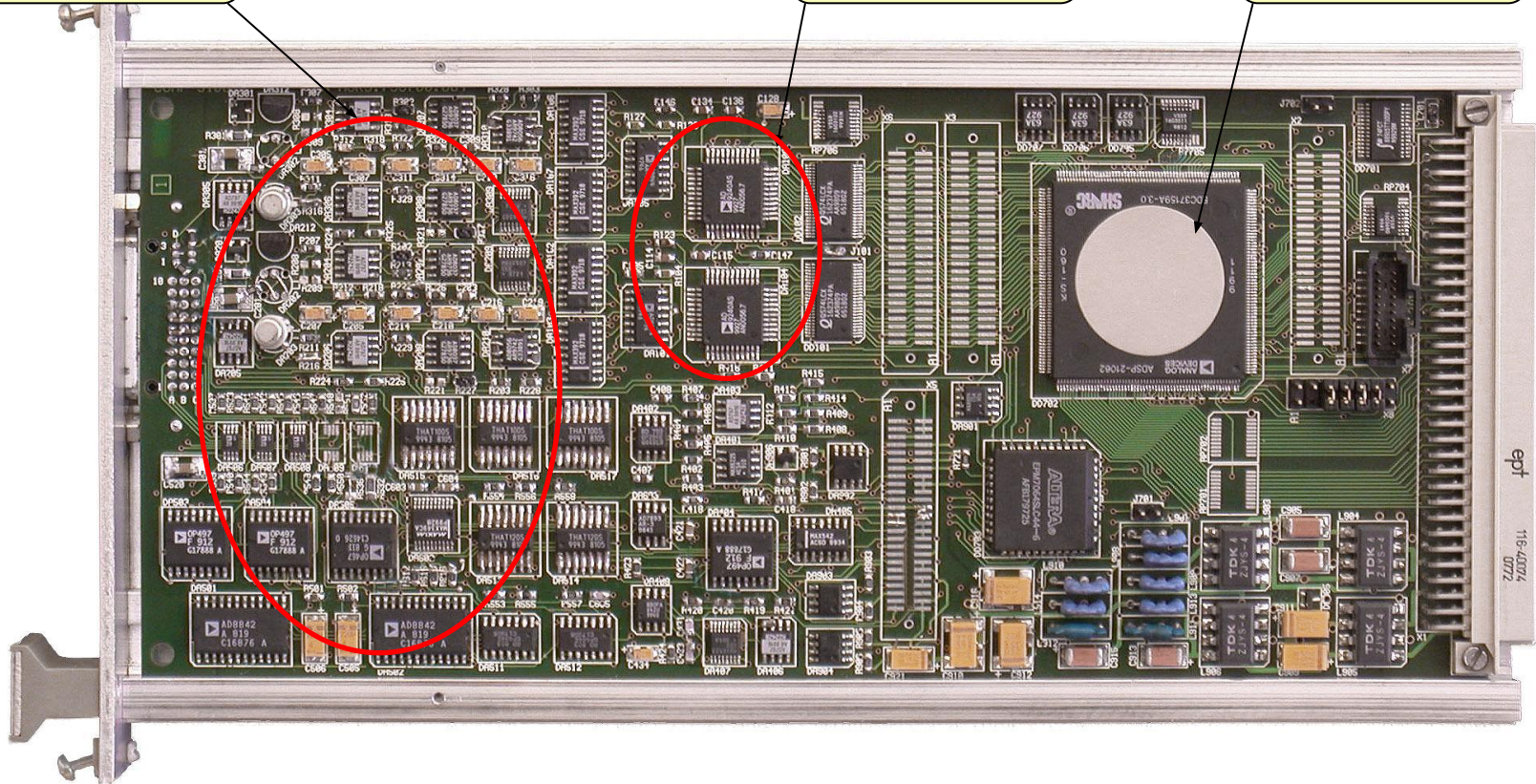
DINACON I: Videoprocessor

SAO

CCD's output
nodes
control unit

Two 14 bit ADCs
10 MHz

32 bit DSP
40 MIPS

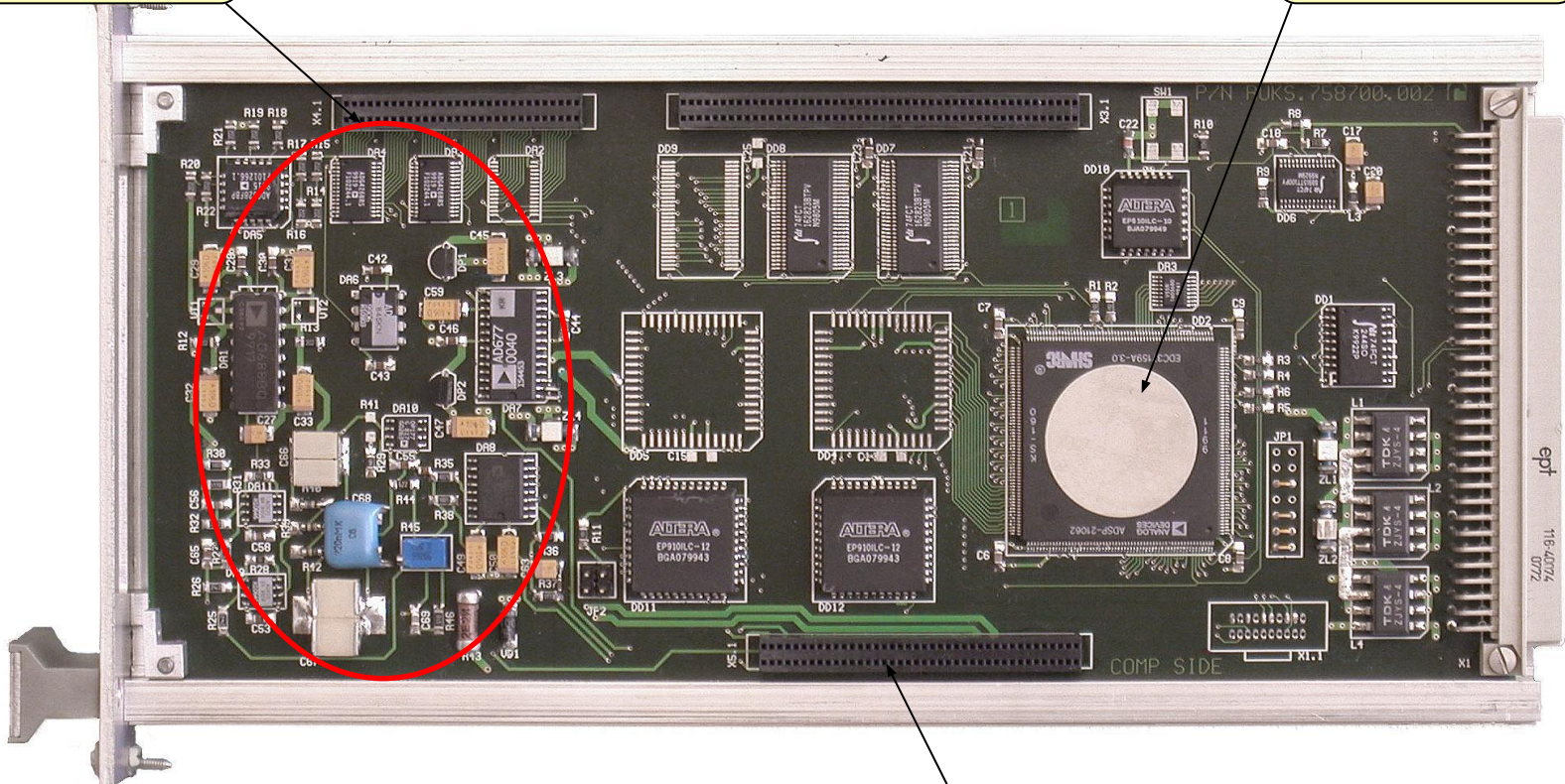


DINACON I: Sequencer

SAO

Telemetry unit
with 16 bit ADC

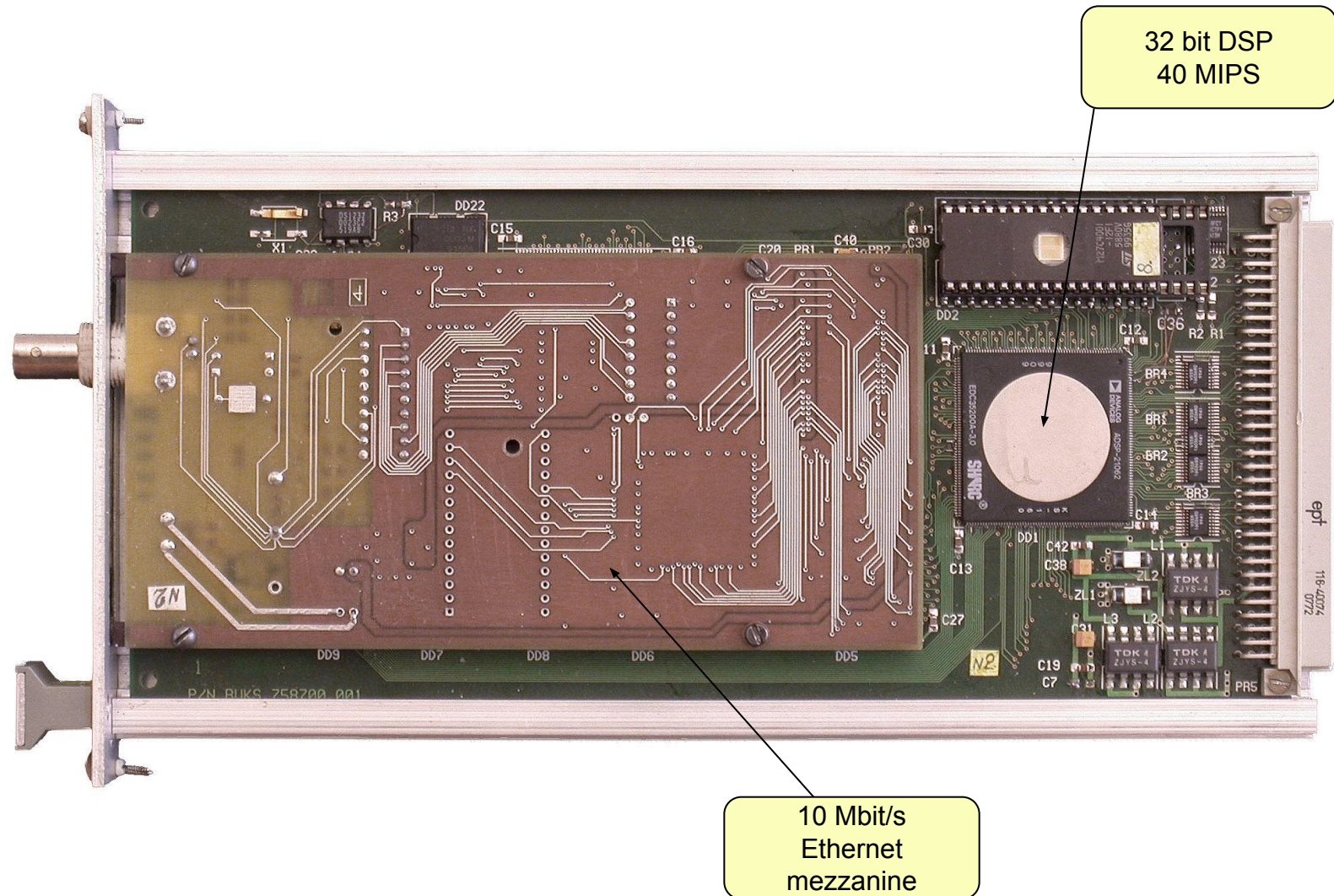
32 bit DSP
40 MIPS



Mezzanine
connector

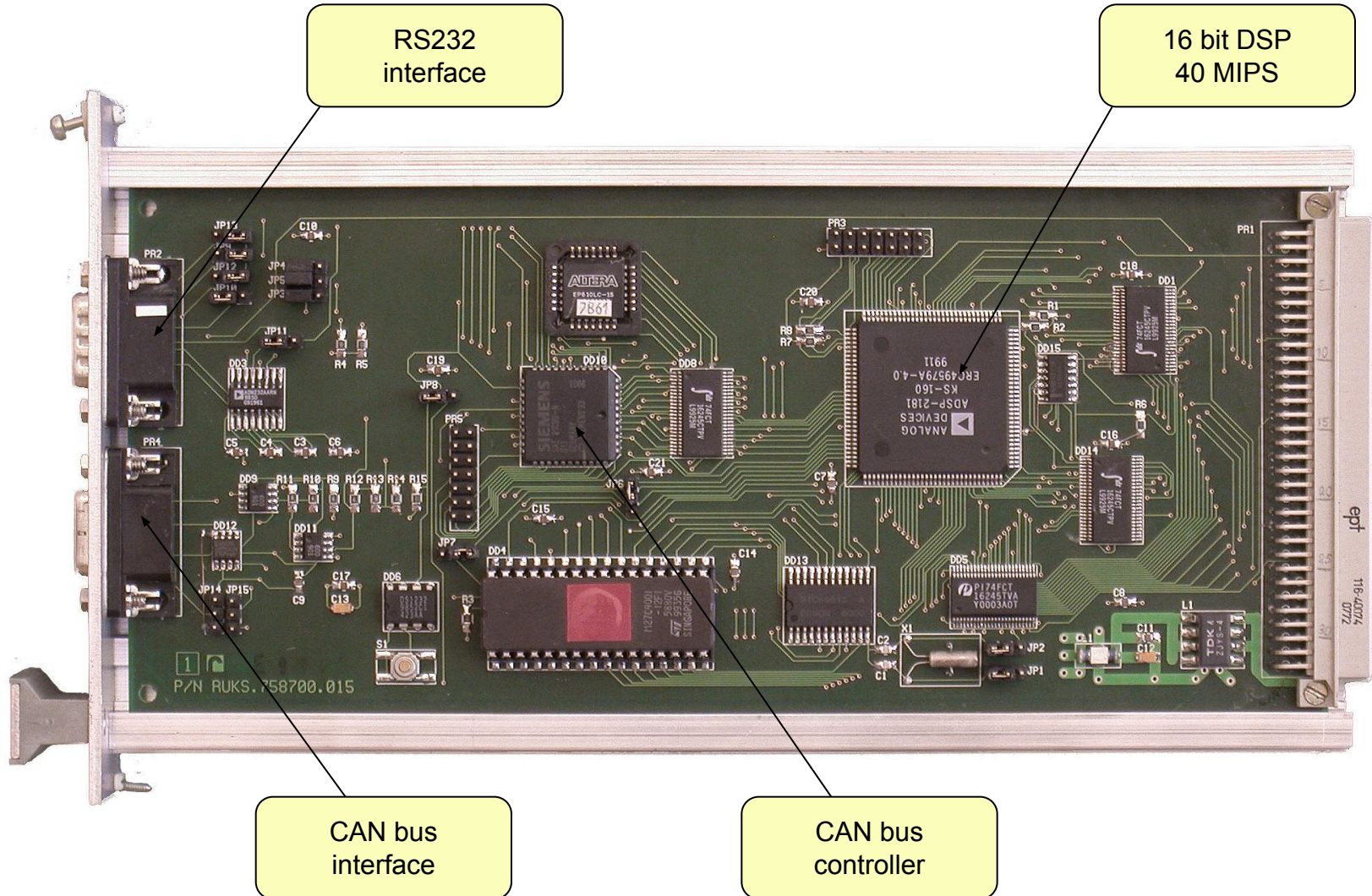
DINACON I: System controller

SAO



DINACON I: Peripheral controller

SAO



The screenshot displays the DINASYS Control Software interface, which is divided into several functional windows:

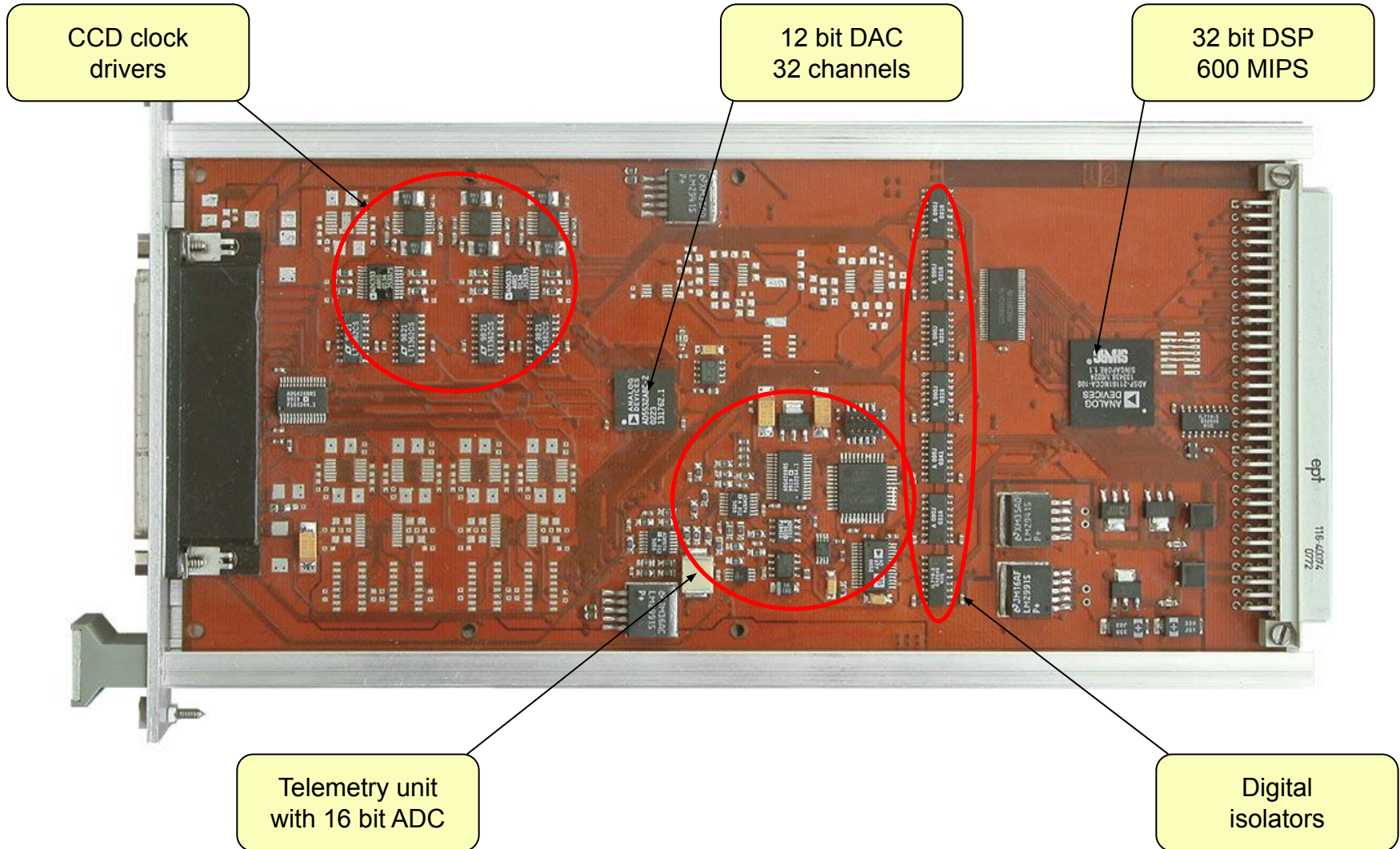
- Exposure Control:** Contains settings for exposure time (1.000 secs), number of lines to read (1000), and observe type (OBJECT). It includes checkboxes for Clear, Enable shutter, Antibloom, Readout, Save, and Display. A Filter number (0-7) is set to 1. Declination is set to 30° 0' 0".
- Control:** Features buttons for Exposure, Power (- OFF -), Mode Standby, Abort, Readout, Stop, Save, Pause, and Display. It also includes fields for Server connection and Status.
- Information:** Shows the next file name (NameNum.ftS) and the acquire directory (d:\program files\dinasys). It includes fields for Name (tmp), Num (7), and Number of exposures (10). The file path is D:\PROGRAM FILES\DINASYS\TMP007.FTS. There are checkboxes for Auto increment file name and Object name, and a field for Number of lines per file (for drift scan) set to 1000.
- Readout options:** Includes Binning X (1) and Binning Y (1) settings, Nodes (A+B), and options for E-Frame, Region, and Sub-regions. Readout rate is set to Fast and Gain is 4 (High).
- Diagram Editor:** Displays a time diagram for various channels (SWL, RGL, FH2L, FH1L, FH3, FH1R, FH2R, RGR, DG, SWR, OG1L, FV2, FV1, FV3, OG1R) with values 0 or 1. Channel 006 (FH2R) is selected.
- Noise Power Density:** A plot showing noise power density versus frequency (Hz) on a logarithmic scale from 1E2 to 1E6.
- Threshold Histogram:** A histogram showing the distribution of pixel values. The x-axis ranges from 3000 to 3400. The y-axis represents the count. The histogram area is 2756, with a minimum of 2800 and a maximum of 3397. The threshold is set to 3400.
- Temperature:** A small window showing chip temperature (0.00 to -135.00) and buttons for Set temperature and Graph.



- System controller with communication adapter
- Sequencer with drivers
- Videoprocessor

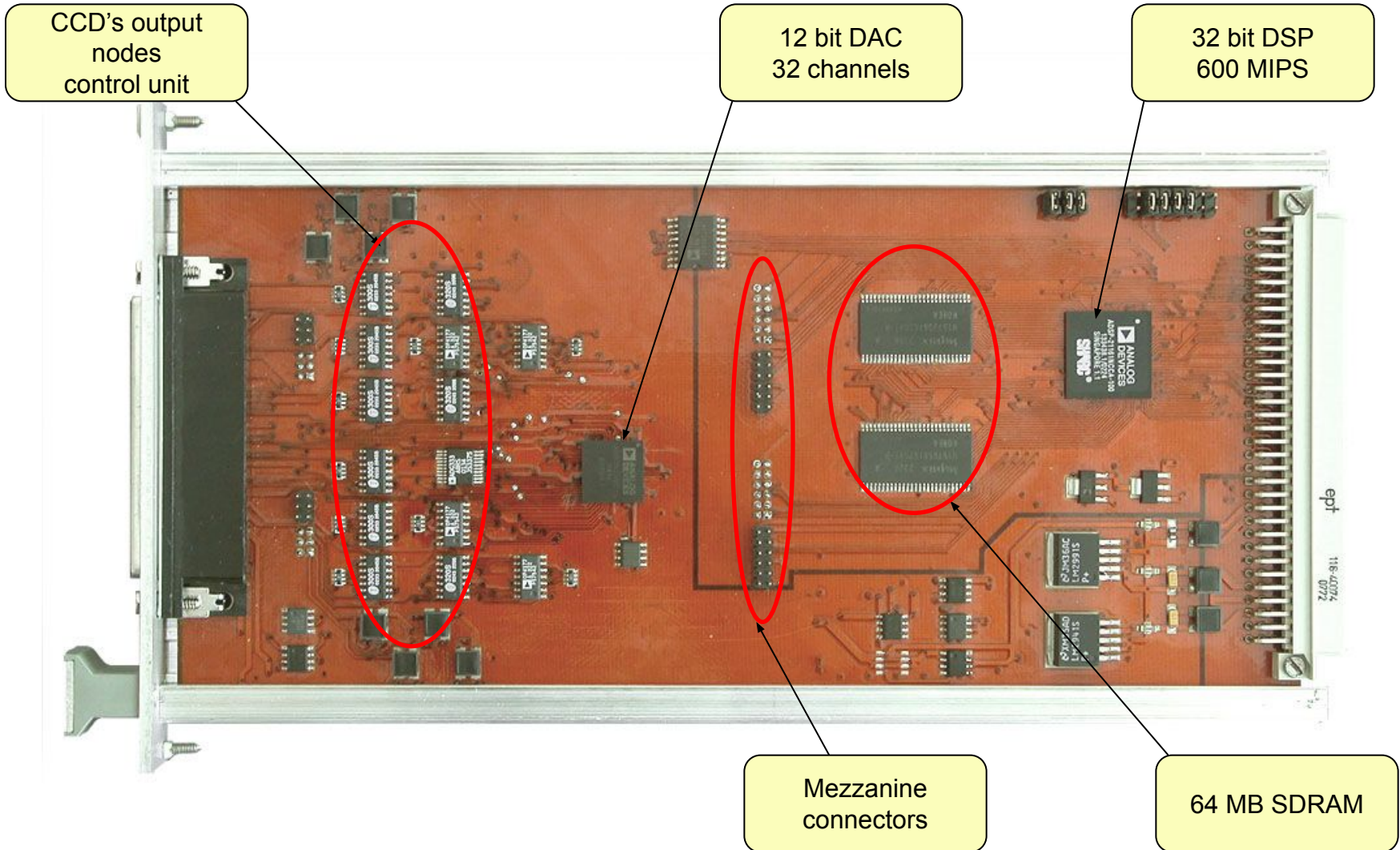
DINACON II: Sequencer

SAO



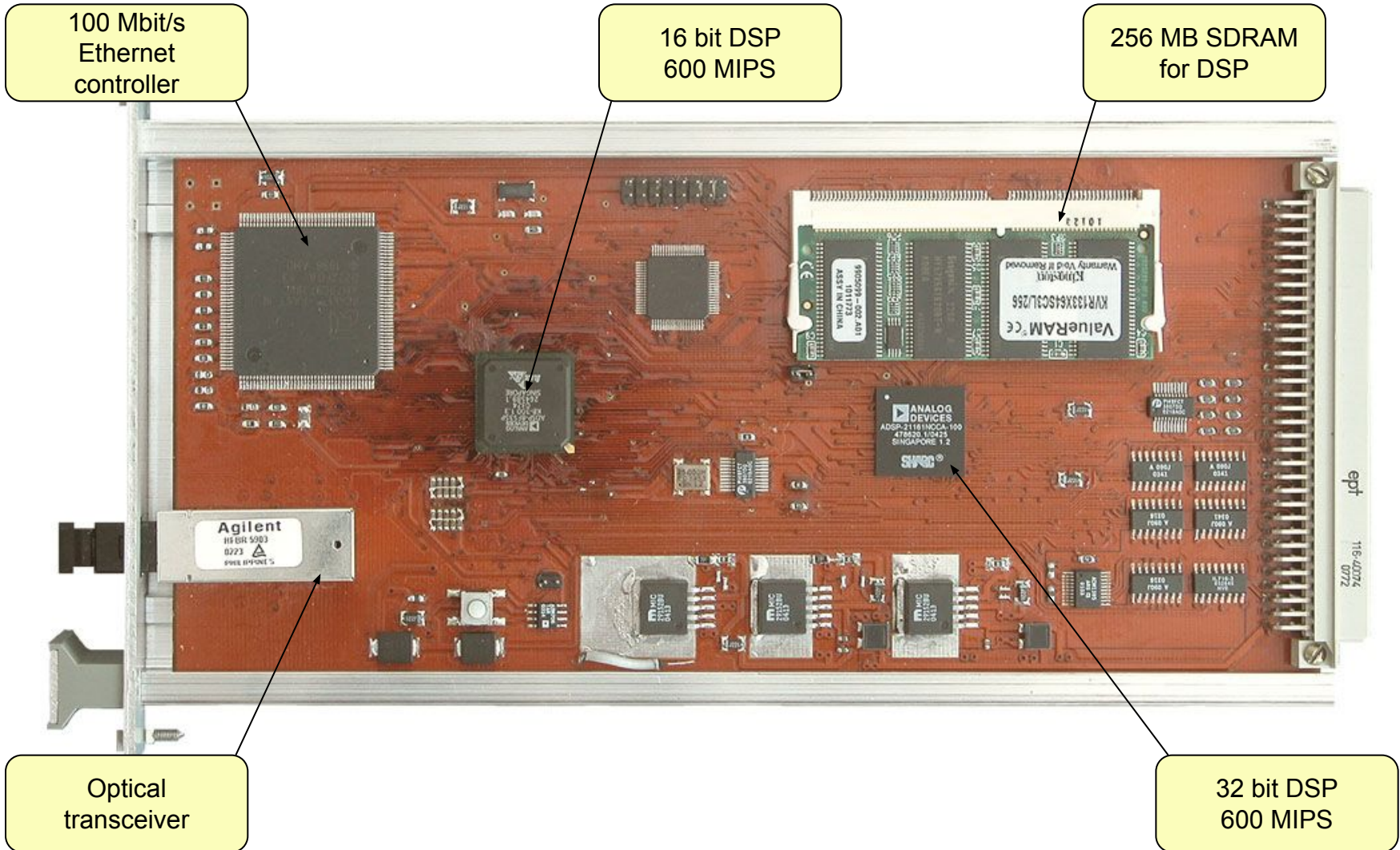
DINACON II: Videoprocessor

SAO



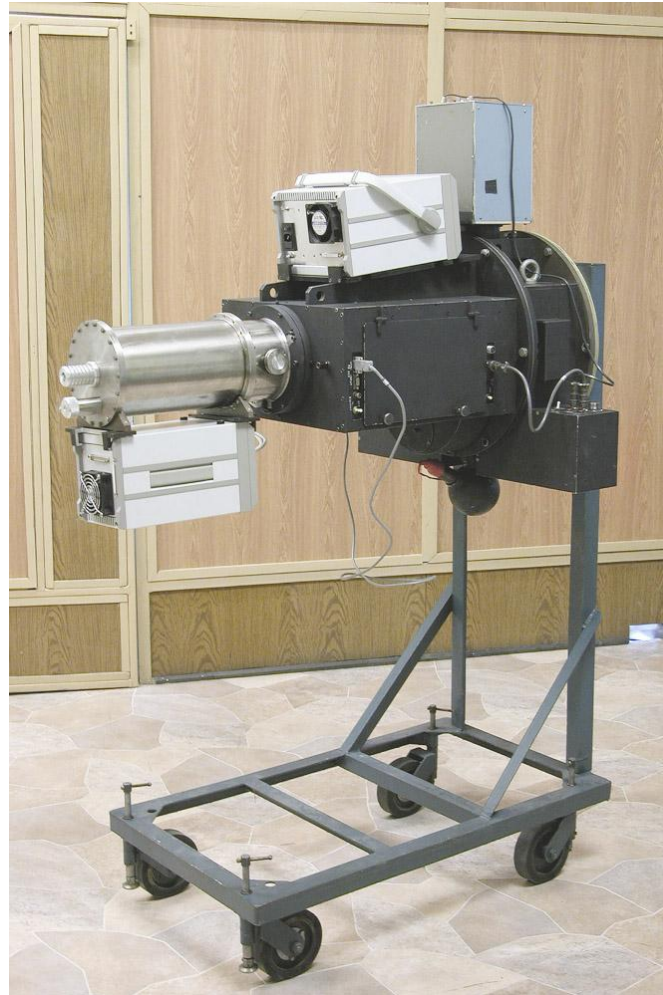
DINACON II: System controller

SAO





DINASYS 2K x 2K on multi-pupil fiber spectrograph MPFS



DINASYS 2K x 2k on multi-mode focal reducer SCORPIO



Camera 2K x 4.5k and controller (without power supply)

Our team

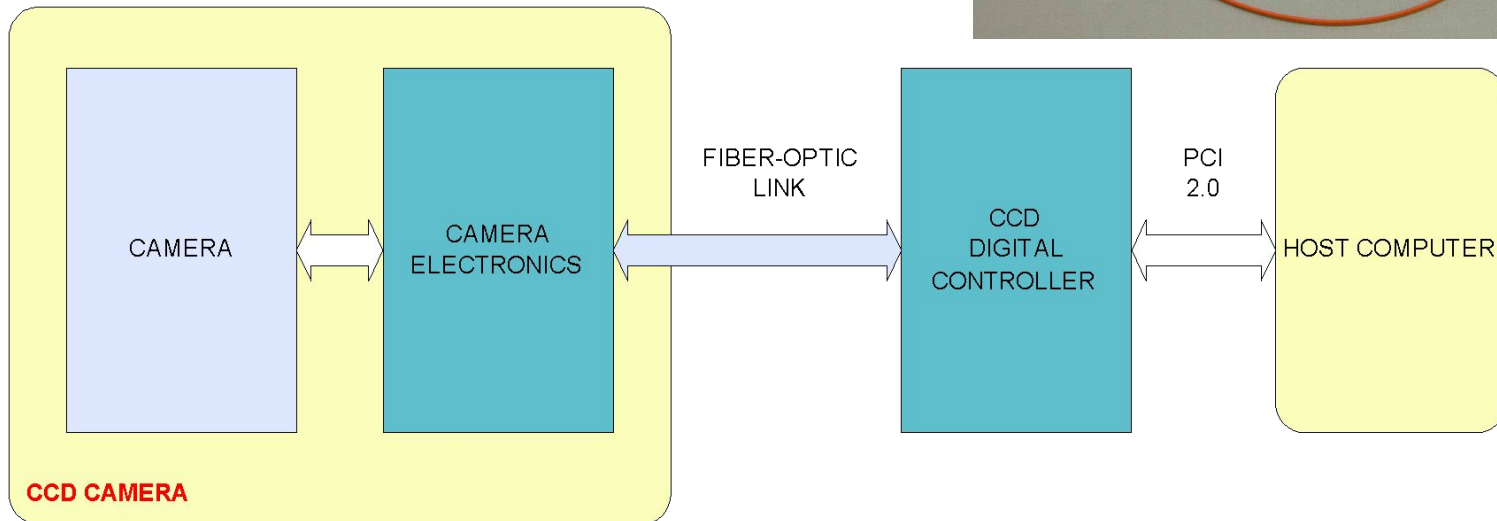
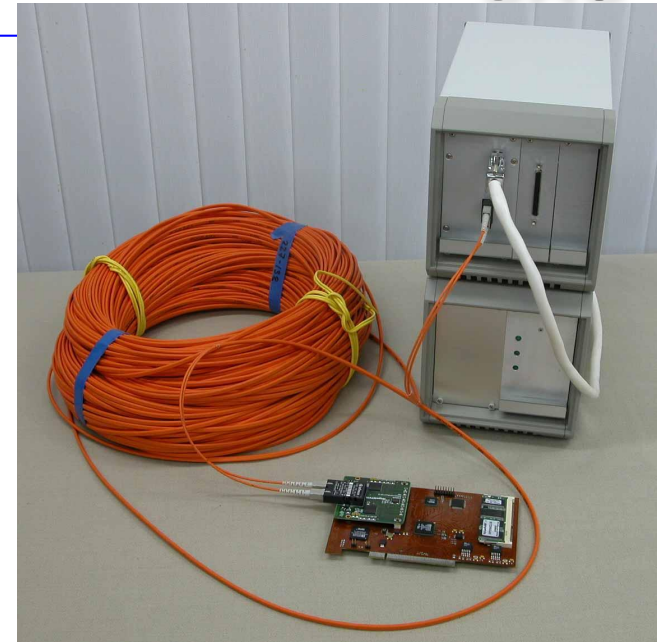
SAO



DINACON III block diagram

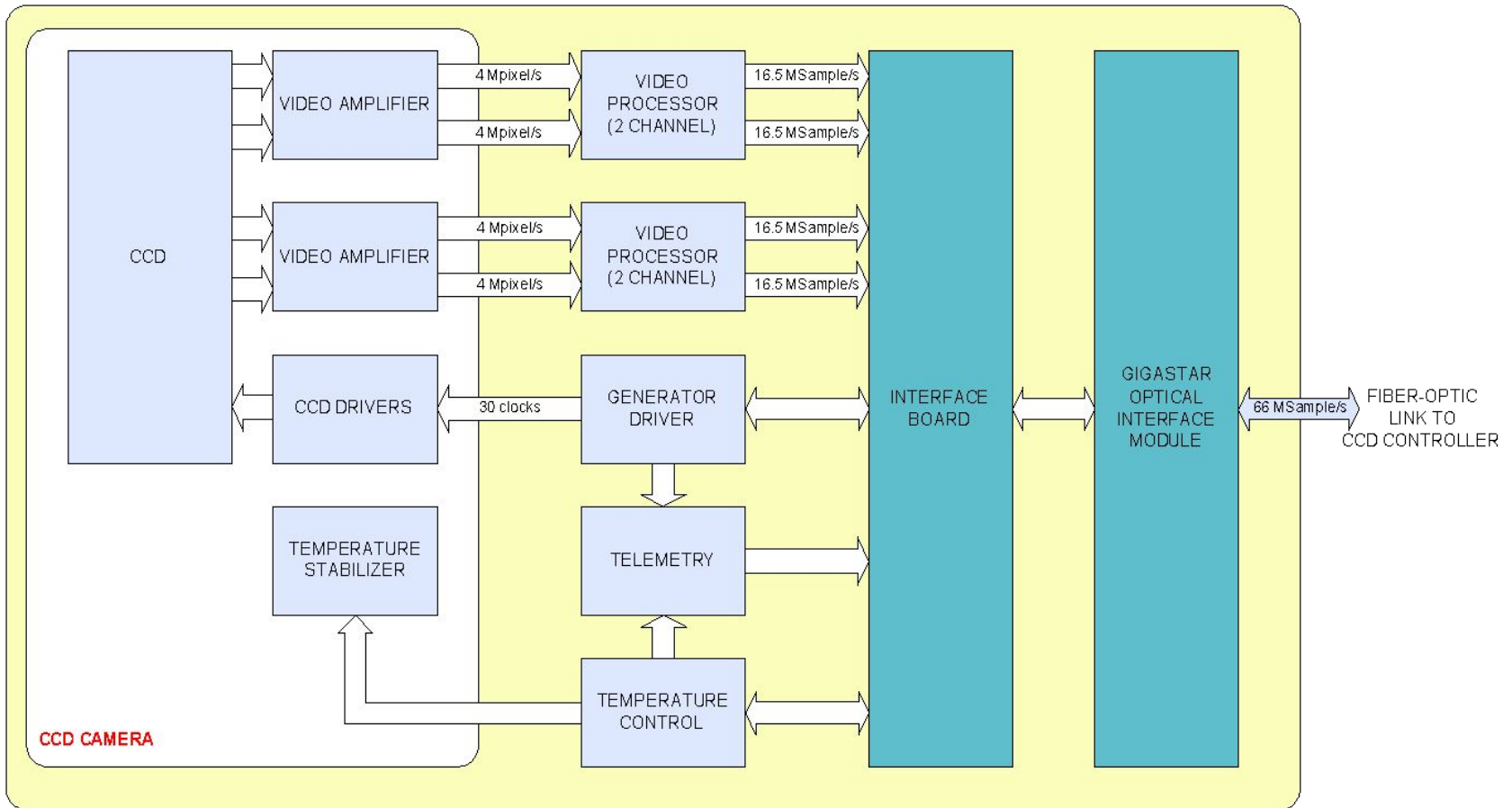
SAO

- Main components:
- **System controller**
- **1 Gbit fiber-optic link**
- **Camera electronics**



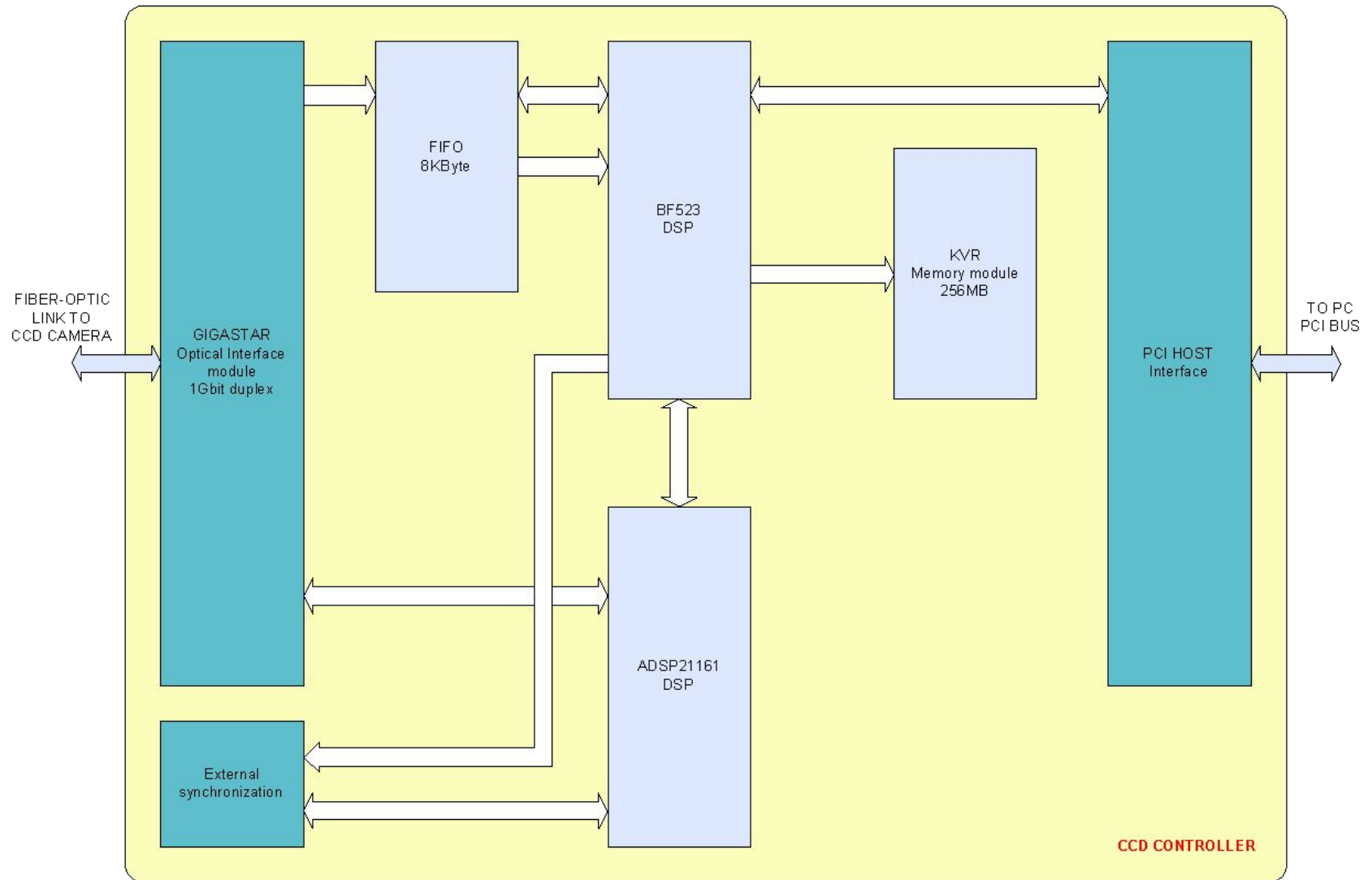
Camera Electronics block diagram

SAO

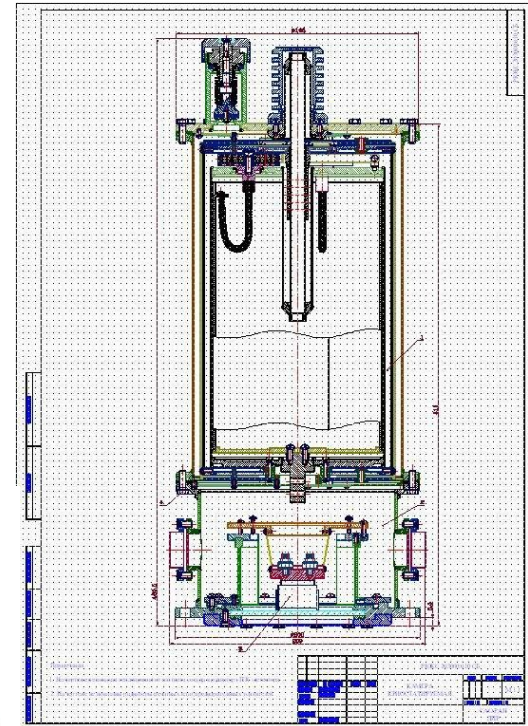
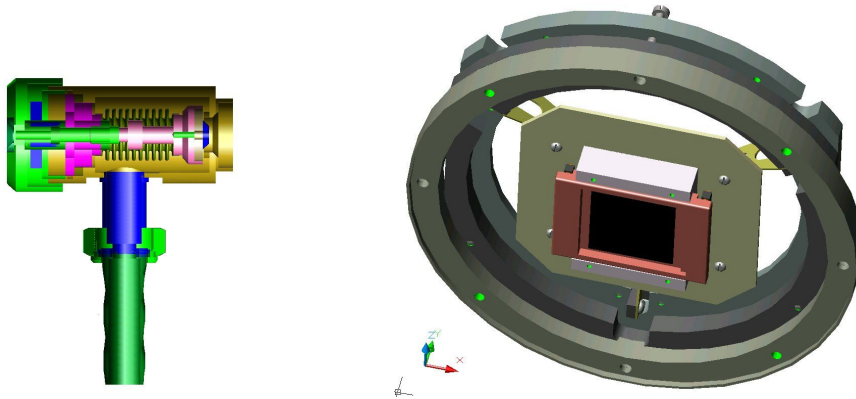


System controller block diagram

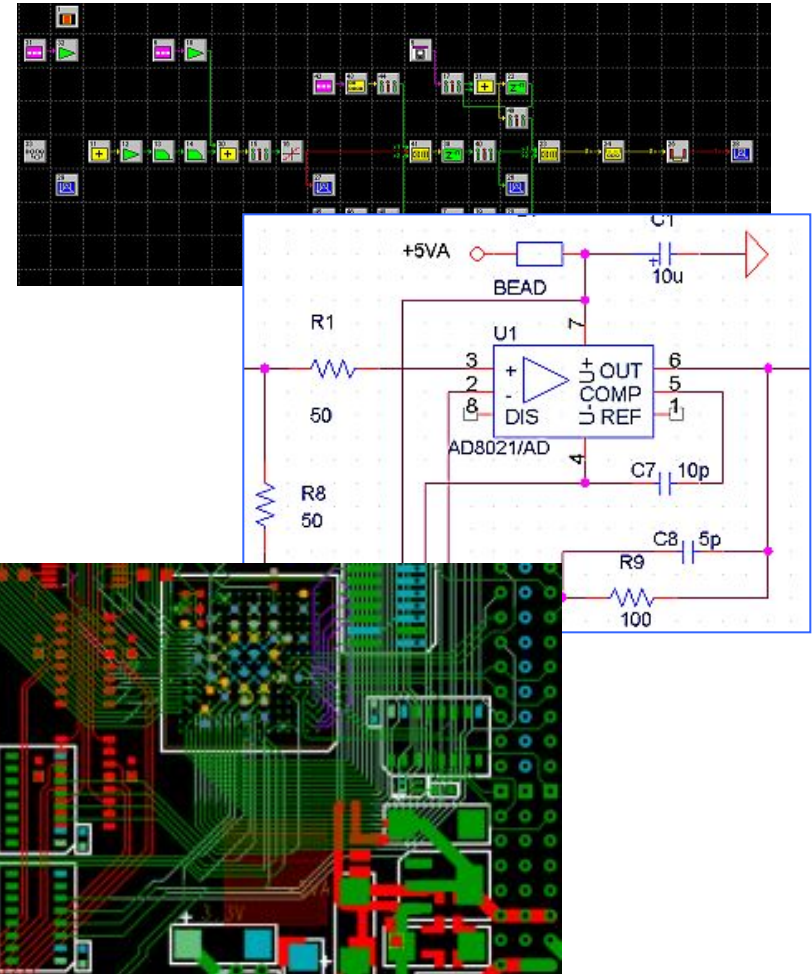
SAO

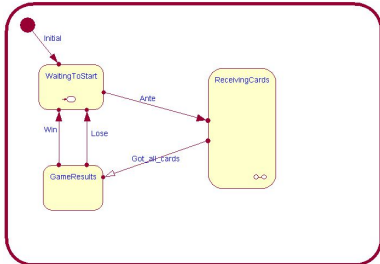


- 2D and 3D computer aided design of CCD systems with release of full design documentation suite
- Structural and thermal simulation of construction units for providing of design requirements



- Detailed mathematical model construction of signals formation and processing for minimization of distortions, noise and instabilities
- Computer aided design of electronics based on IC of all integration levels (including BGA packages) and technology of surface-mount multi-layer PCBs
- Computer simulation and analysis of electronic circuits and PCBs for compliance to electrical, thermal, noise requirements

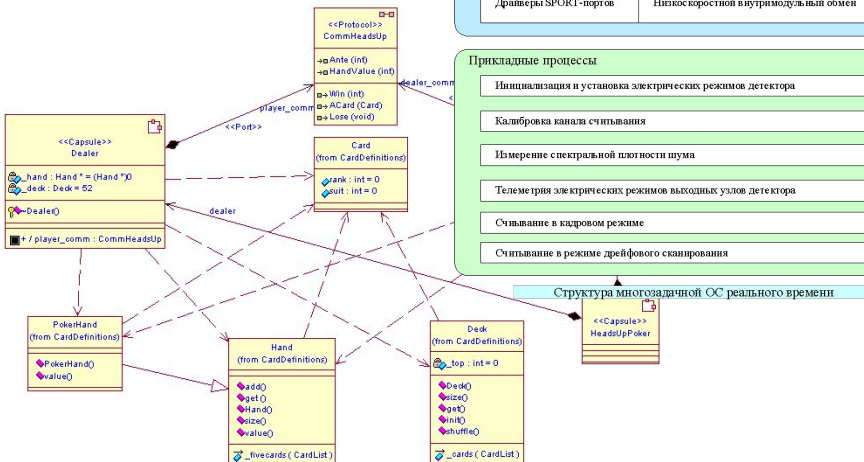




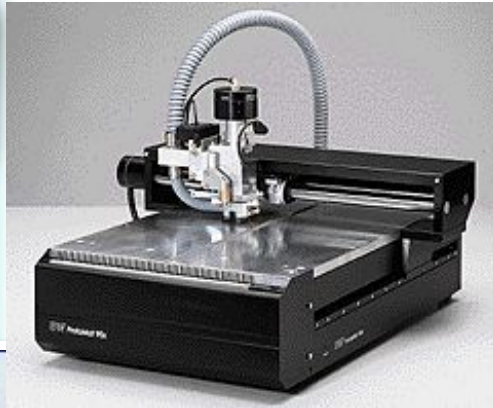
Ядро	
Функции ядра	Механизм сохранения контекста и переключения задач
	Приоритетная диспетчеризация задач
Обработка прерываний	Системное время
	Средства синхронизации задач: семафоры, очереди, сообщения
	Средства межядерной и мекропроцессорной маршрутизации сообщений
	Системный таймер
	Переключение задач
	Ввод-вывод
	Внешние события

Системные процессы	
Супервизор	Приним и исполнение команд Маршрутизация сообщений
Драйверы LNK-портов	Высокоскоростной межмодульный обмен в фоновом режиме ПДЦ
Драйверы SPORT-портов	Низкоскоростной в интрамодульный обмен

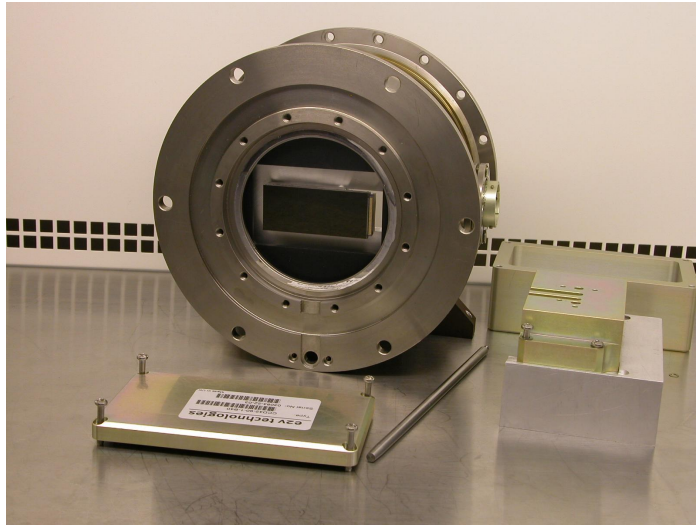
Прикладные процессы	
Инициализация и установка электрических режимов детектора	
Калибровка канала считывания	
Измерение спектральной плотности шума	
Телеметрия электрических режимов выходных узлов детектора	
Считывание в кадровом режиме	
Считывание в режиме дрейфового сканирования	



- Development of embedded software for digital signal processors
- Development of multitasking real-time kernels for multi-processor systems
- Application of object-oriented modelling language UML for effective development of complex software systems



- Production of multi-layer PCB prototypes
- Surface mounting of electronic components on PCBs (including IC with BGA packages)
- Embedded software debugging by in-circuit emulators and digital storage oscilloscopes



- Assembling of CCD cameras in dust-free conditions
- Testing of CCDs performance
- Research of non-documented physical properties of CCDs for optimization of signal processing quality

