Advanced Design Lab: CCD History

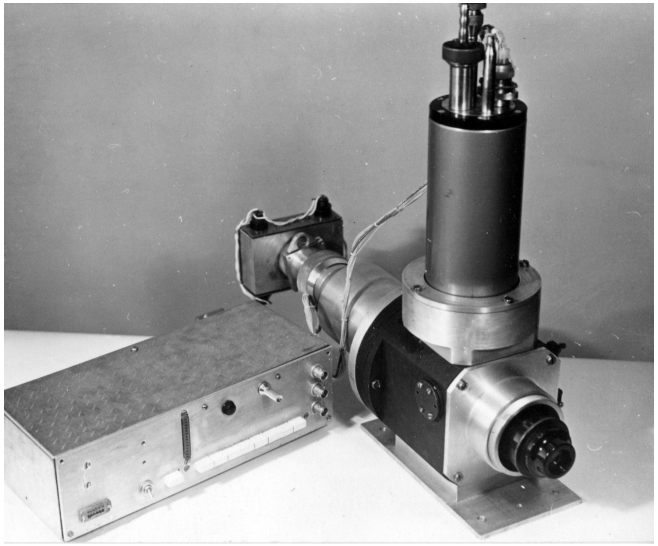
Special Astrophysical Observatory, 2005

Activities in 1980-2005

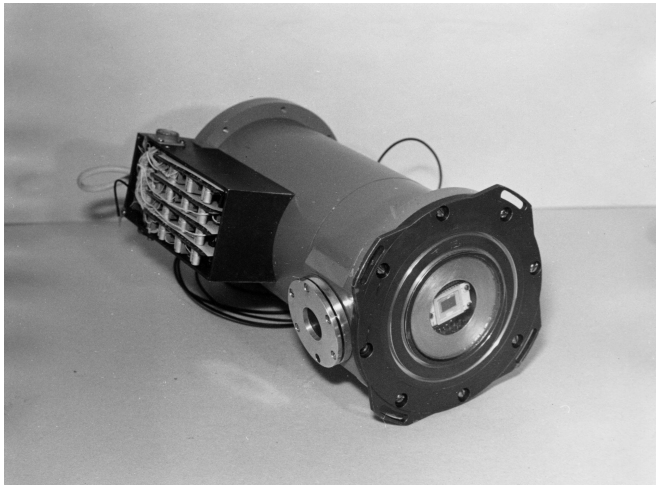
SAO

- Development of four generations of CCD Controllers
- Development of LN2 Cameras for various observation purposes
- Production of about 30 CCD Systems for 6-m telescope and other observatories
- Research and development of methods of CCD readout noise minimizing and photometric precision maximizing
- Investigation and testing of numerous SITe, E2V, Lick, TI, Atmel and others CCDs
- Climatic testing of CCD systems

1980s: First CCDs



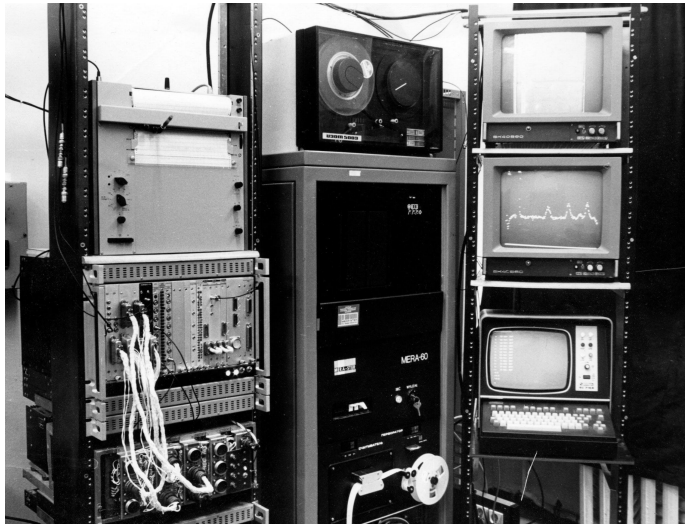
- **1981.** The first CCD Camera with 320 x 288 front illuminated surface channel CCD

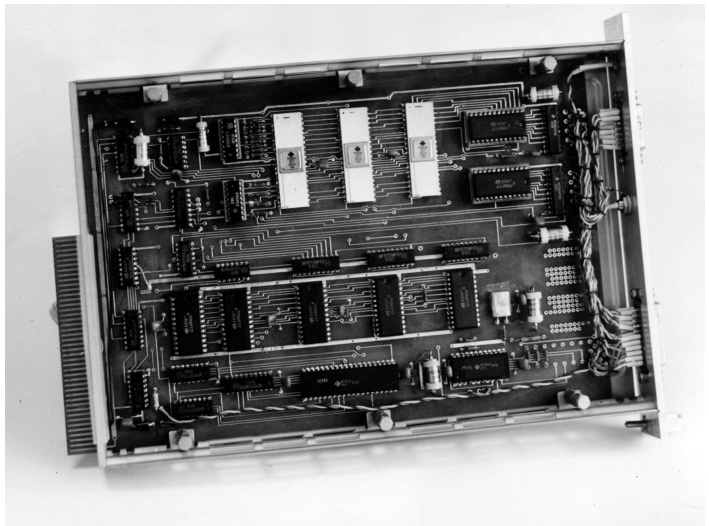


- **1984.** CCD Camera with 512 x 576 front illuminated surface channel CCD

1980s: First CCDs

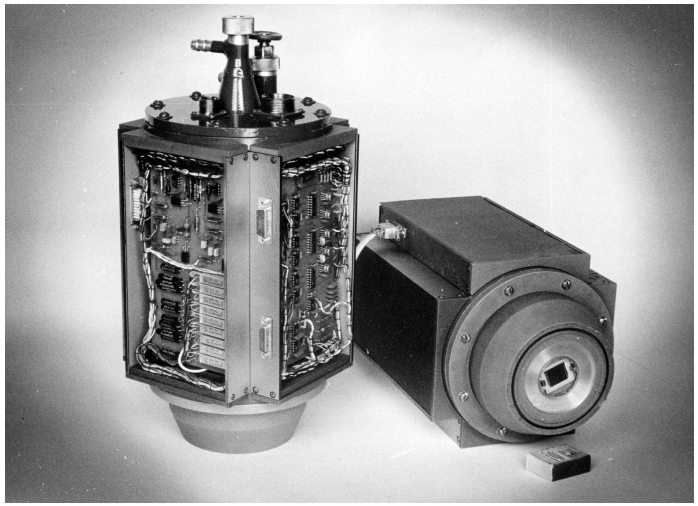
SAO



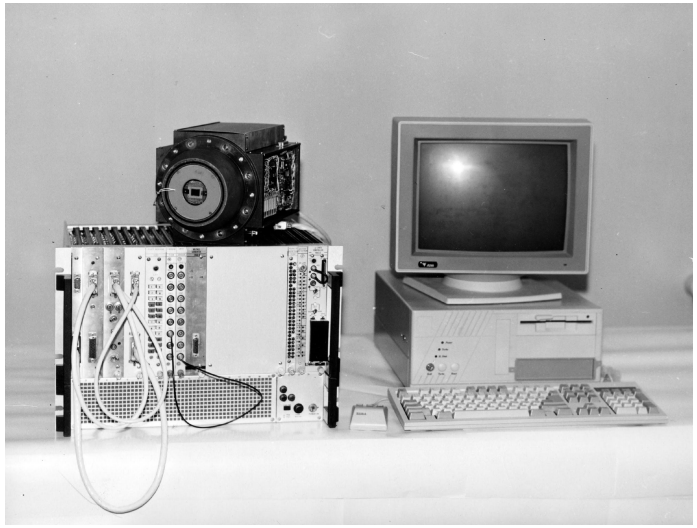


- **1984.** Generation I CCD Controller with control computer
- **1985.** First application of bit-slice processor in Generation II CCD Controller

1980s: First CCDs



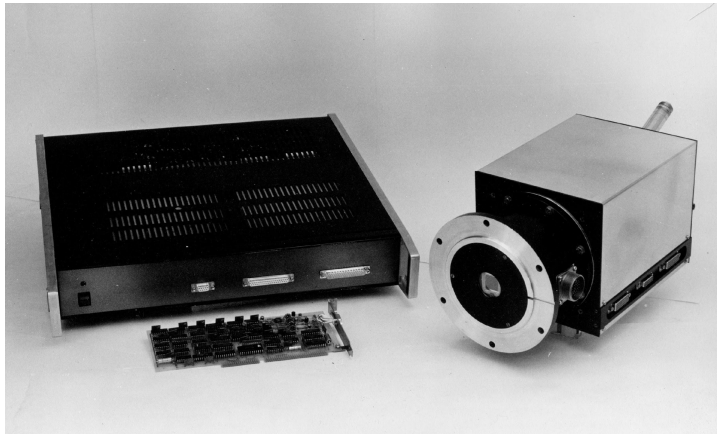
- **1985.** LN2 CCD Camera with 520 x 580 front illuminated CCD with buried channel



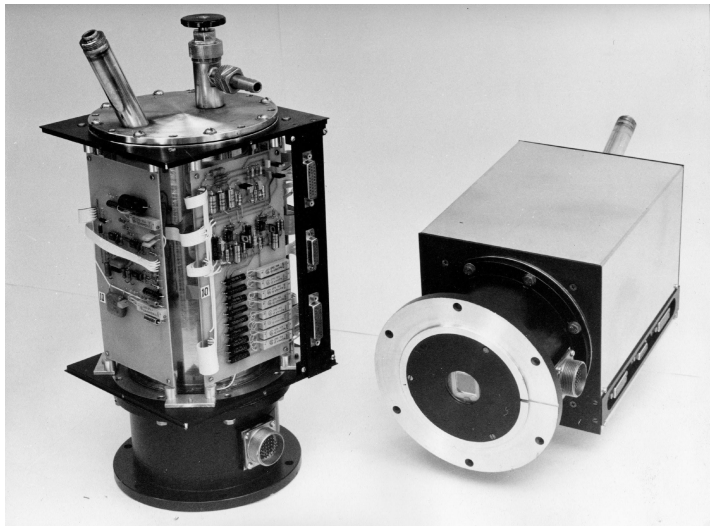
- **1985.** Generation II CCD Controller based on bit-slice processor

1990s: Low noise CCDs

SAO



- **1994.** Generation III CCD Controller with embedded Intel 8080 microcomputer



- **1994.** LN2 CCD Cameras with 1K x 1K and 2K x 2K CCDs

2000s: Ultra low noise CCDs

SAO

- **2000.** DINACON - New Generation DSP based CCD Controller for ultra low noise and high precision imaging

- **2000.** LN2 Dewars for up to 4K x 4K CCDs

DINACON: New imaging concept

SAO

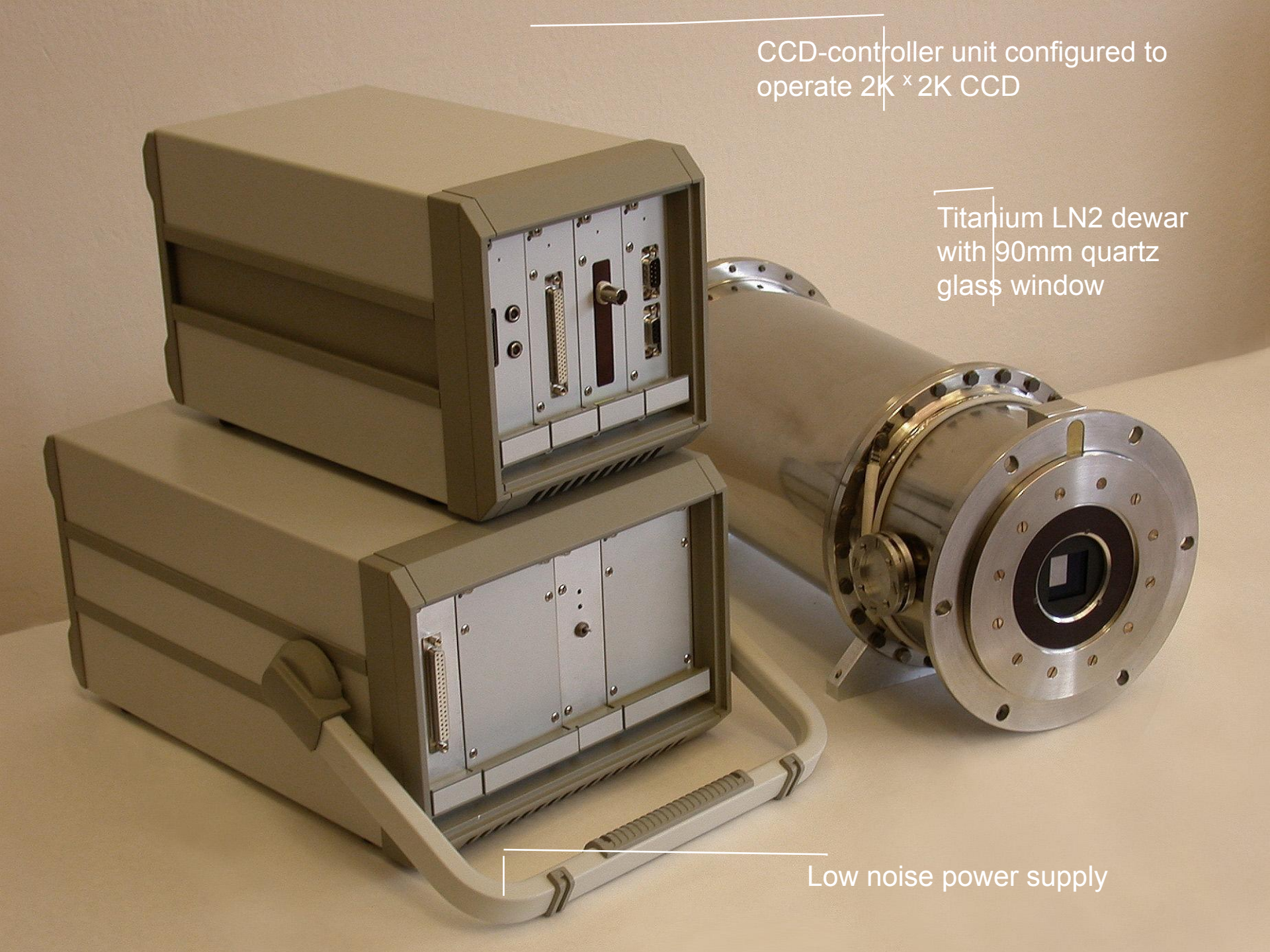
Novelty

- Optimal filtering of video signal
- Digital correction of bias and gain instabilities and non-linearity
- Flexible multiprocessor architecture with multitasking RTOS

Advantages

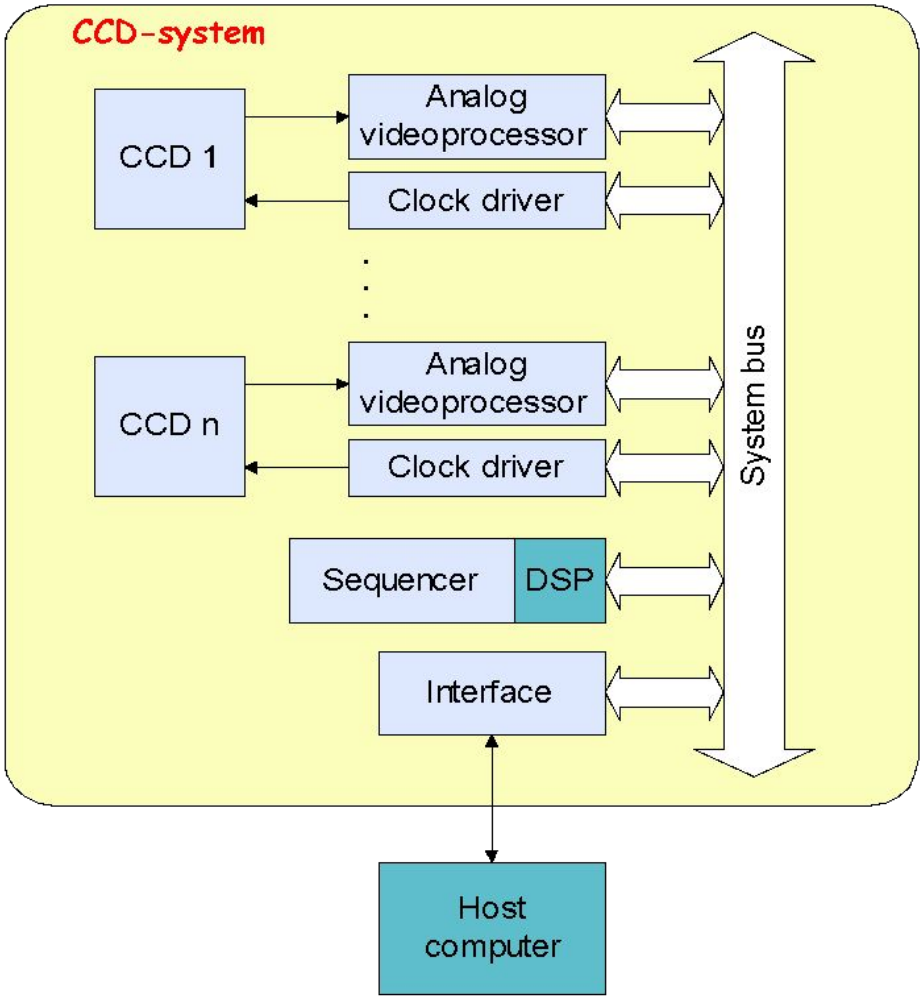
- Minimum readout noise
- Very high stability and linearity of CCD System transfer characteristic
- High dynamical range
- Easy to control the complex mosaic and infrared detectors

Generation IV CCD controller DINACON: DSP based Intelligent Array Controller


CCD-controller unit configured to operate 2K x 2K CCD
Titanium LN2 dewar with 90mm quartz glass window
Low noise power supply

Typical single processor CCD-system

SAO



Advantages

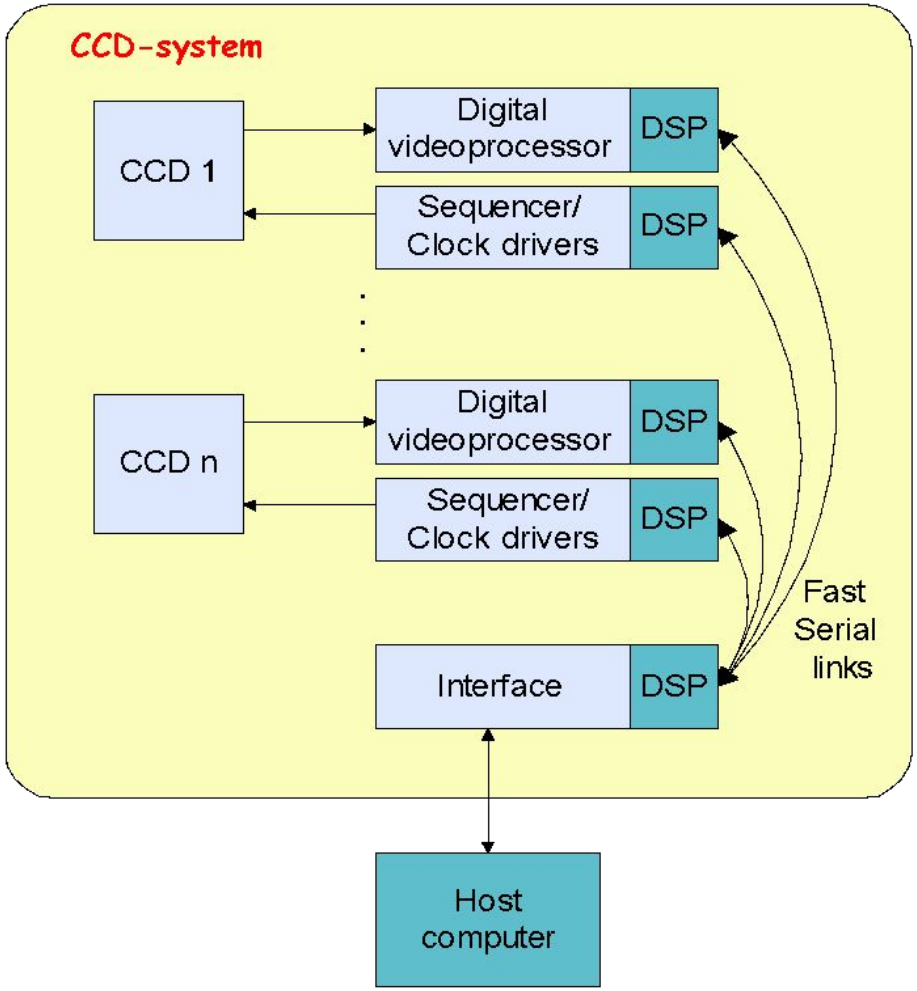
- relative simplicity
- multichannel operations

Limitations

- incomplete noise filtering
- noisy system bus
- limited number of channels (n<16)
- low level of flexibility and intelligent functions

SAO's DSP-based CCD-system

SAO

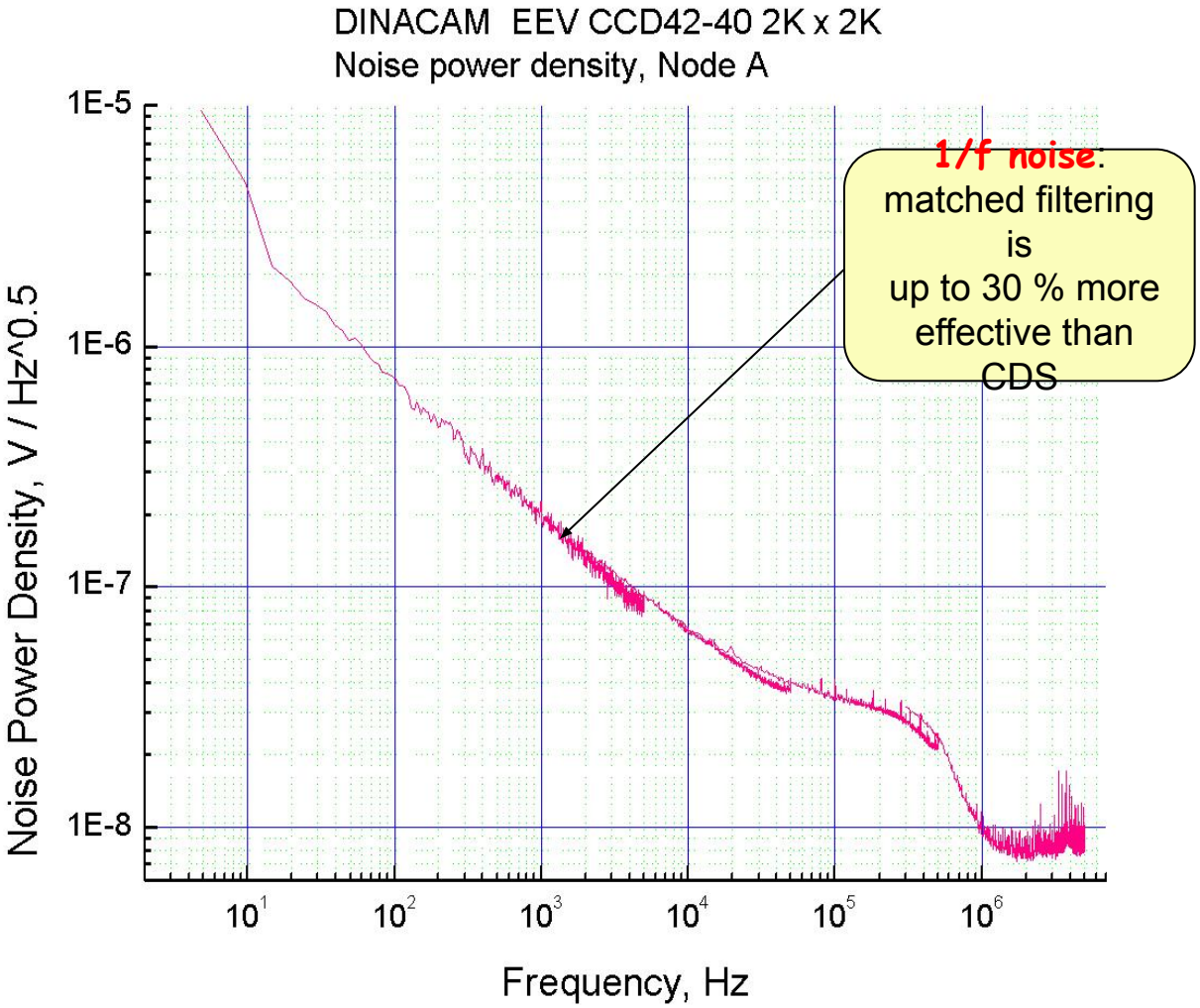


Advantages

- ultralow noise through matched filtering
- no noisy system bus
- higher precision and accuracy
- flexible star- or- tree-type topology
- number of channels up to 32
- high level of intelligent functions

Why need matched filtering?

SAO



DINACON: Photometric results

SAO

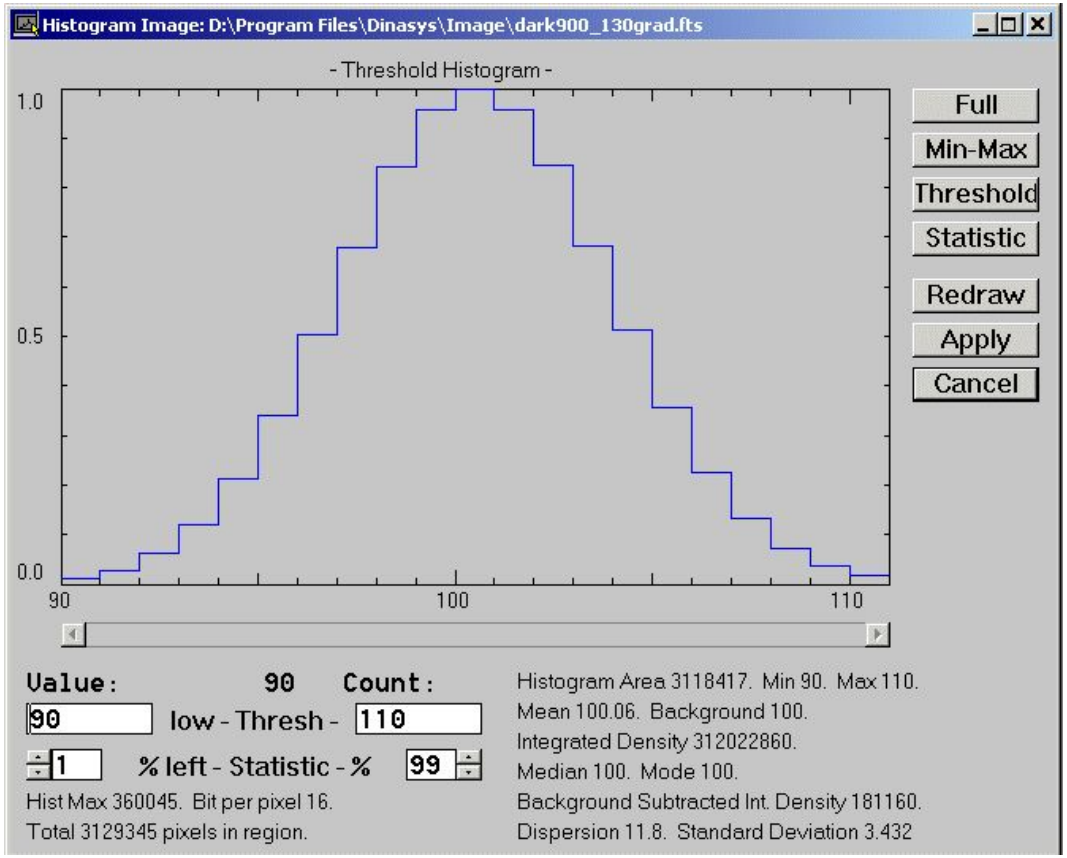
- Readout noise reduction: 2.5 e → 1.7 e
- Photometric instability: 0.03% / 24 h
- Nonlinearity reduction: 1.00% → 0.03%

Literature:

- Buffington et al., 1990:
  Instability = 0,3 % , Δt = 10 h, at room temperature
- Robinson et al., 1995:
  Instability = 0,5 %, Δt = 10 days, at stabilized temperature

DINACON: CCD 42-40 noise

SAO

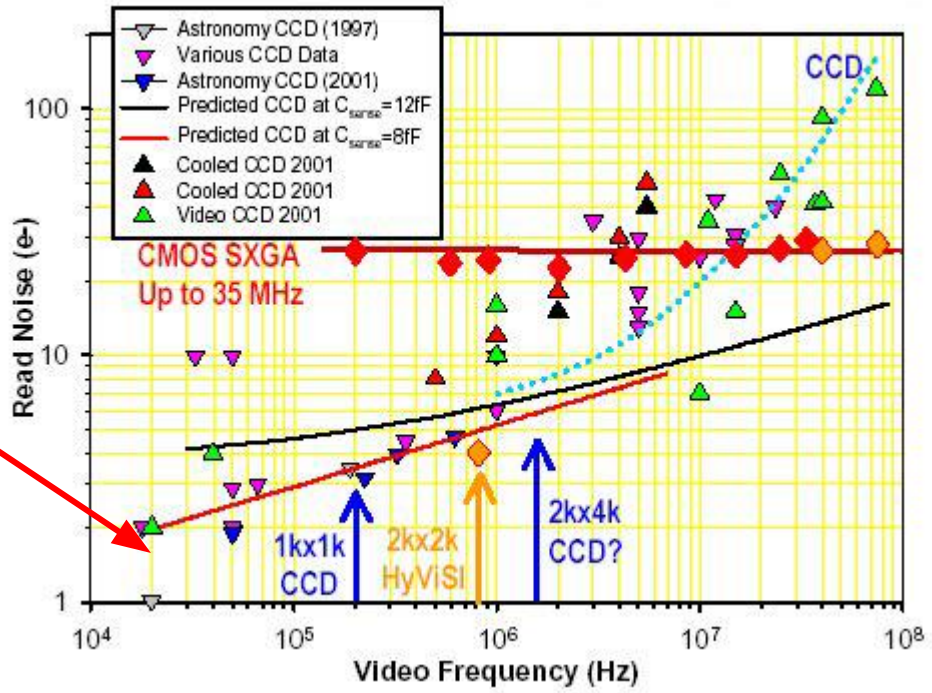


- ADU = 0.5 e
- Readout rate = 18 kHz
- Noise = 1.7 e

DINACON: The best noise

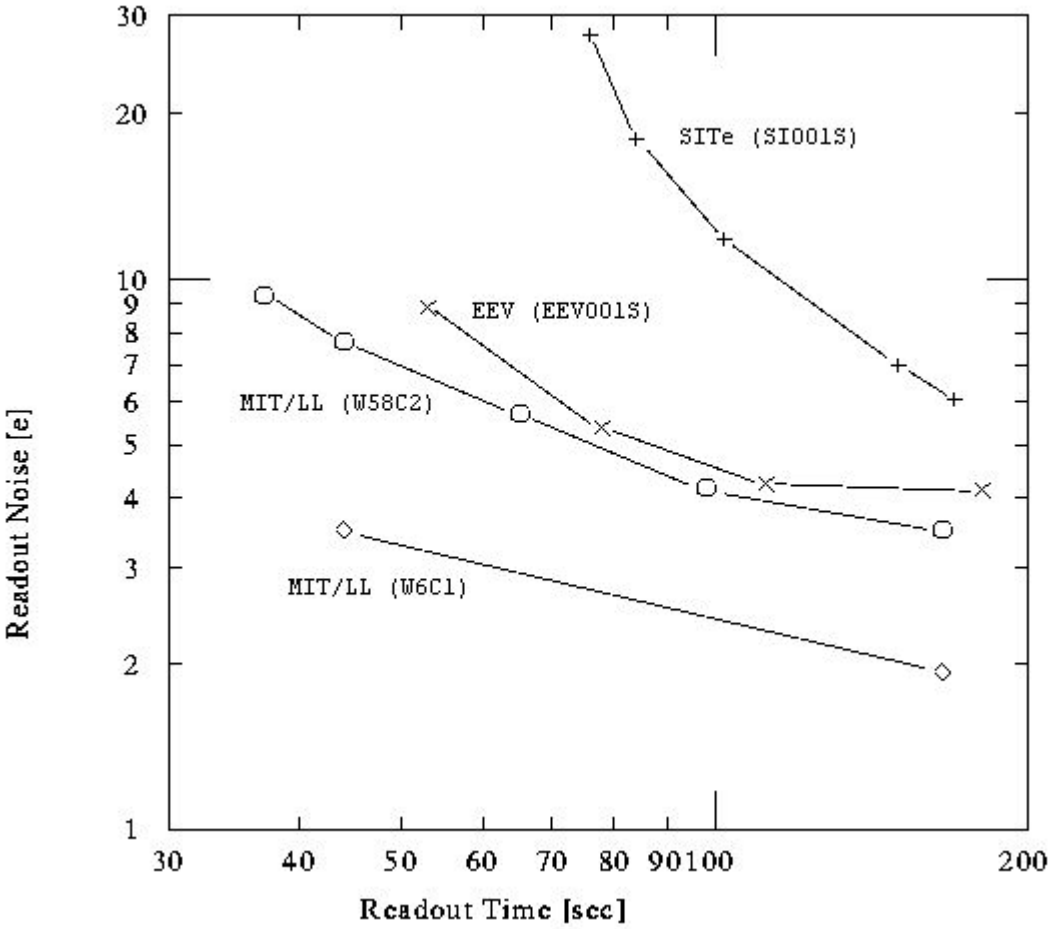
SAO

SAO's
CCD 42-40



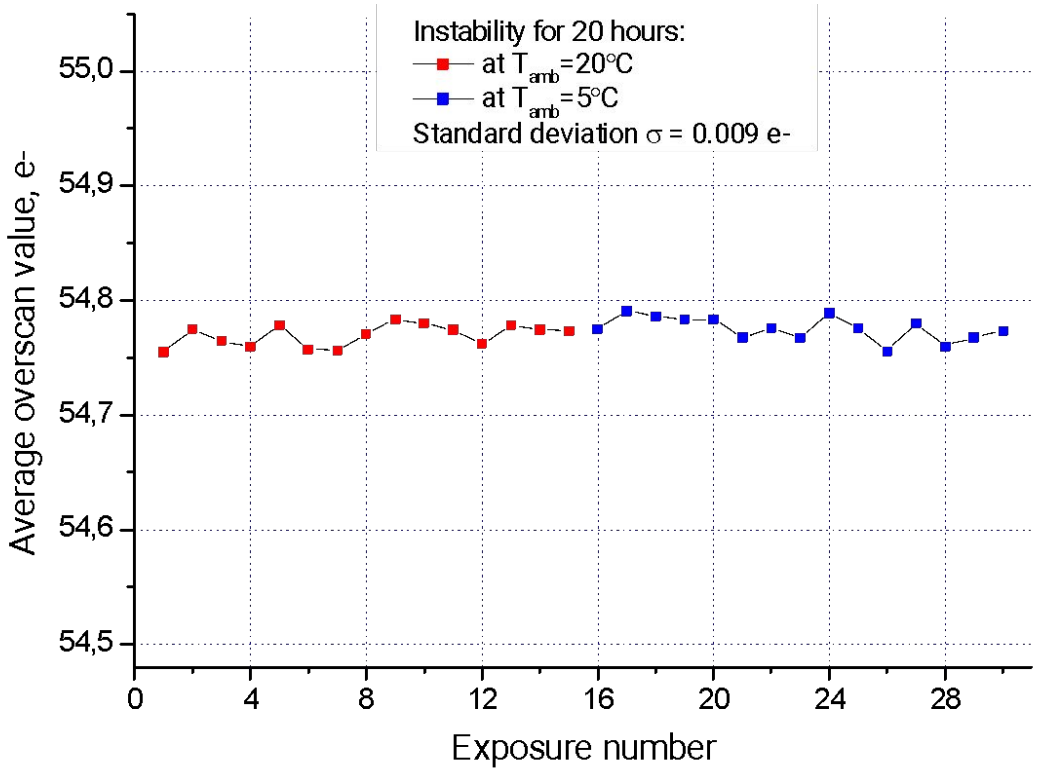
Scientific CCDs Noise

SAO



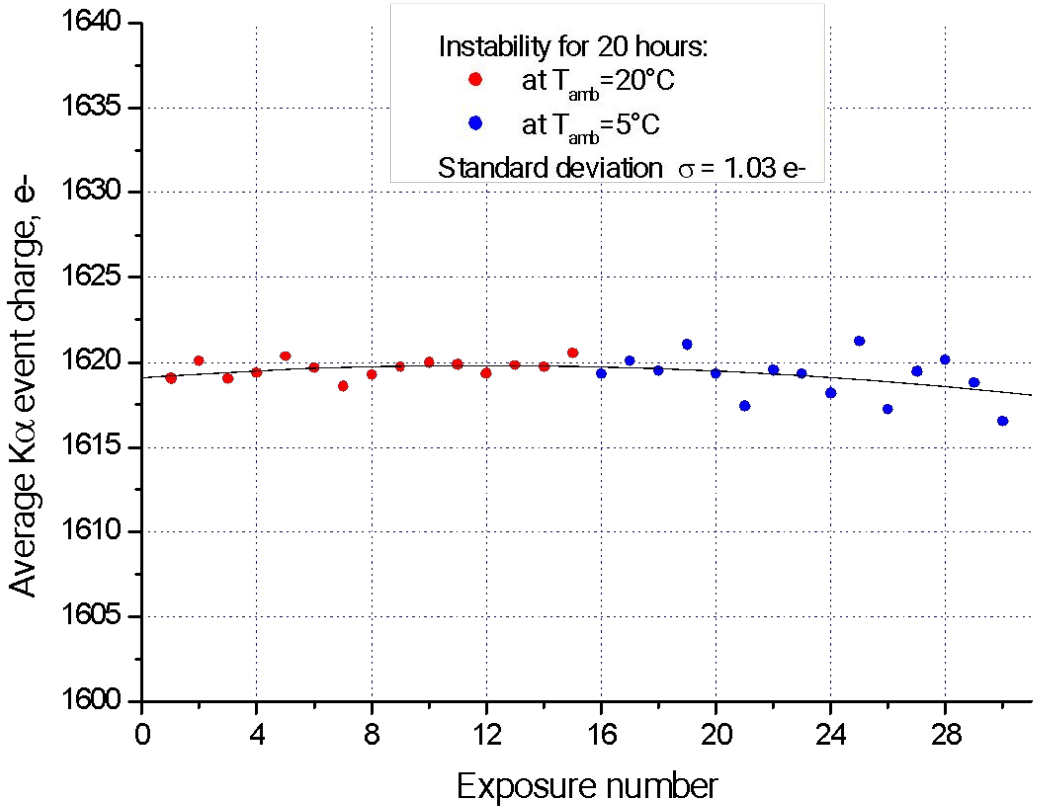
DINACON: Overscan instability

SAO



DINACON: Gain instability

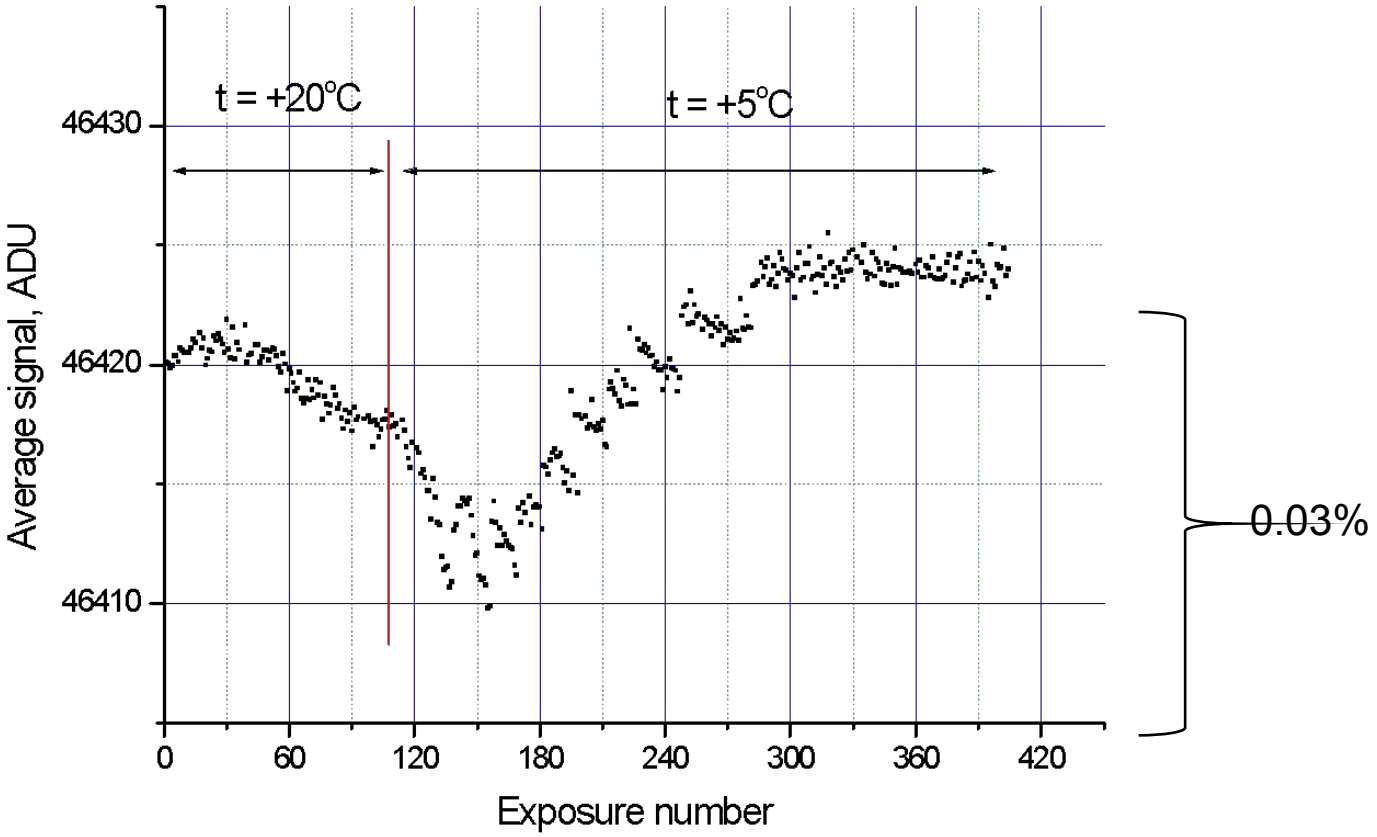
SAO



Gain instability at 1620 electrons level measured by means of Fe55

DINACON: Gain instability

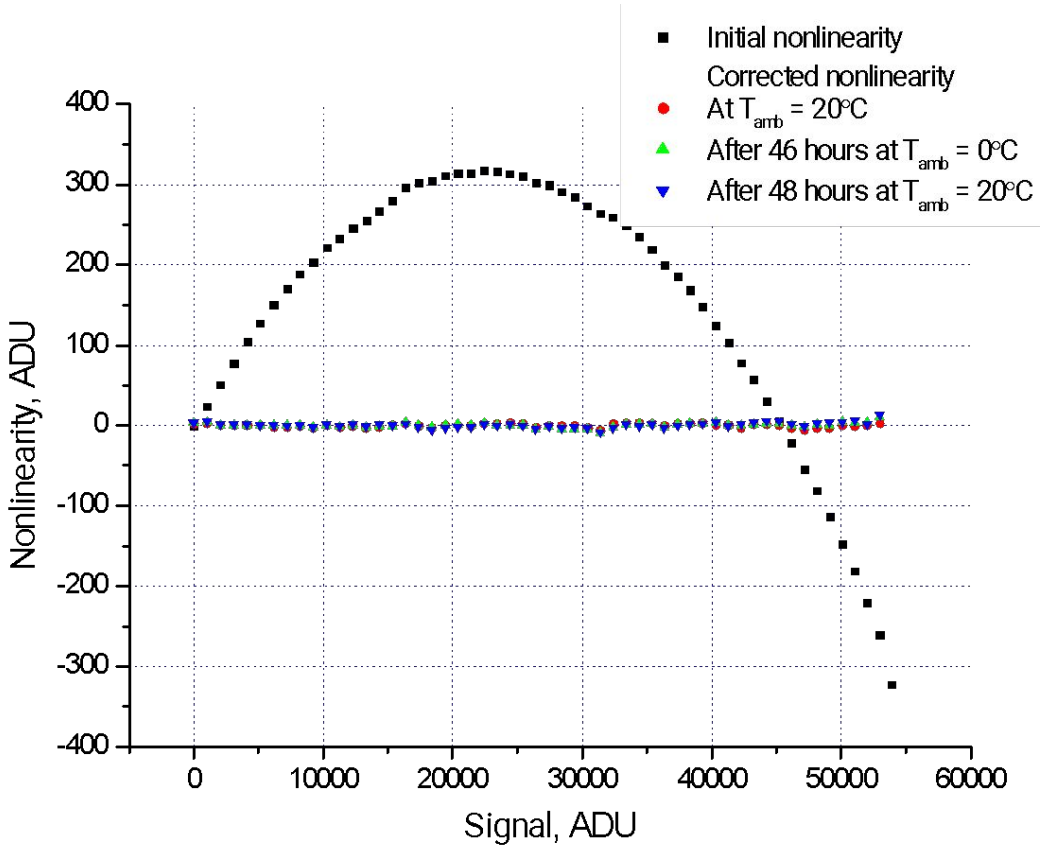
SAO



Gain instability measured by means of stable light source

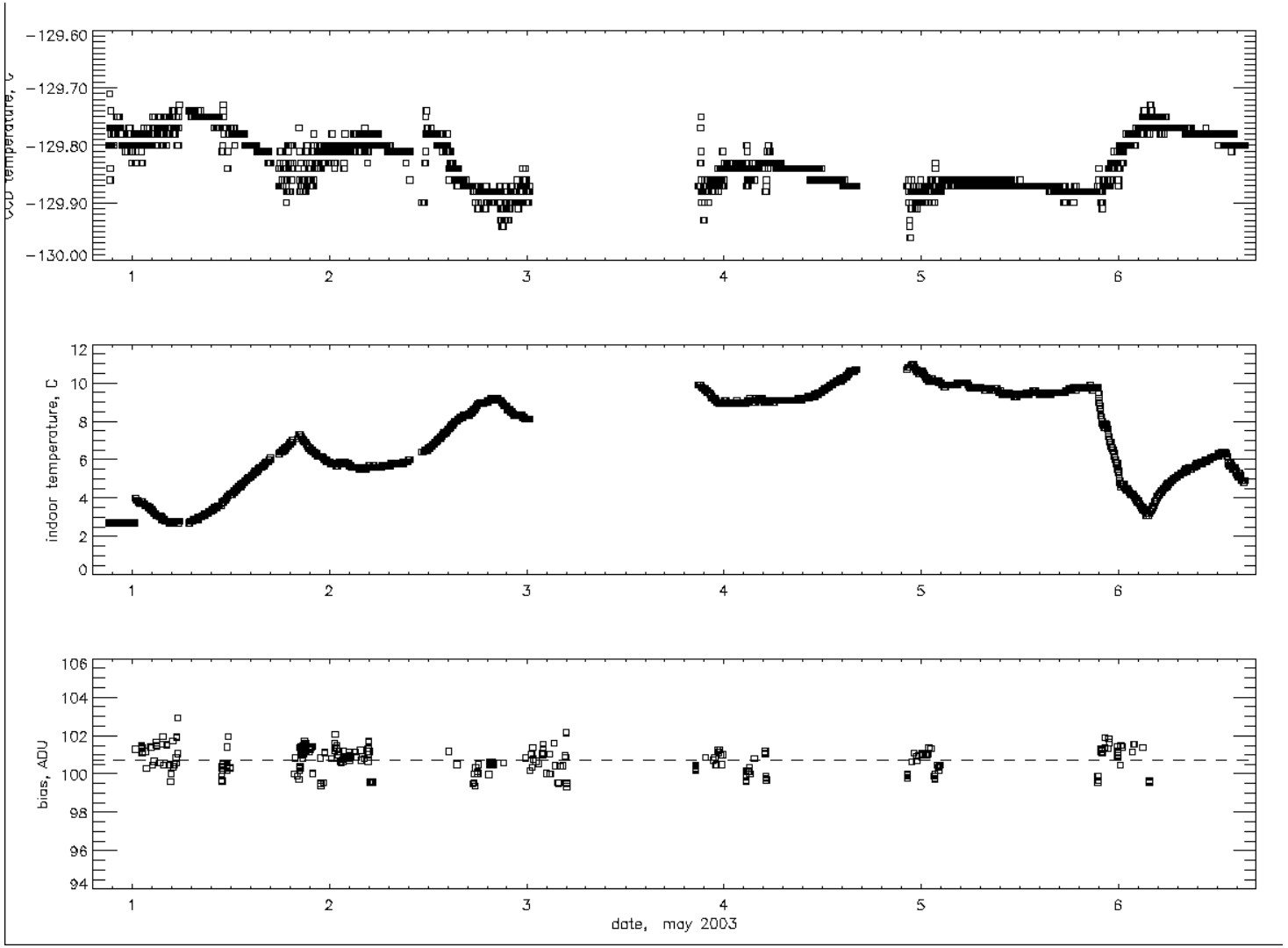
DINACON: Nonlinearity correction

SAO



DINACON: Instabilities on telescope

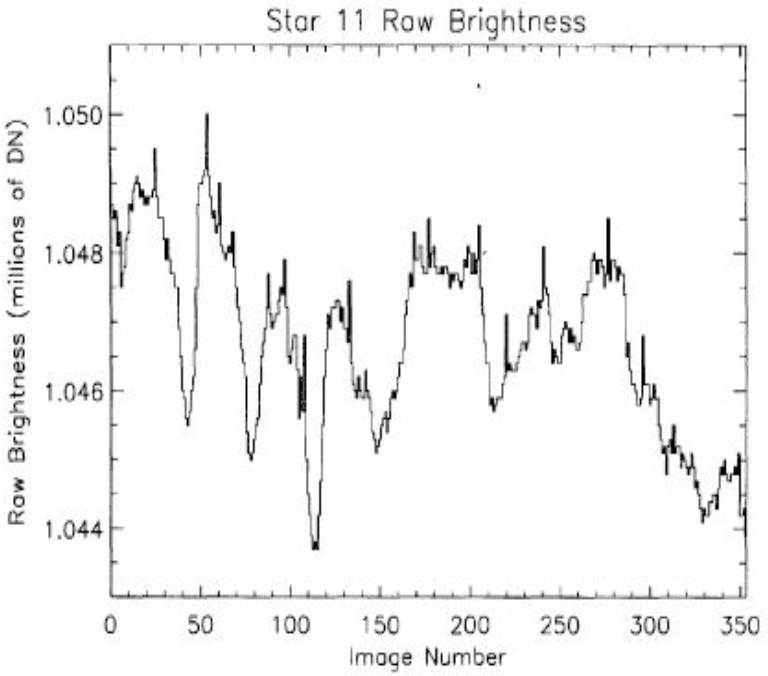
SAO

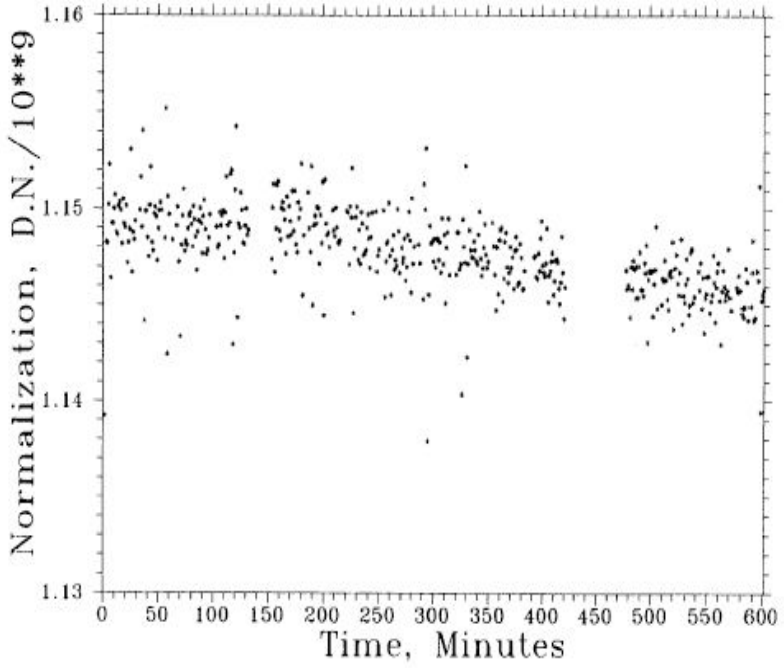


Gain instability: the best results

Robinson et al,1995: 0.6% p-p
Conditions: room temperature

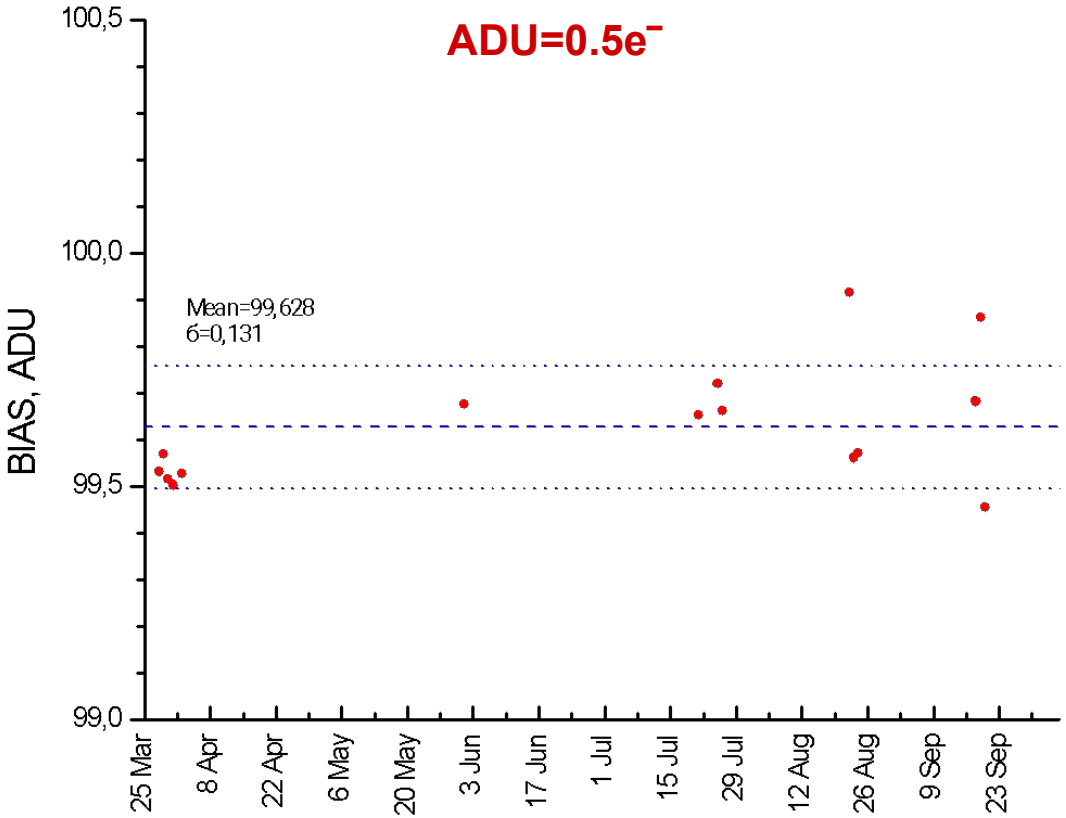
Buffington et al, 1990: 0.8% p-p
Conditions: stabilized temperature





DINACON: Long-term bias instability

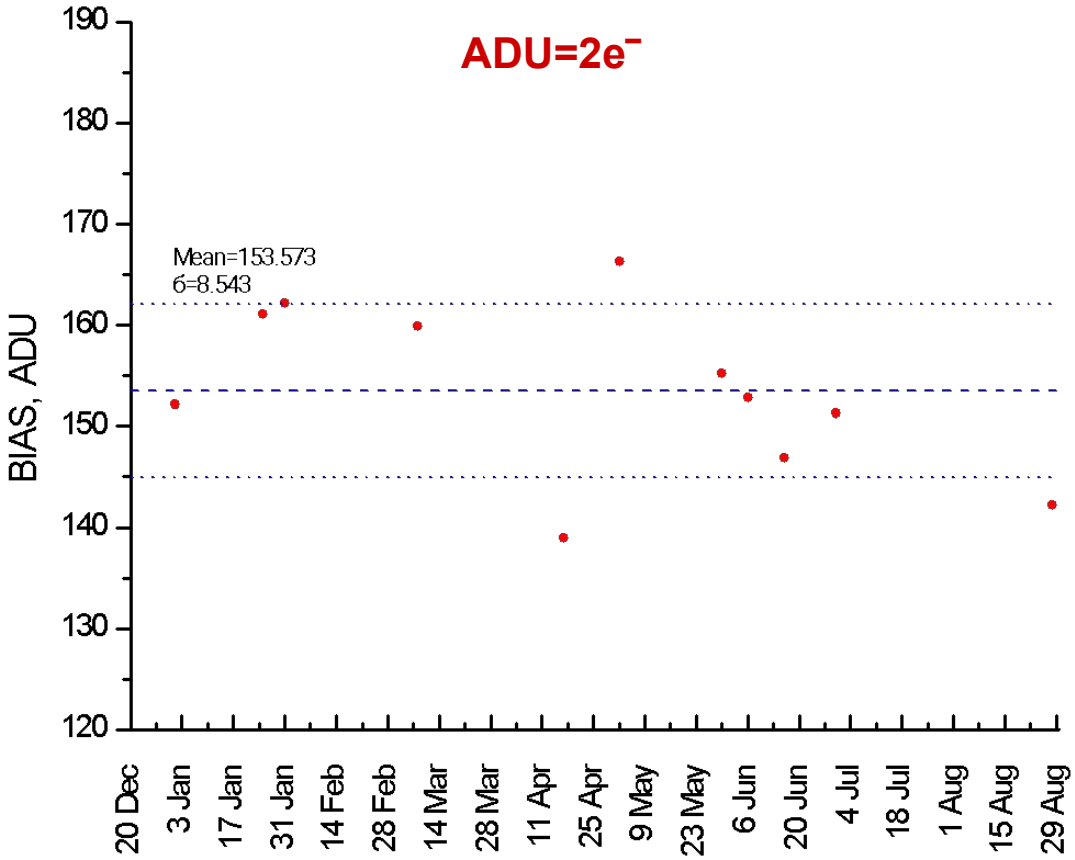
SAO



Instability during 6 monthes is about 1 electron p-p

ESO's FIERA: Long-term bias instability

SAO



Instability during 8 monthes is about 60 electrons p-p

CCD Controllers Comparison

SAO

	SDSU-II (SDSU)	FIERA (ESO)	Arcon (NOAO)	DINACON I (SAO)
Architecture				
Embedded computer	no	yes	no	no
Processor type	DSP56002, 24 bit, 40 ns/instr.	TMS320C40, 32 bit, 20 ns/instr.	TRAM , 16/32 bit, 50 ns/instr.	ADSP2160, 32 bit, 25 ns/instr.
Multiprocessing	no	2 processors	yes	yes
Topology	-	linear	star	star or tree
Interprocessor connections	-	common bus	4 port/processor, 20 bit/s/port	5 port/processor, 160 Mbit/s/port
External communications	SCSI 12 MB/s, fiber 5 MB/s	fiber 128 MB/s	fiber 4 MB/s	fiber 10 MB/s, Ethernet 1 MB/s
Embedded memory	32 KB	-	-	8 MB
Signal processing				
Type of signal processing	analog	analog	analog	**digital**
Number of ports (videochannels)	1 – 32	2-32	4-16	2 - 64
Dynamical range, bit	16	16 (21)	16	18 - 20
Max. pixel rate, Mpixel/s/port	1.0	2.0 (5.5)	0.4	2.5
Internal noise (at 1 Mpixel/s), e-	-	1.3	-	**< 1**
Buffer memory, MB/port	external	-	0.064	8
Transfer characteristic correction	no	no	no	**yes**
Detector control				
Max. number of channels	16	16	4	32
Time resolution, ns	40	20	40	25
Amplitude resolution, bit	12	16	-	12
Control clocks per channel	24	-	28	48
Bias voltages per channel	8	-	16	20

CCD Controllers Comparison

SAO

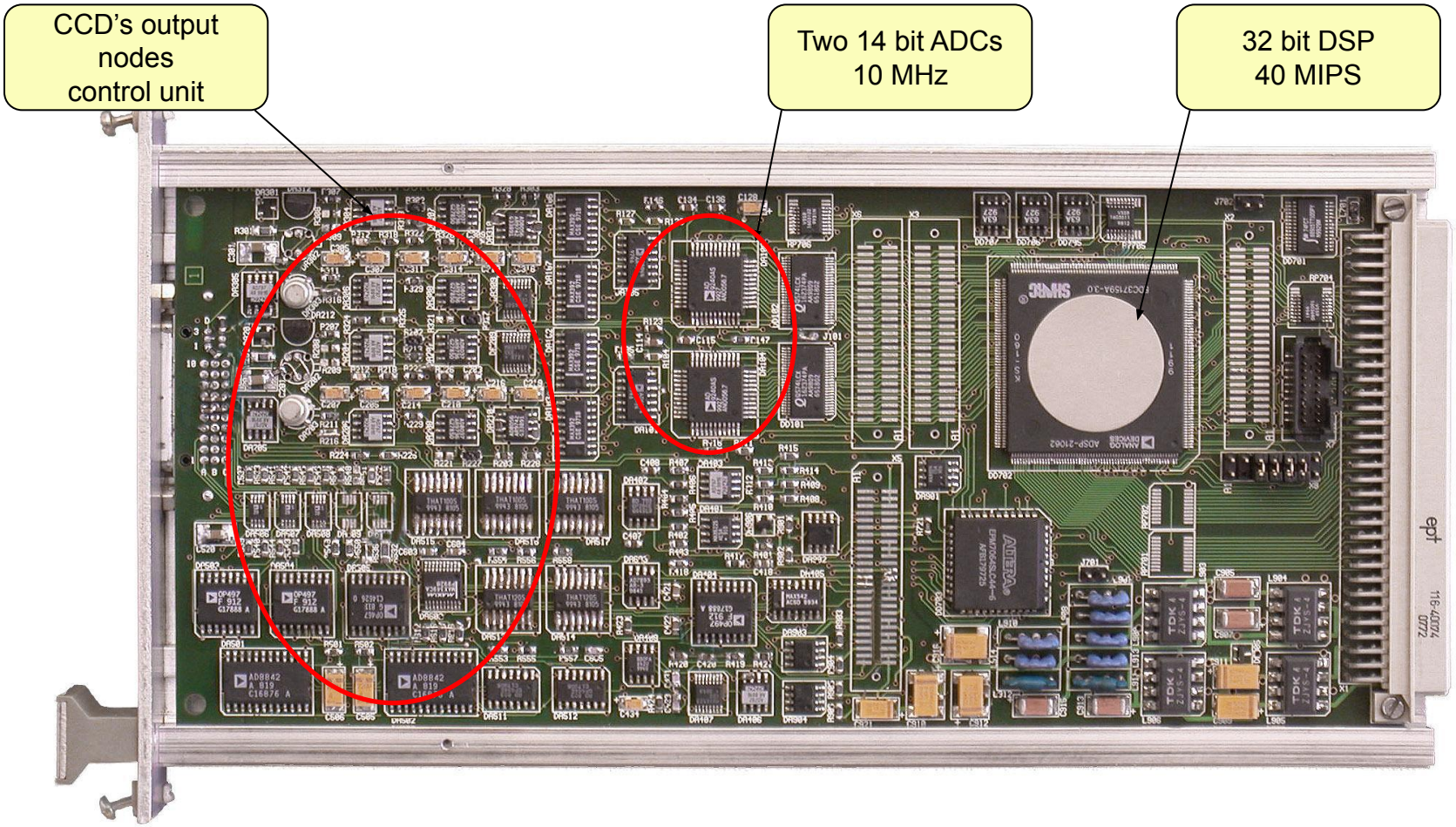
Property	SDSU-II (SDSU)	FIERA (ESO)	Arcon (NOAO)	DINACON (SAO)
Controller architecture				
Modularity	+	+	+	+
Expandability	+	+	-	+
Detector control				
Program setting of clock parameters	+	+	+	+
Clock telemetry	-	+	-	+
Program setting of output stage mode	-	-	-	+
Telemetry of output stage mode	-	-	-	+
Program setting of CCD temperature	+	+	+	+
Telemetry of CCD temperature	+	+	+	+
Programming of optional storing and readout modes	-	-	-	+
Videoprocessing				
Multichannel processing	+	+	+	+
Digital matched noise filtering	-	-	-	+
Measuring of noise spectrum of output stage	-	-	-	+
Auto-calibration and correction of transfer function of video channel	-	-	-	+
Extended dynamic range of video-channel (> 16 бит)	-	+	-	+

DINACON I Module Structure

- System controller with communication adapter
- Sequencer with drivers
- Videoprocessor
- Peripheral controller

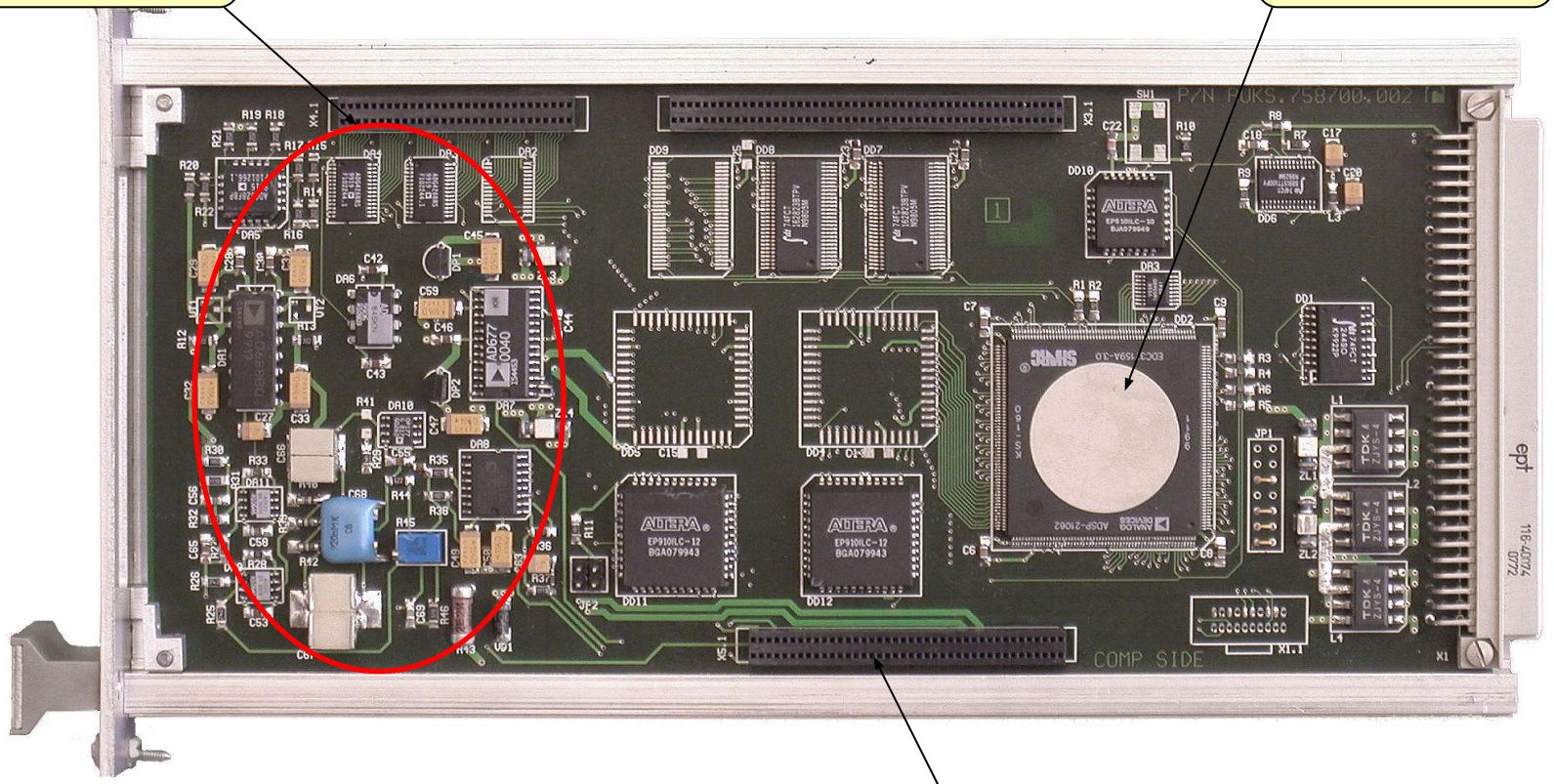
DINACON I: Videoprocessor

SAO



DINACON I: Sequencer

SAO

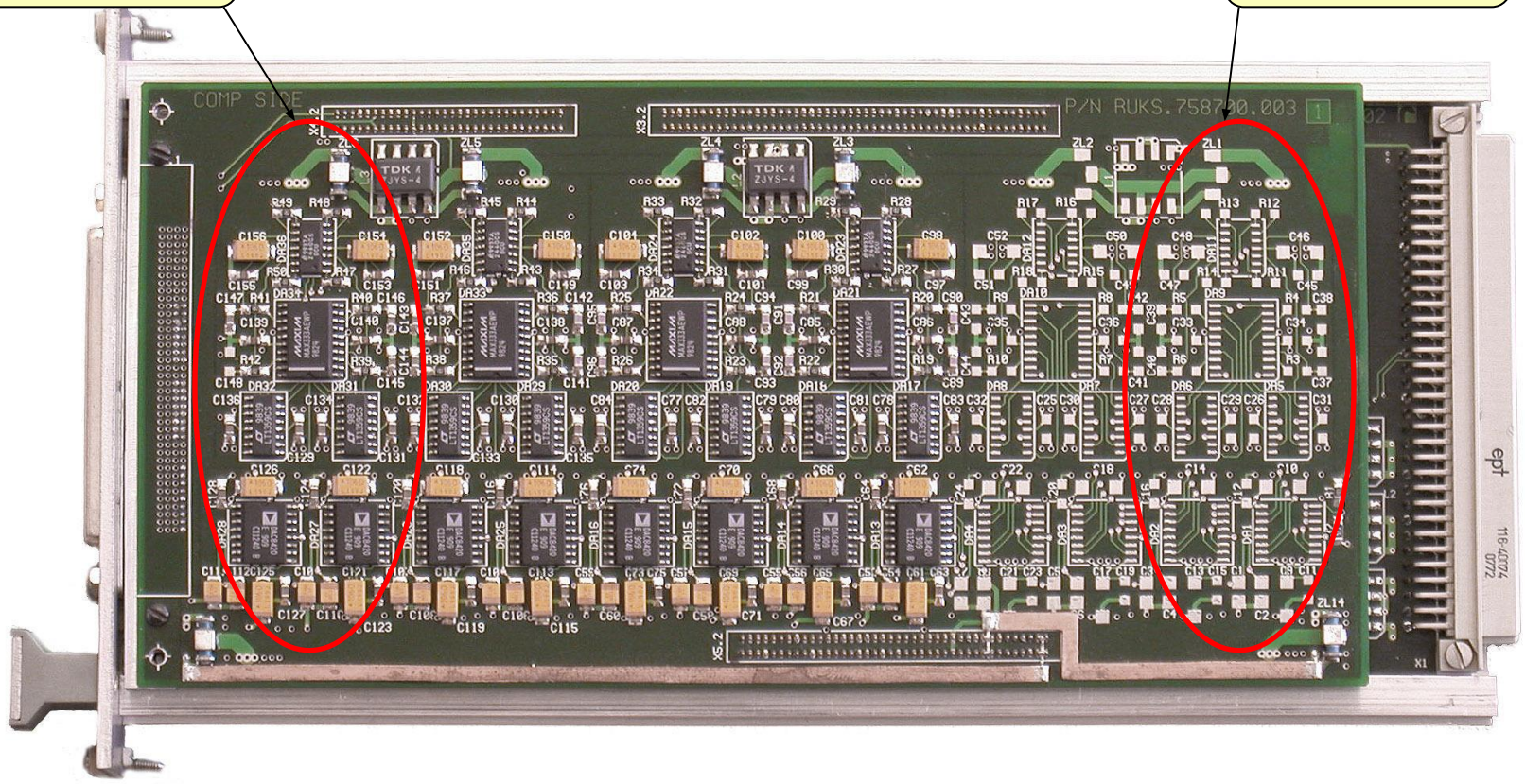


DINACON I: Clock drivers

SAO

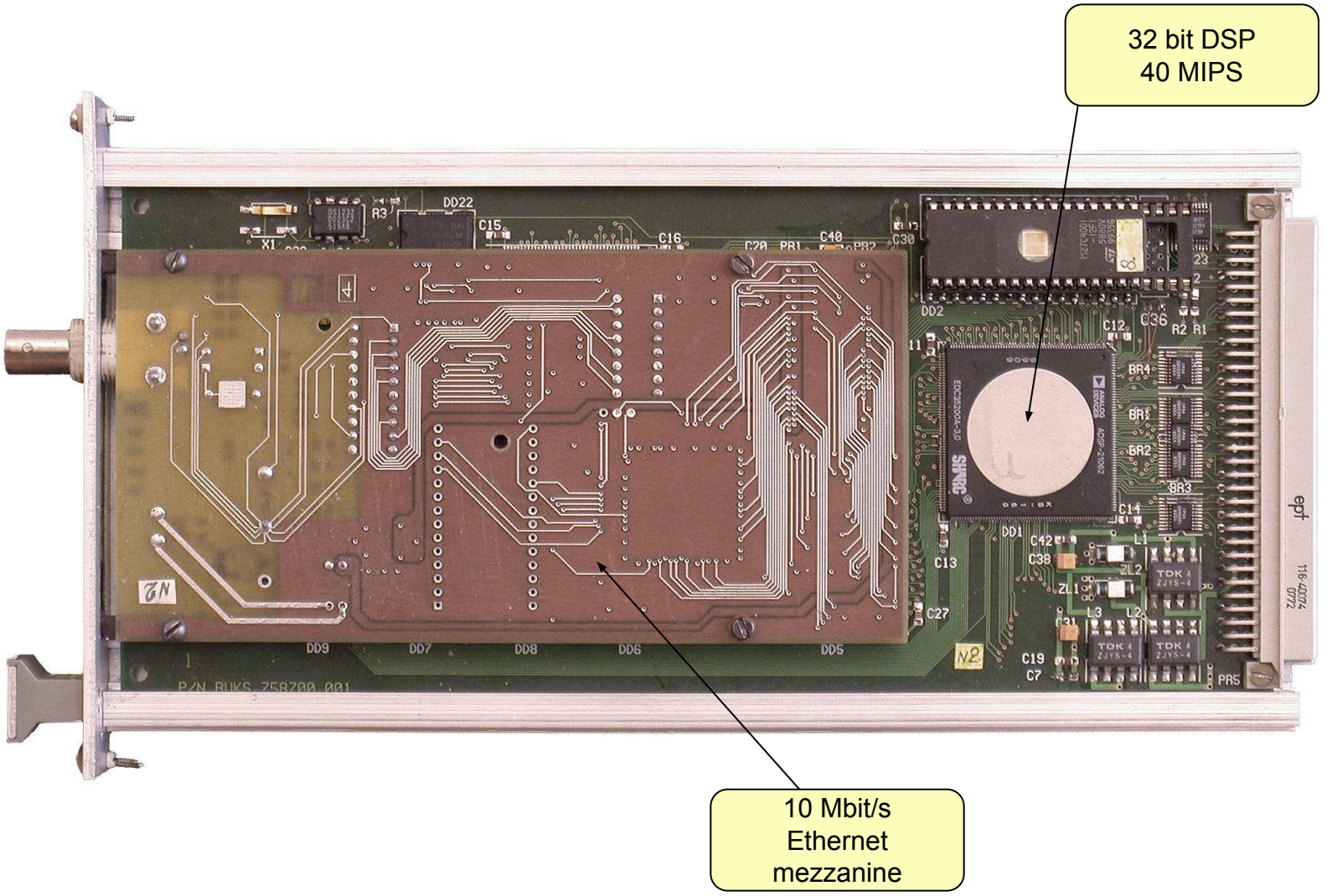
4 CCD clocks
unit # 1

4 CCD clocks
Unit #6



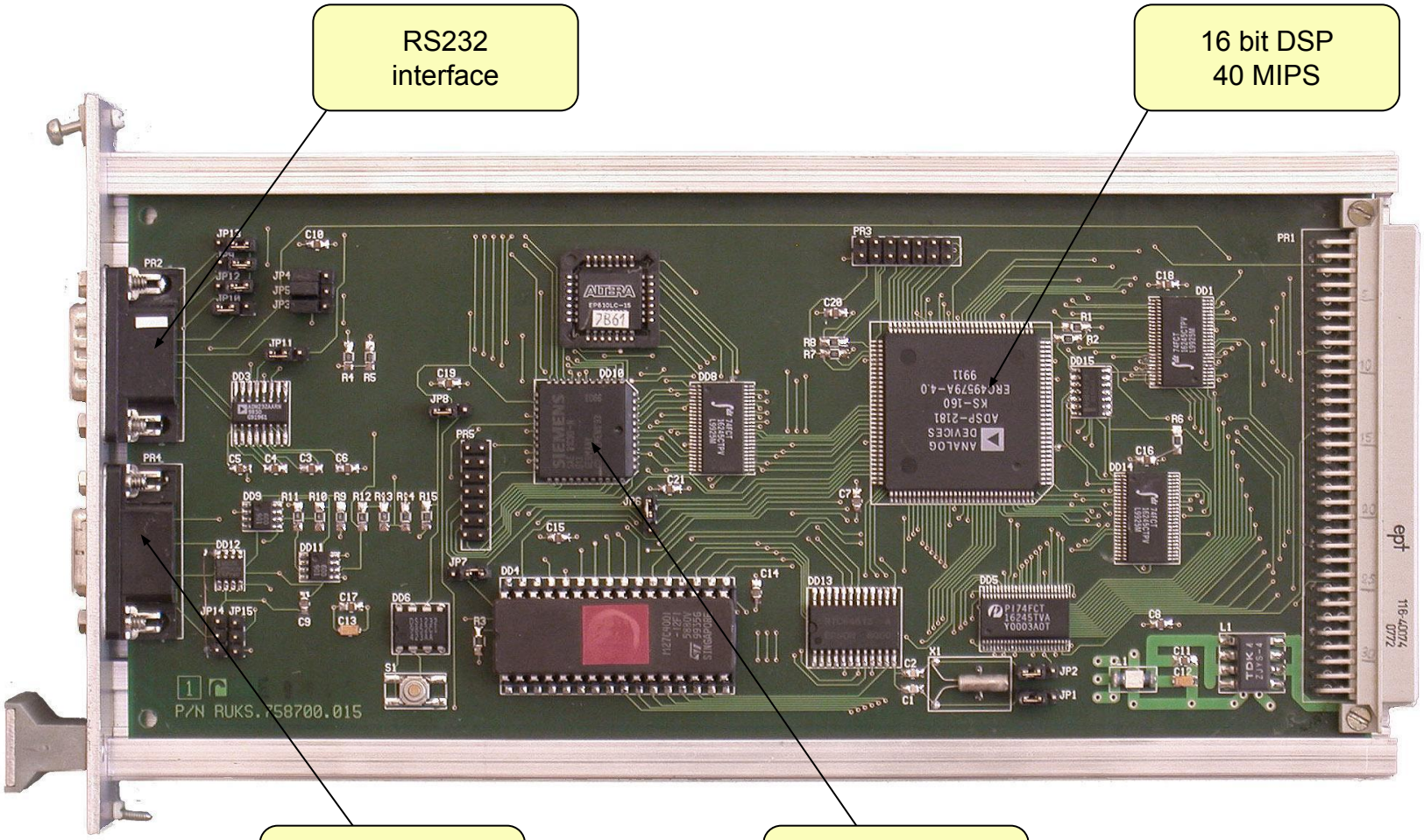
DINACON I: System controller

SAO



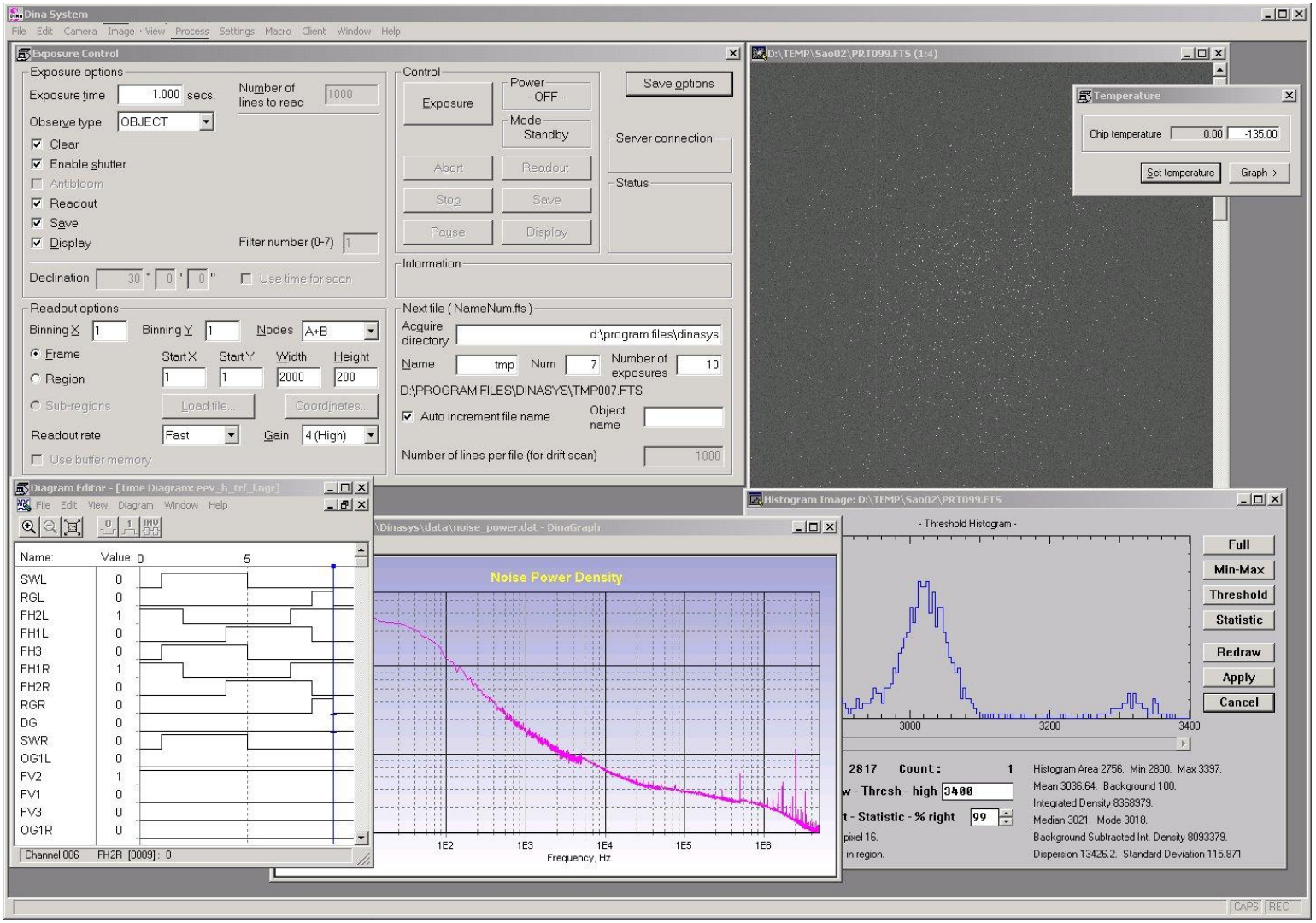
DINACON I: Periferal controller

SAO



DINASYS: Control Sofware

SAO

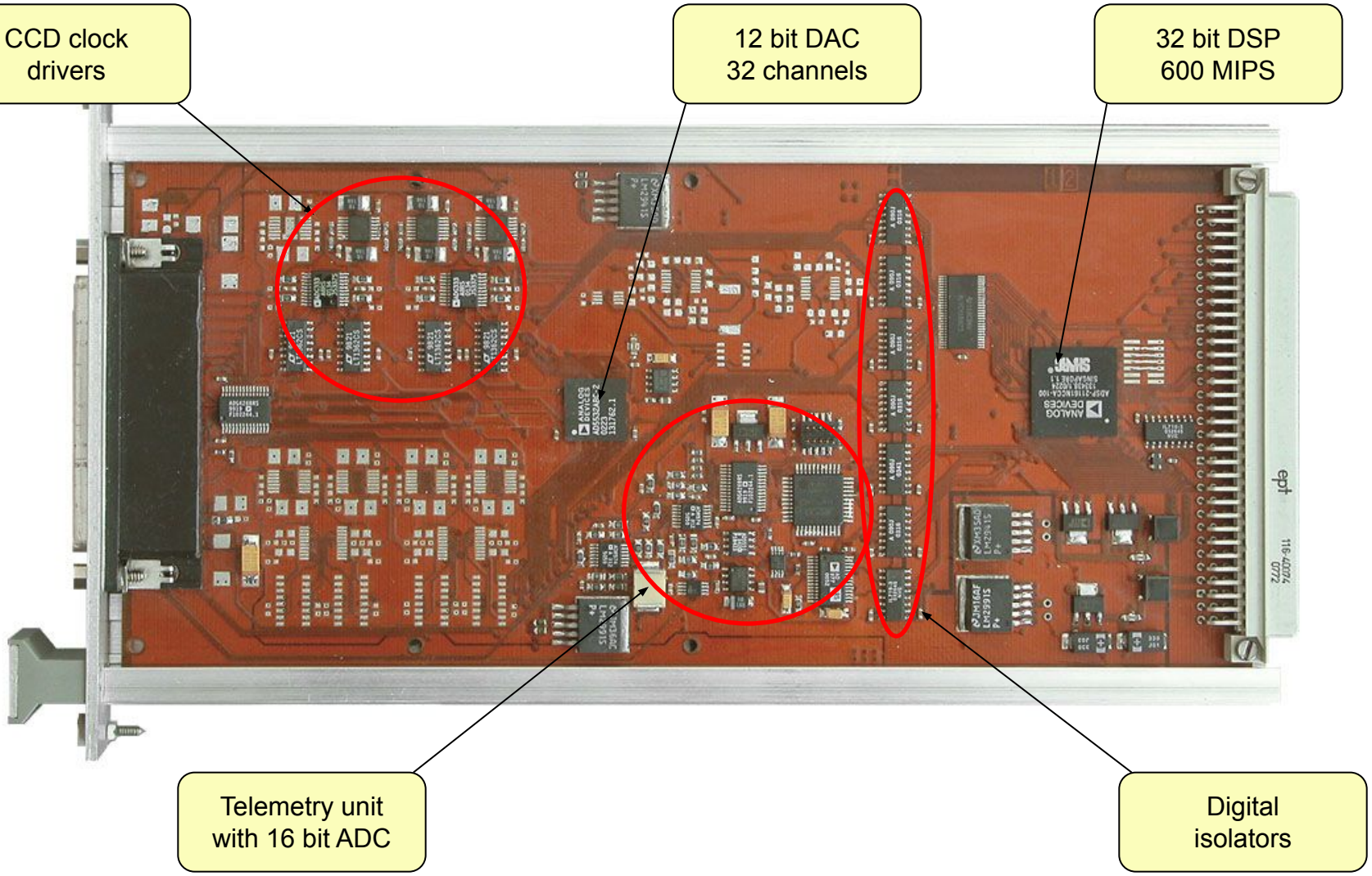


DINACON II Module Structure

- System controller with communication adapter
- Sequencer with drivers
- Videoprocessor

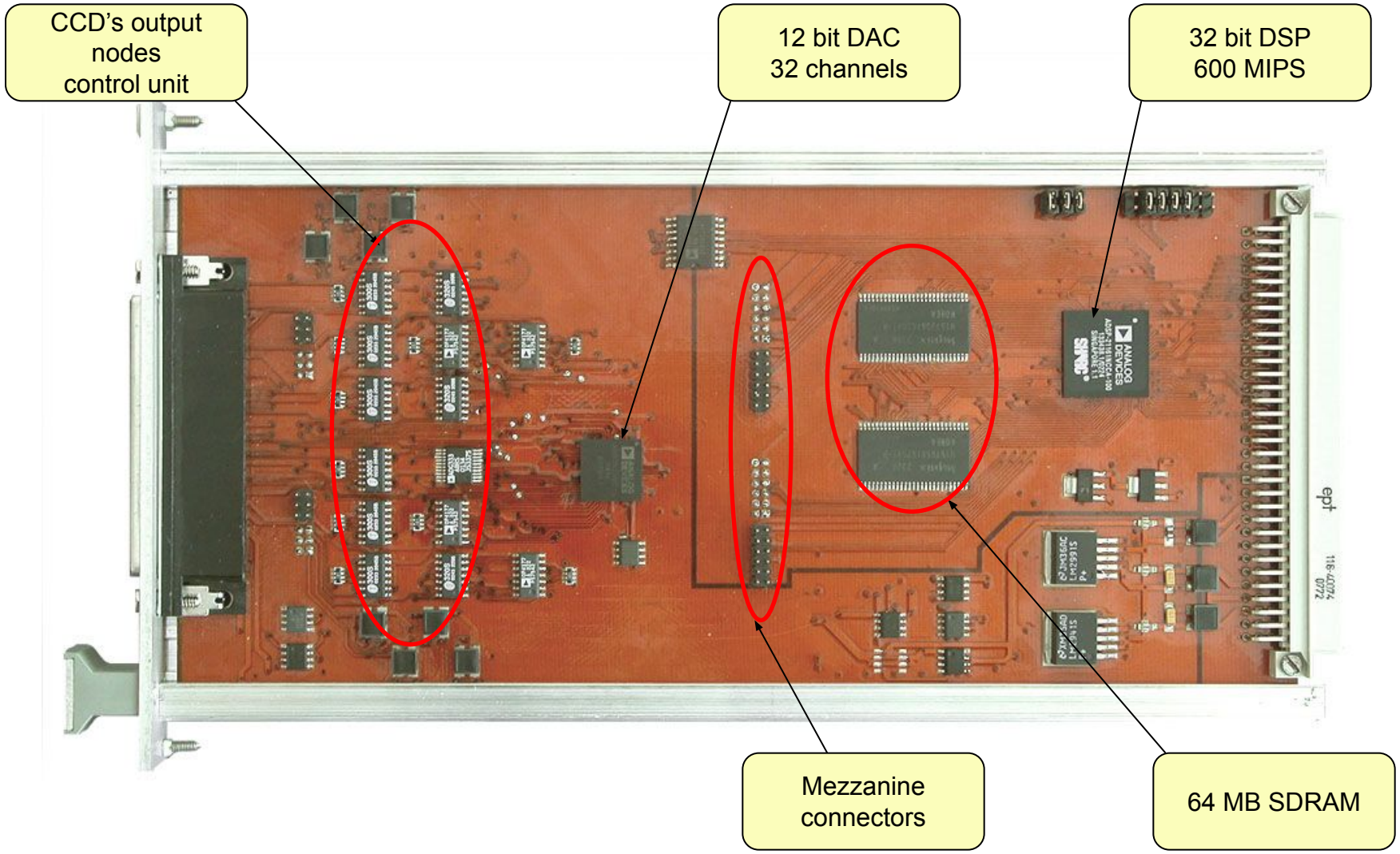
DINACON II: Sequencer

SAO



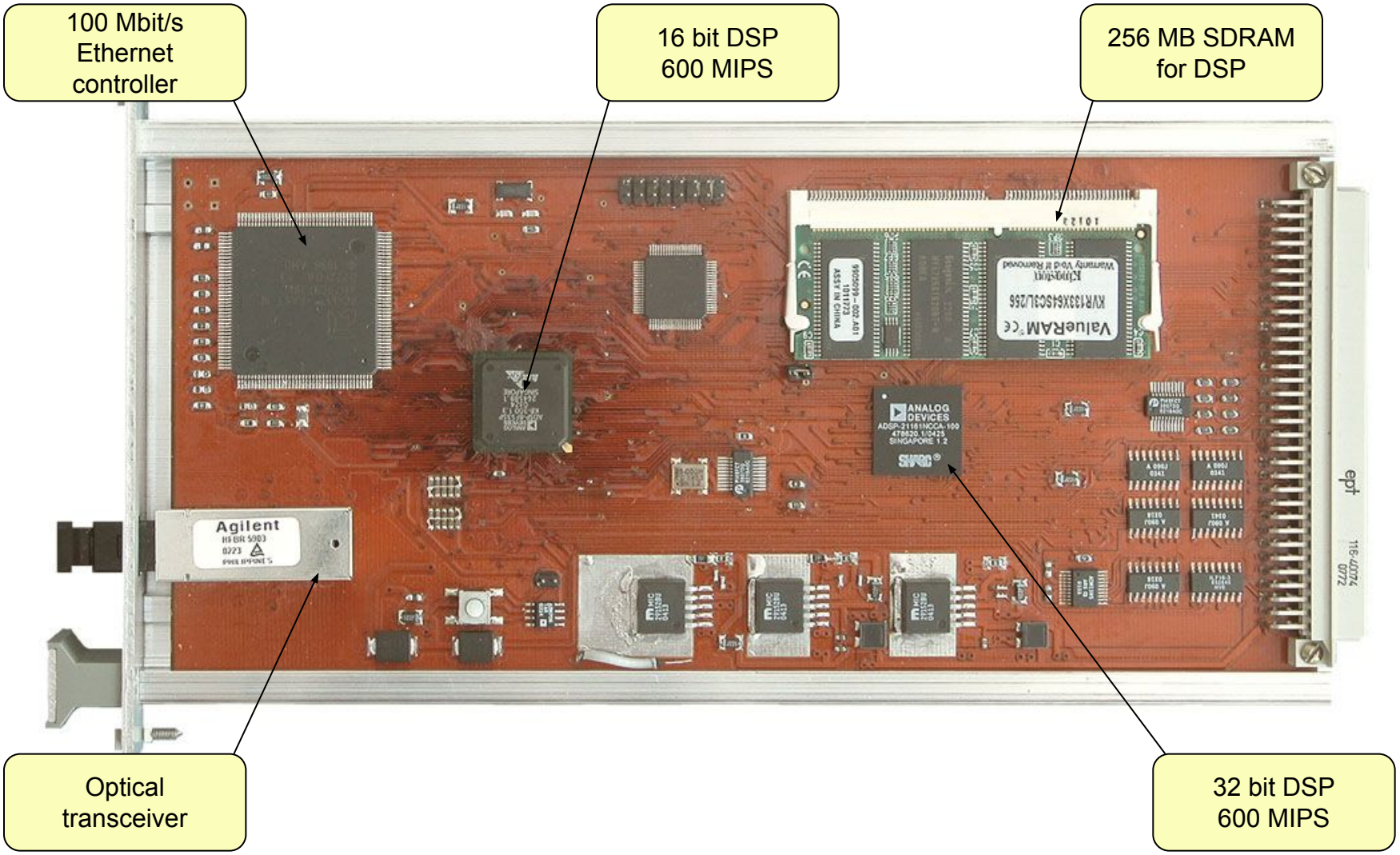
DINACON II: Videoprocessor

SAO

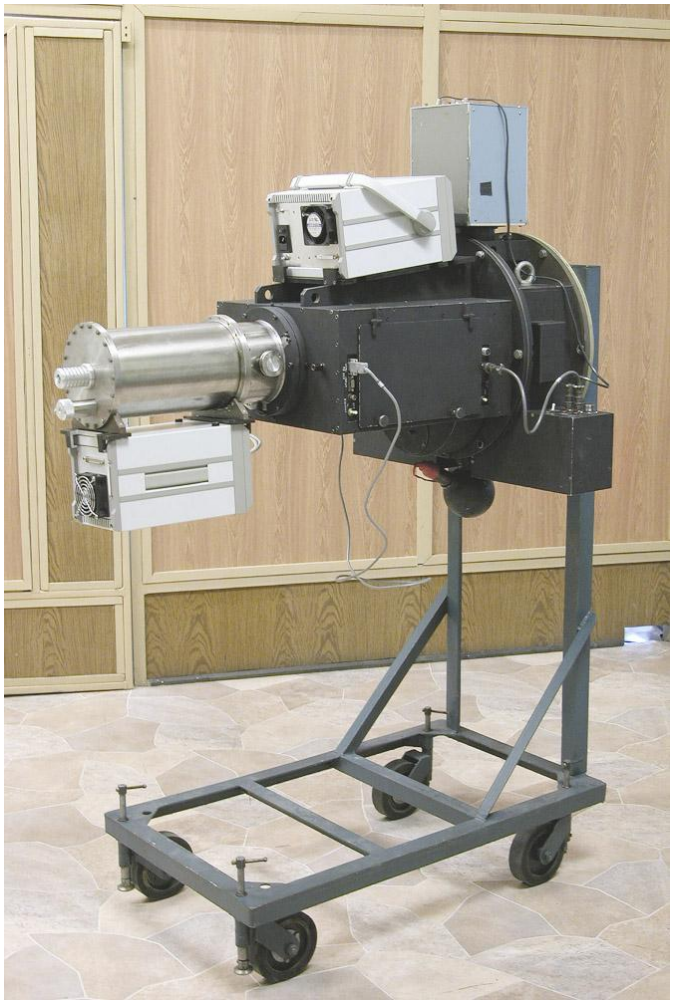


DINACON II: System controller

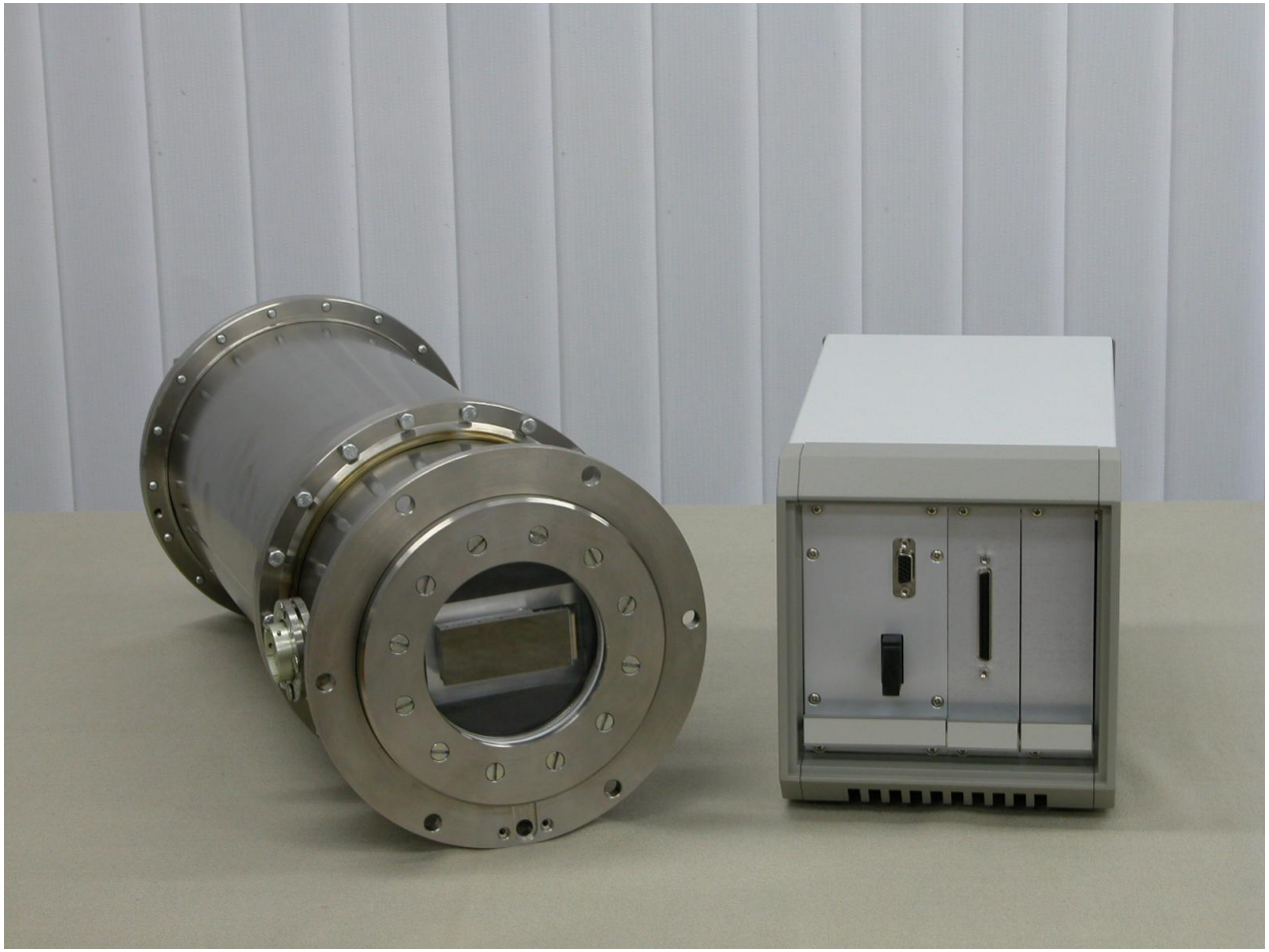
SAO



DINASYS 2K x 2K on multi-pupil fiber spectrograph MPFS



DINASYS 2K x 2k on multi-mode focal reducer SCORPIO



Camera 2K x 4.5k and controller (without power supply)

Our team

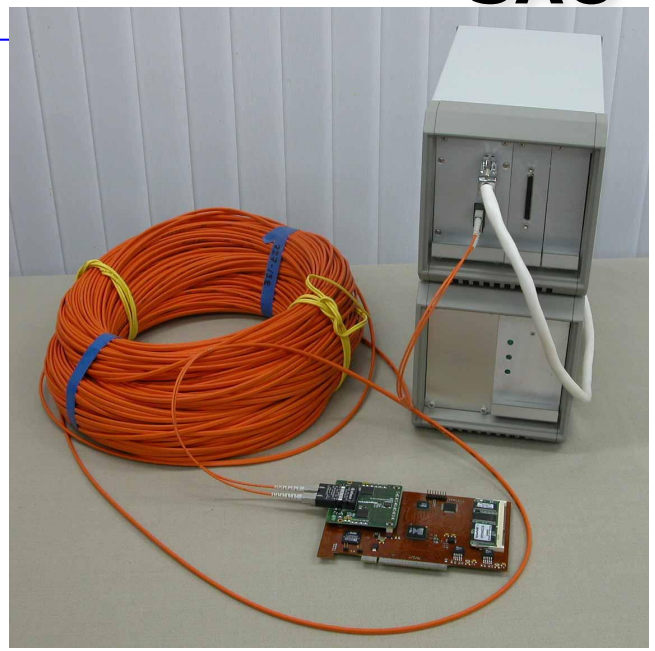
SAO

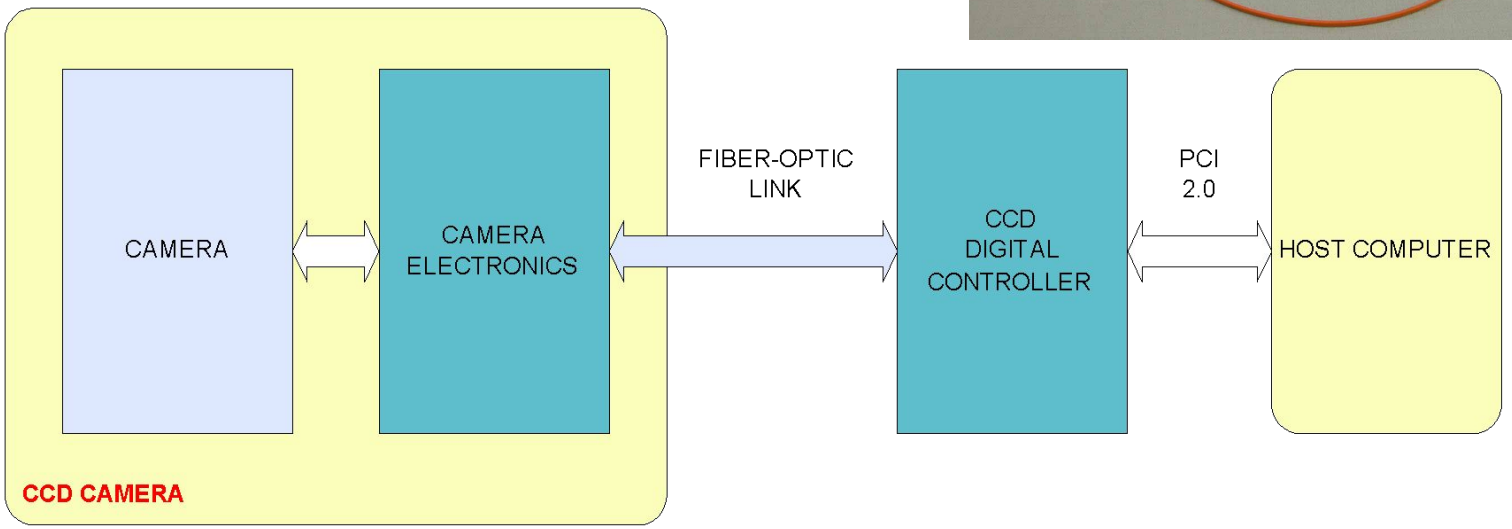
DINACON III block diagram

SAO

- Main components:

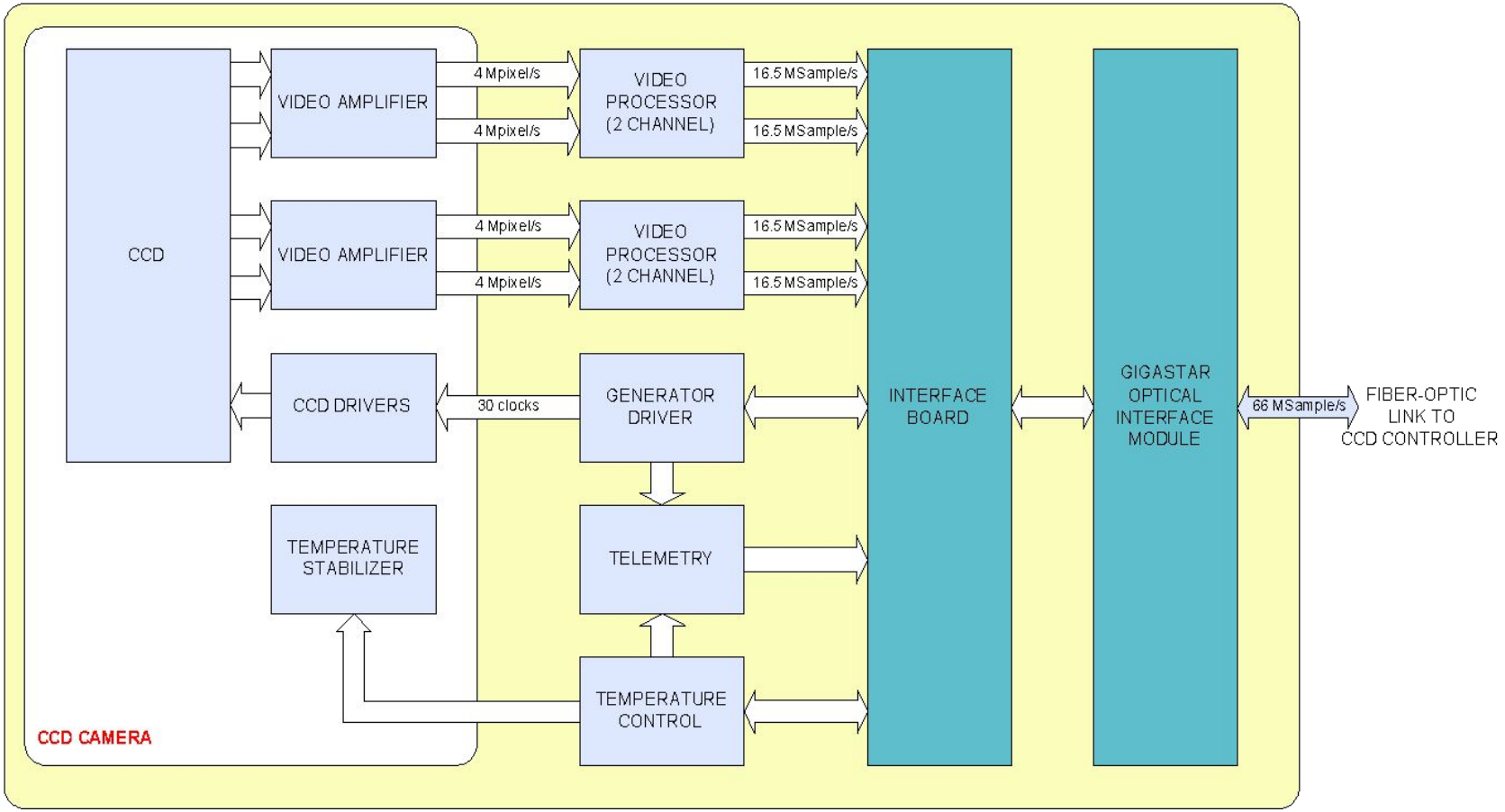
- **System controller**
- **1 Gbit fiber-optic link**
- **Camera electronics**





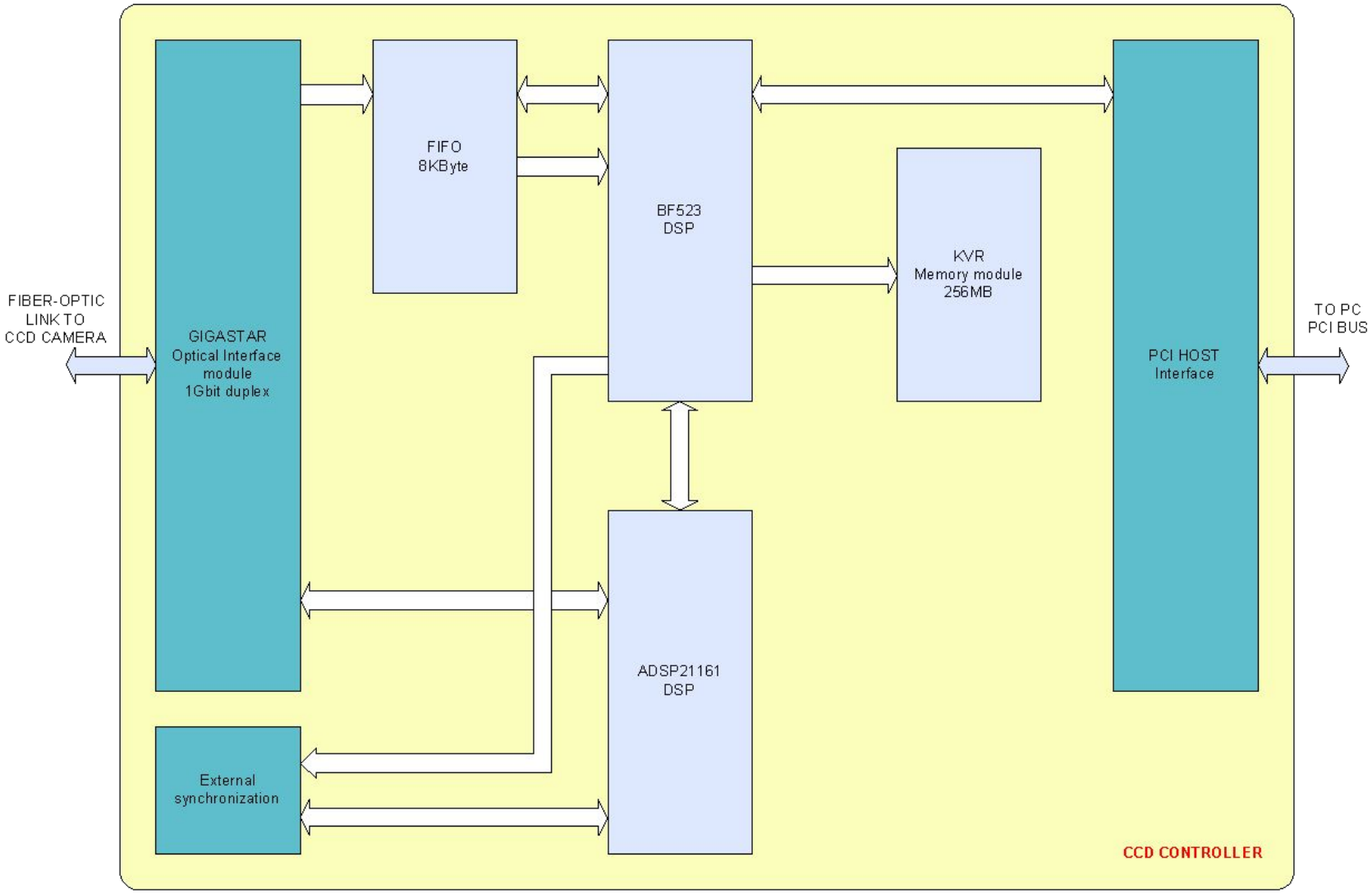
Camera Electronics block diagram

SAO



System controller block diagram

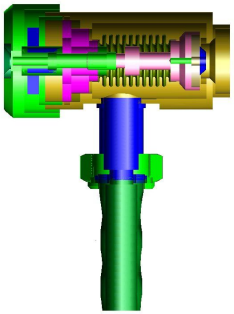
SAO

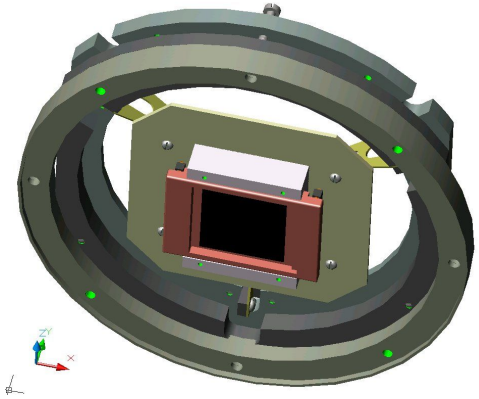


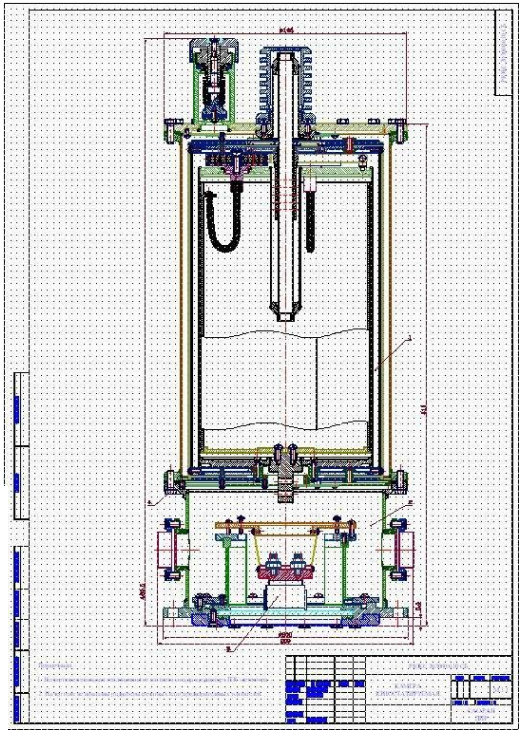
ADLab's resources

SAO

- 2D and 3D computer aided design of CCD systems with release of full design documentation suite
- Structural and thermal simulation of construction units for providing of design requirements



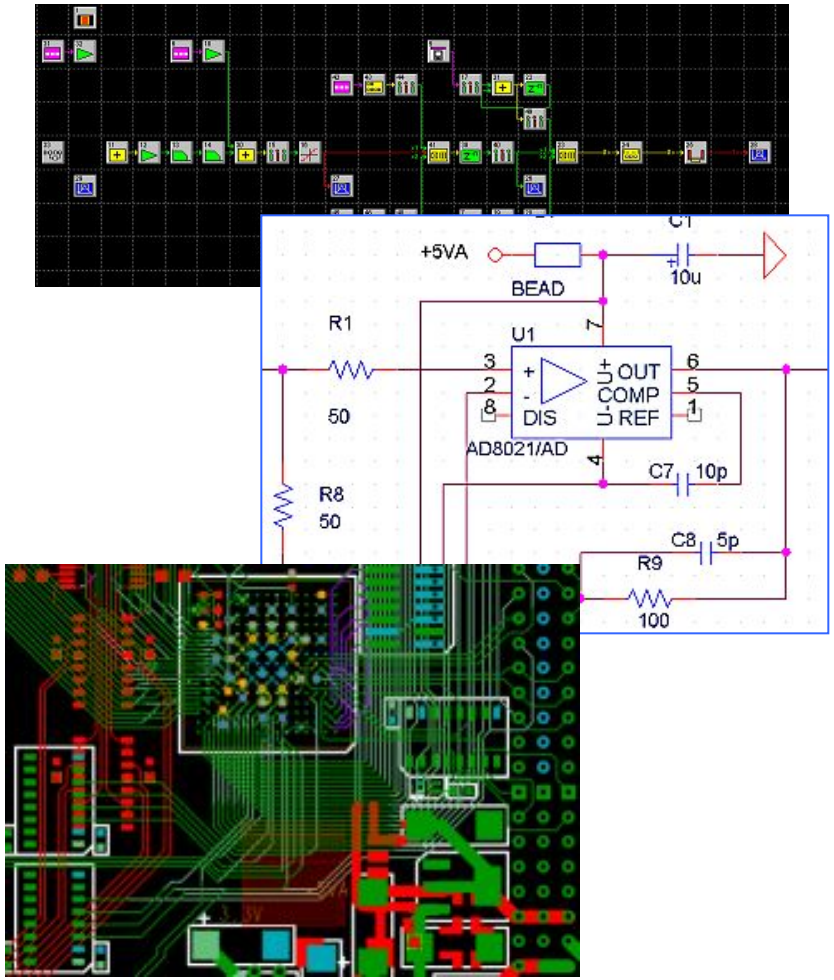




ADLab's resources

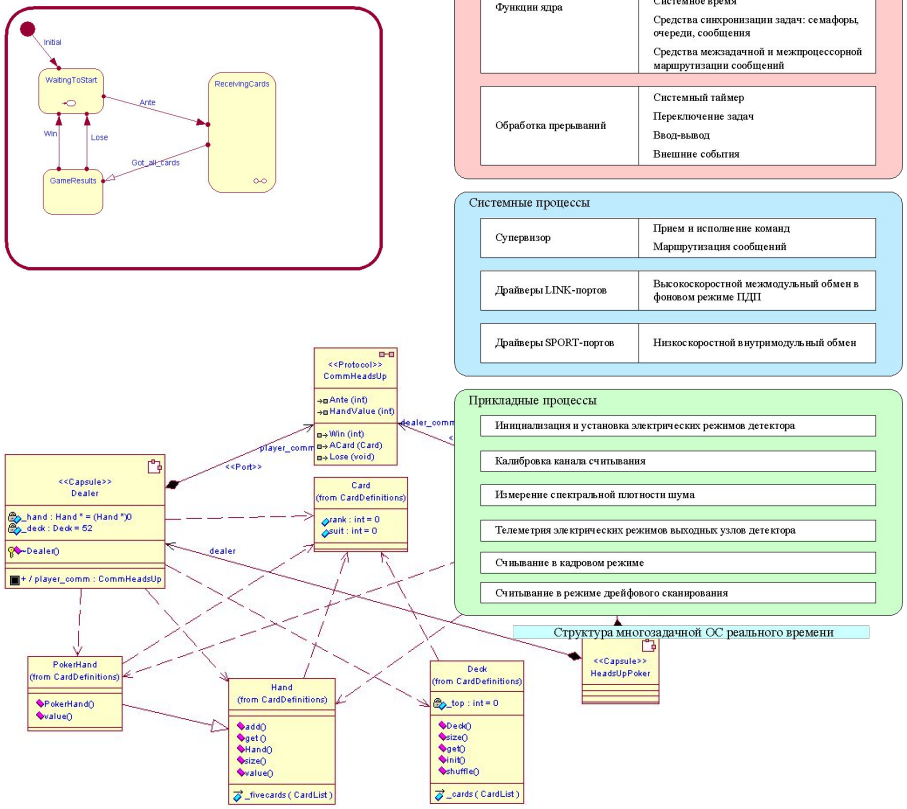
SAO

- Detailed mathematical model construction of signals formation and processing for minimization of distortions, noise and instabilities
- Computer aided design of electronics based on IC of all integration levels (including BGA packages) and technology of surface-mount multi-layer PCBs
- Computer simulation and analysis of electronic circuits and PCBs for compliance to electrical, thermal, noise requirements



ADLab's resources

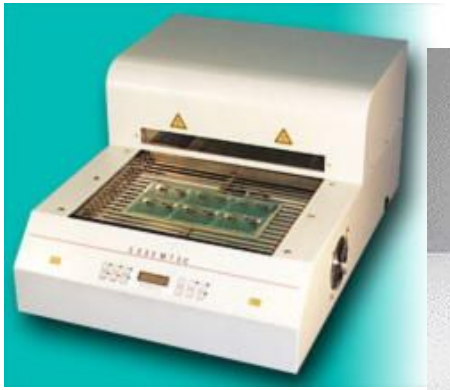
SAO

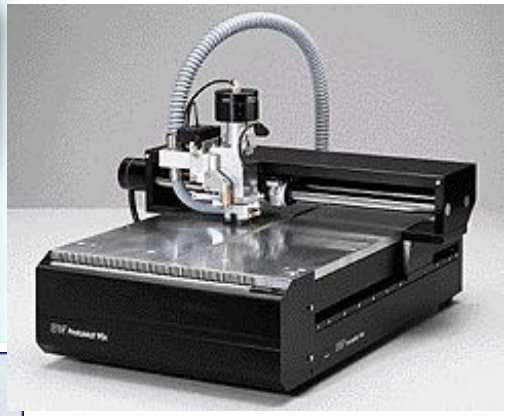


- Development of embedded software for digital signal processors
- Development of multitasking real-time kernels for multi-processor systems
- Application of object-oriented modelling language UML for effective development of complex software systems

ADLab's resources

SAO

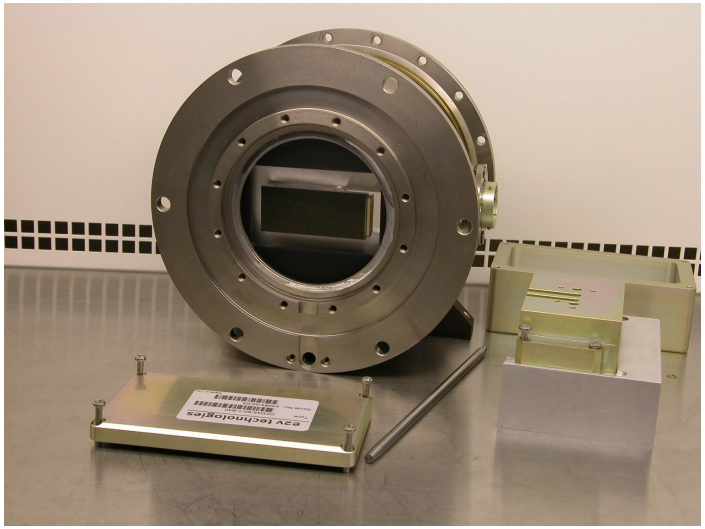


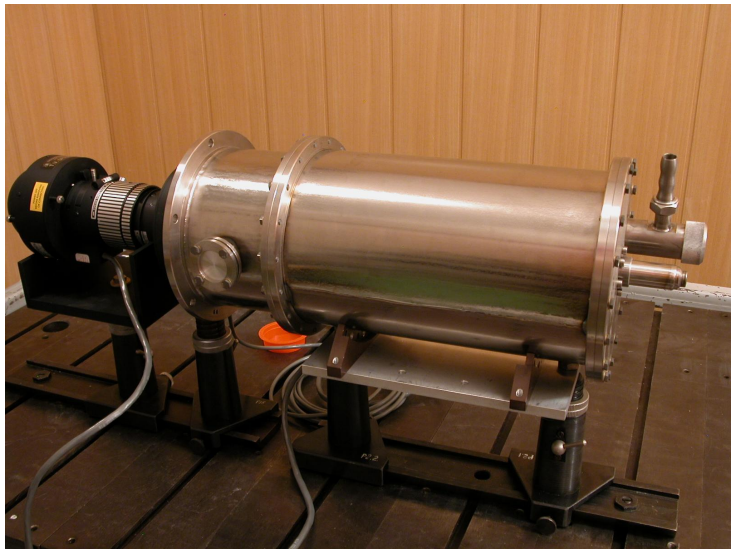


- Production of multi-layer PCB prototypes
- Surface mounting of electronic components on PCBs (including IC with BGA packages)
- Embedded software debugging by in-circuit emulators and digital storage oscilloscopes

ADLab's resources

SAO





- Assembling of CCD cameras in dust-free conditions
- Testing of CCDs performance
- Research of non-documented physical properties of CCDs for optimization of signal processing quality