

# Мікропроцесорна техніка

(лекція 6)  
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2019 р.

**PSoC Creator 4.2**  
**Designing with PSoC 3/5**



# Мікропроцесорн а техніка

## ADC+LCD

PSoC Creator 4.2  
Designing with PSoC 3/5



**PSoC 3/5 включає в себе можливість обробки аналогових, цифрових і змішаних сигналів, а також можливість формування аналогових і цифрових сигналів, охоплюючи широкий спектр прикладних задач**

## Особливості PSoC 3/5:

- Реконфігуровувані Аналогові модулі:
- Вбудовані АЦП і ЦАП, аналогові фільтри різних типів, підсилювачі аналогових сигналів, компаратори, аналогові модулятори і т. д.
- Реконфігуровувані Цифрові модулі:
- Вбудовані таймери, лічильники, PWM, UART, SPI, IrDA, I2C і т. д.
- Flash від 4КВ до 32КВ для зберігання програми
- SRAM от 256В до 2КВ для зберігання даних
- Процесорне ядро - МК8051, CISC, 4MIPS

**Оптимальними для PSoC являються задачі, коли необхідна обробка аналогових сигналів на апаратному рівні (підсилення, фільтрація, АМ/ФМ модуляція, демодуляція) із наступним перетворенням в цифрову форму в смузі аналогових сигналів до 100 кГц.**

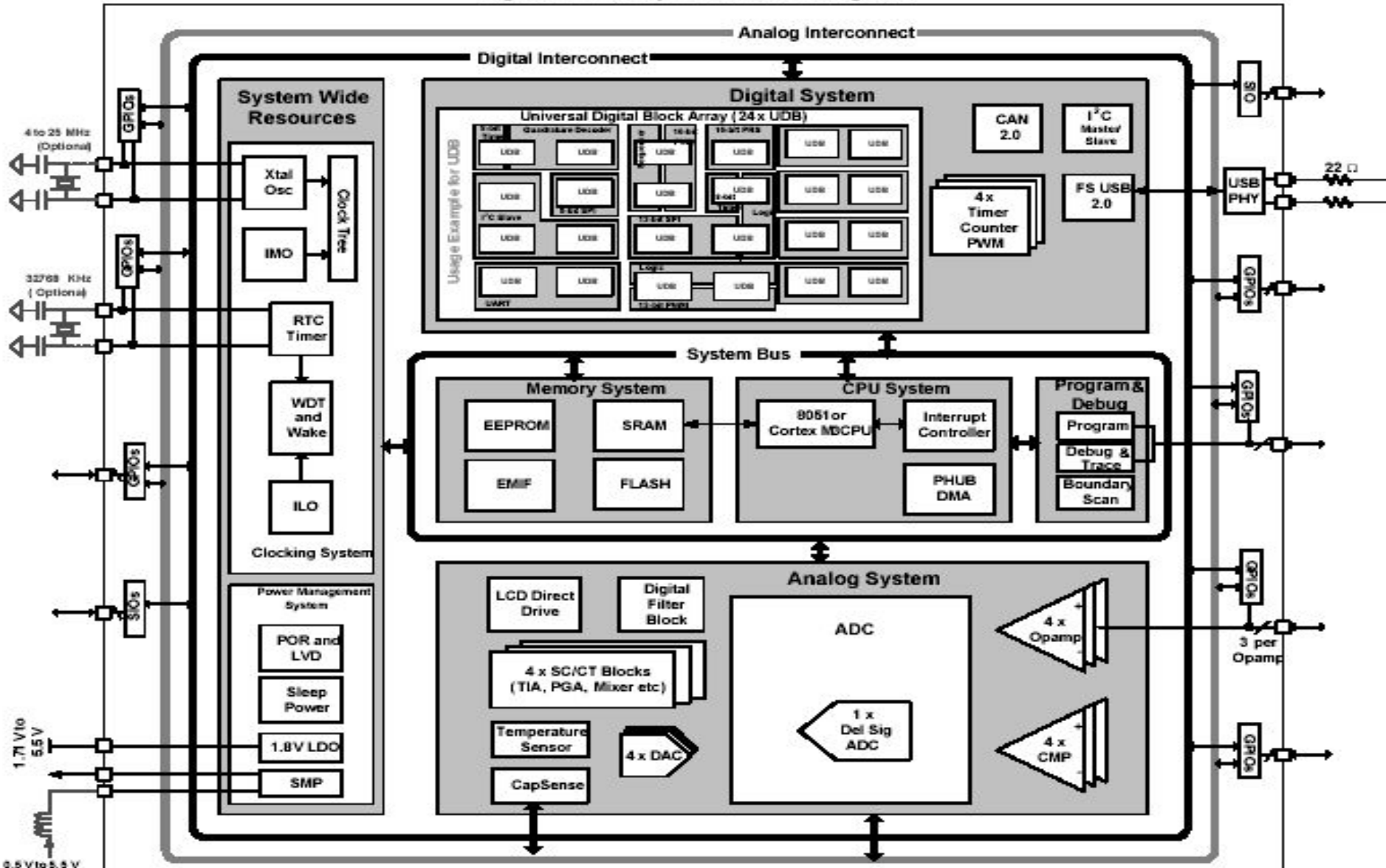
**Виграш полягає в переносі зовнішніх дискретних компонентів у середину процесора.**





# Цифрові та аналогові модулі

Figure 1-1. Simplified Block Diagram



**Принцип дії даного АЦП дещо більш складний, ніж у інших типів АЦП.**

**Його суть в тому, що вхідна напруга порівнюється зі значенням напруги, накопиченим інтегратором.**

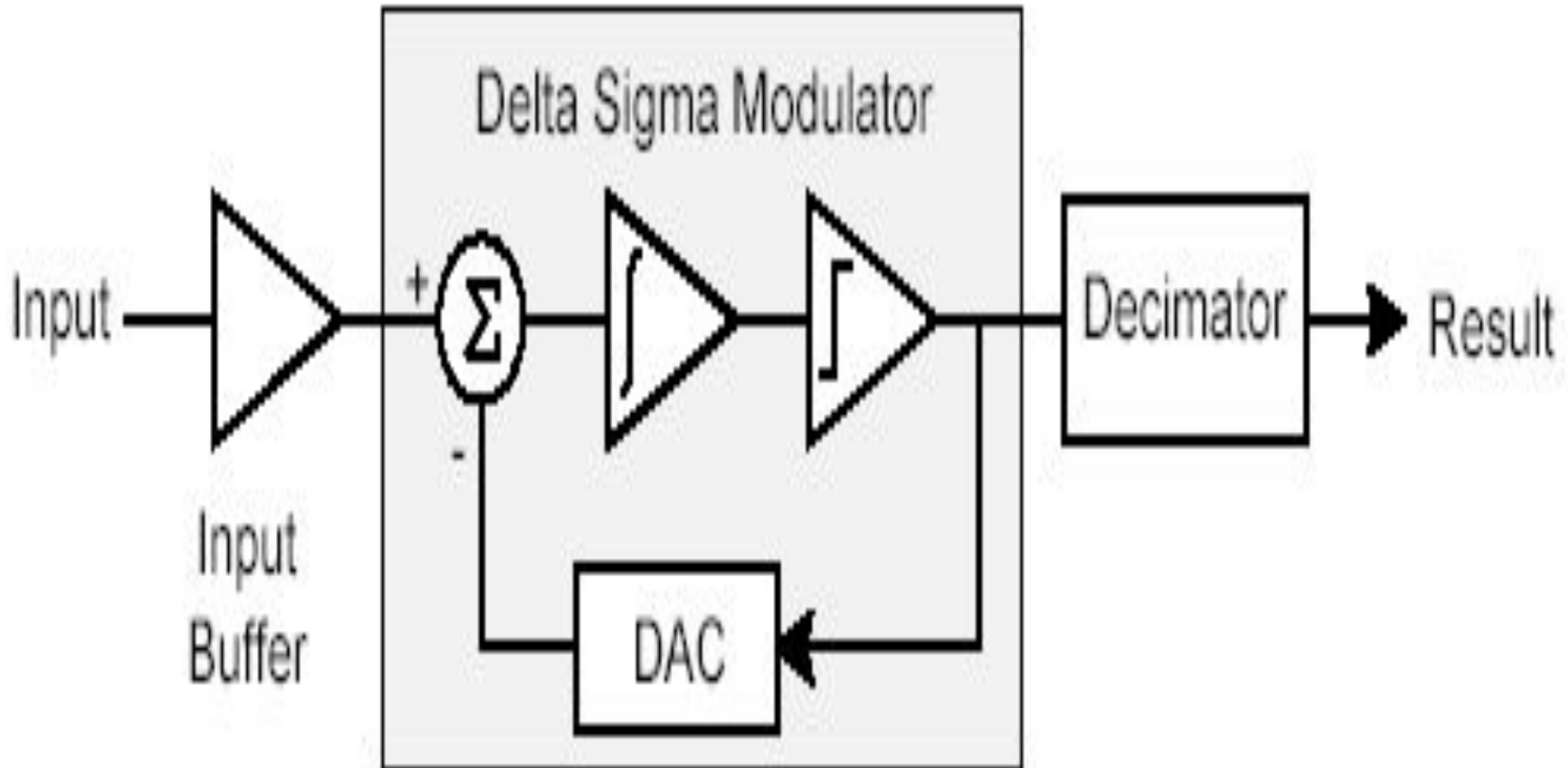
**На вхід інтегратора подаються імпульси позитивної чи від'ємної полярності, в залежності від результату порівняння.**

**Таким чином, даний АЦП представляє собою просту слідкуючу систему: напруга на виході інтегратора «відслідковує» вхідну напругу (рис. ).**

**Результатом роботи даної схеми являється потік нулів та одиниць на виході компаратора, який потім пропускається через цифровий ФНЧ, в результаті отримується N-бітний результат.**

**ФНЧ на рис. об'єднаний з «дециматором», пристроєм, який понижує частоту слідування відліків шляхом їх «проріджування».**

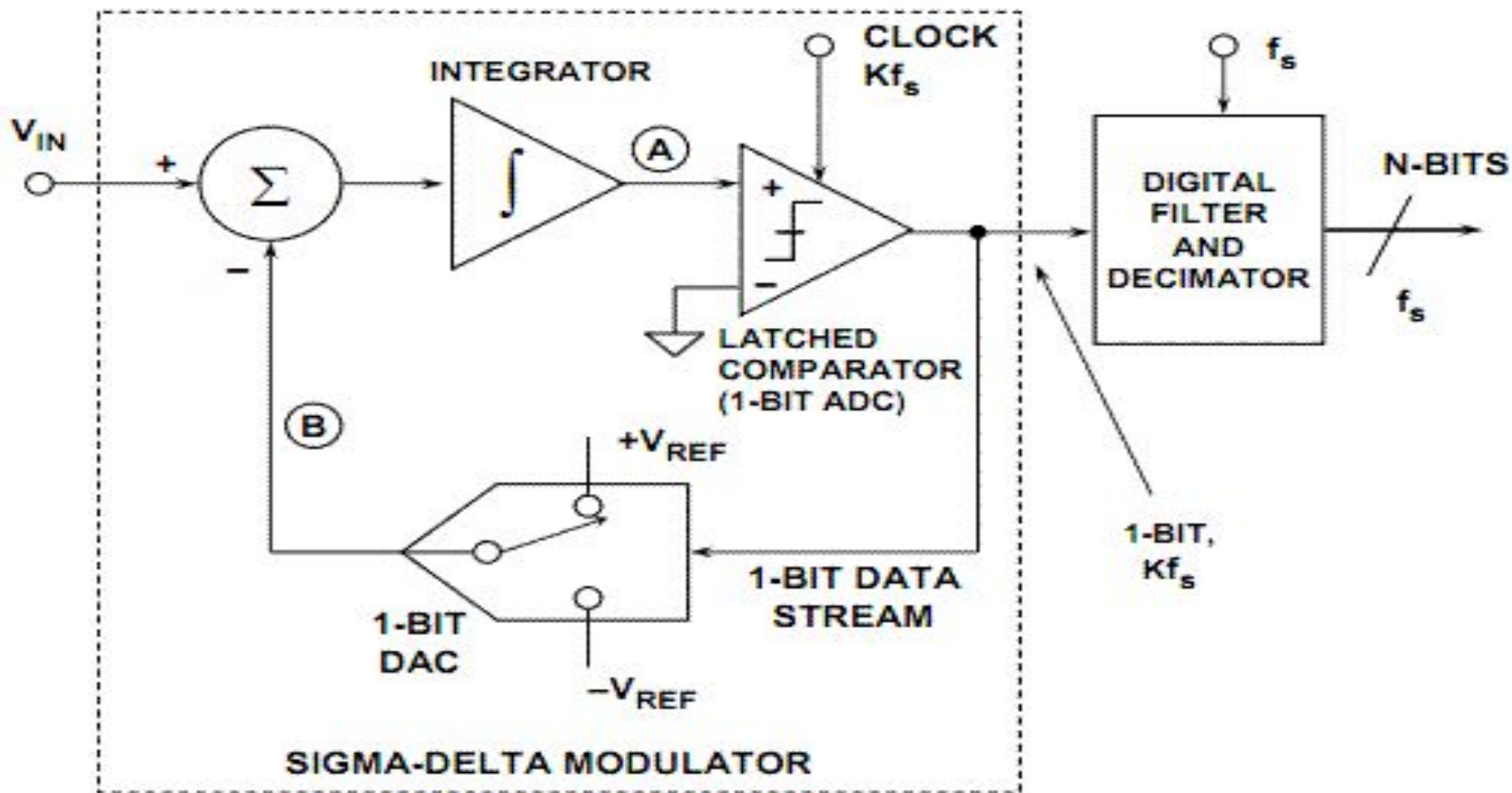




**ADC\_DelSig Block Diagram**



# Delta Sigma Analog to Digital Converter (ADC\_DelSig)

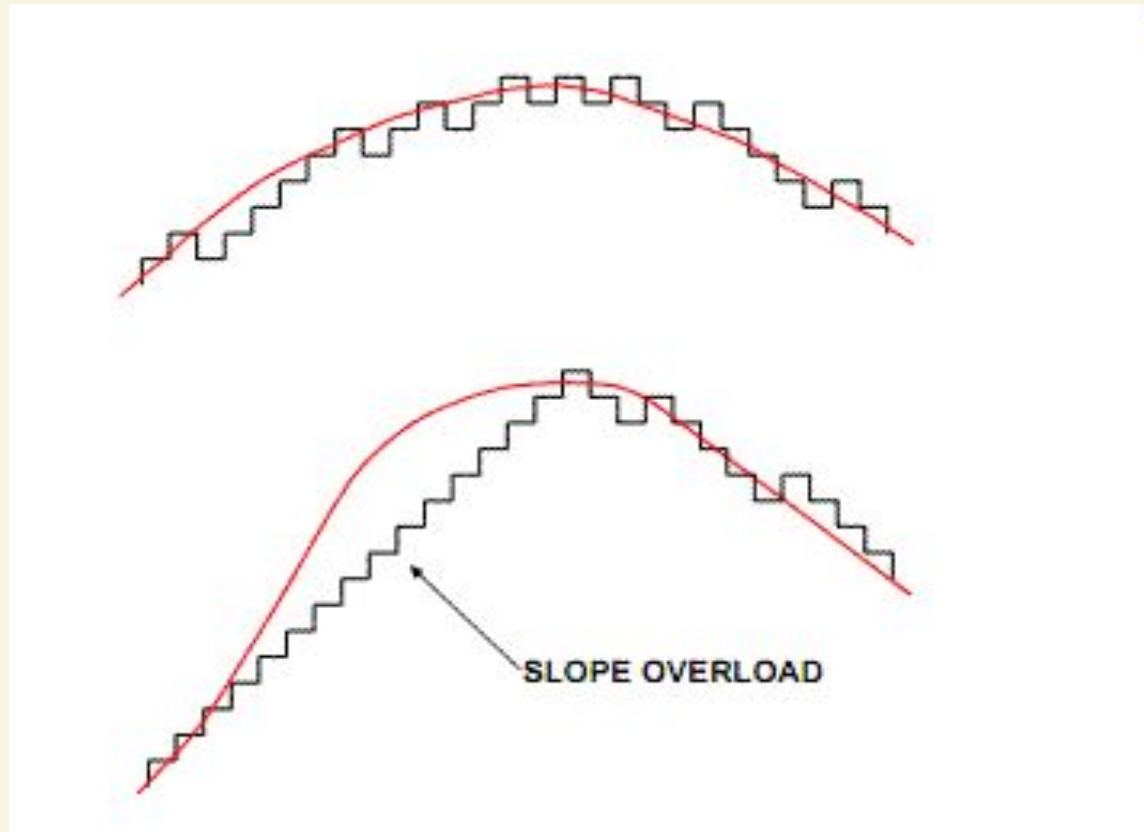


**Структурна схема сигма-дельта АЦП.**



CYPRIOΣ

# Delta Sigma Analog to Digital Converter (ADC\_DelSig)



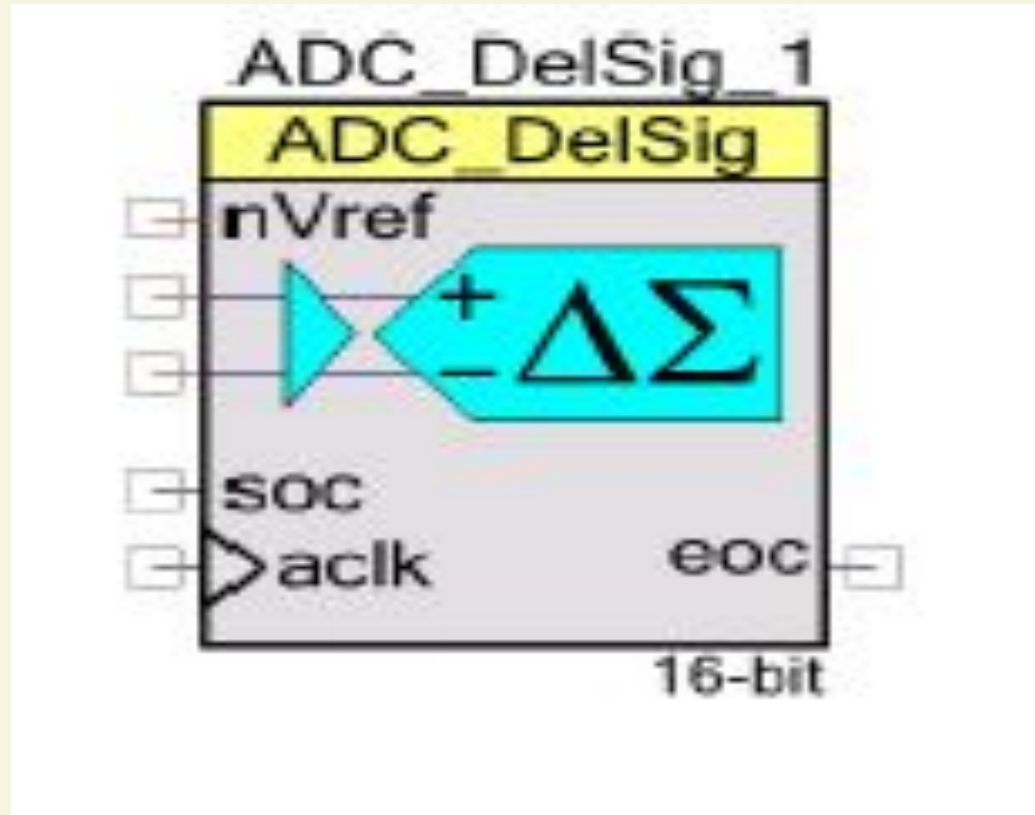
**Сигма-дельта АЦП як слідкуюча система**



# Delta Sigma Analog to Digital Converter (ADC\_DelSig)

- 1. When processing audio information, the ADC\_DelSig is used in a continuous operation mode.**
- 2. When used for scanning multiple sensors, the ADC\_DelSig is used in one of the multisample modes.**
- 3. When used for single-point high-resolution measurements, the ADC\_DelSig is used in single-sample mode.**
- 4. Delta-sigma converters are good for both high-speed medium-resolution (8 to 16 bits) applications, and low-speed high-resolution (16 to 20 bits) applications. The sample rate can be adjusted between 10 and 384000 samples per second, depending on mode and resolution.**

# Delta Sigma Analog to Digital Converter (ADC\_DelSig)



**It can produce 16-bit.**



# Delta Sigma Analog to Digital Converter (ADC\_DelSig)

- 1. When used for single-point high-resolution measurements, the ADC\_DelSig is used in single-sample mode.**
- 2. Delta-sigma converters are good for both high-speed medium-resolution (8 to 16 bits) applications.**
- 3. The sample rate can be adjusted between 2000 and 38400 samples per second, depending on mode and resolution.**

This example project shows how you can use **PSoC** to transfer data from one peripheral (**ADC**) to another (**LDC**),

## Features

- Delta-Sigma ADC in single-ended mode
- LCD used to verify output



PSoC Creator 2.1

File Edit View Debug Project Build Tools Window Help

Workspace Explorer

Source Components Datasheets Results

**Start Page**

PSoC® Creator™

简体中文 日本語 한국어 English

**Recent Projects**

- HelloWorld\_Blinky01.cywrk
- CapSense\_CSD\_Design01...
- CapSense\_CSD\_Design01...
- CharLCD\_CustomFont01.c...
- CharLCD\_CustomFont01.c...

Create New Project...  
Open Existing Project...

**Getting Started**

- PSoC Creator Start Page
- Quick Start Guide
- Intro to PSoC
- Intro to PSoC Creator
- PSoC Creator Training
- Help Tutorials
- Getting Started With PSoC 3
- Getting Started With PSoC 5

**Examples and Kits**

- Find Example Project...
- No Kit Packages Installed

**PSoC Creator News and Information**

**Happy Lunar New Year!**  
Posted on 02/11/2013

Gong Xi Fa Cai! As many of my friends and colleagues are celebrating the New Year and welcoming in the year of the water snake, I wanted to take a minute and wish you all well. May the New Year bring each of you prosperity, good luck and a new PSoC design. ....  
[Read More](#)

**Tips + Tricks: Menu Customization**  
Posted on 01/24/2013

Did you know you can create a customized menu in PSoC® Creator? Right click in a blank area of the top menu and select customize from the

Notice List

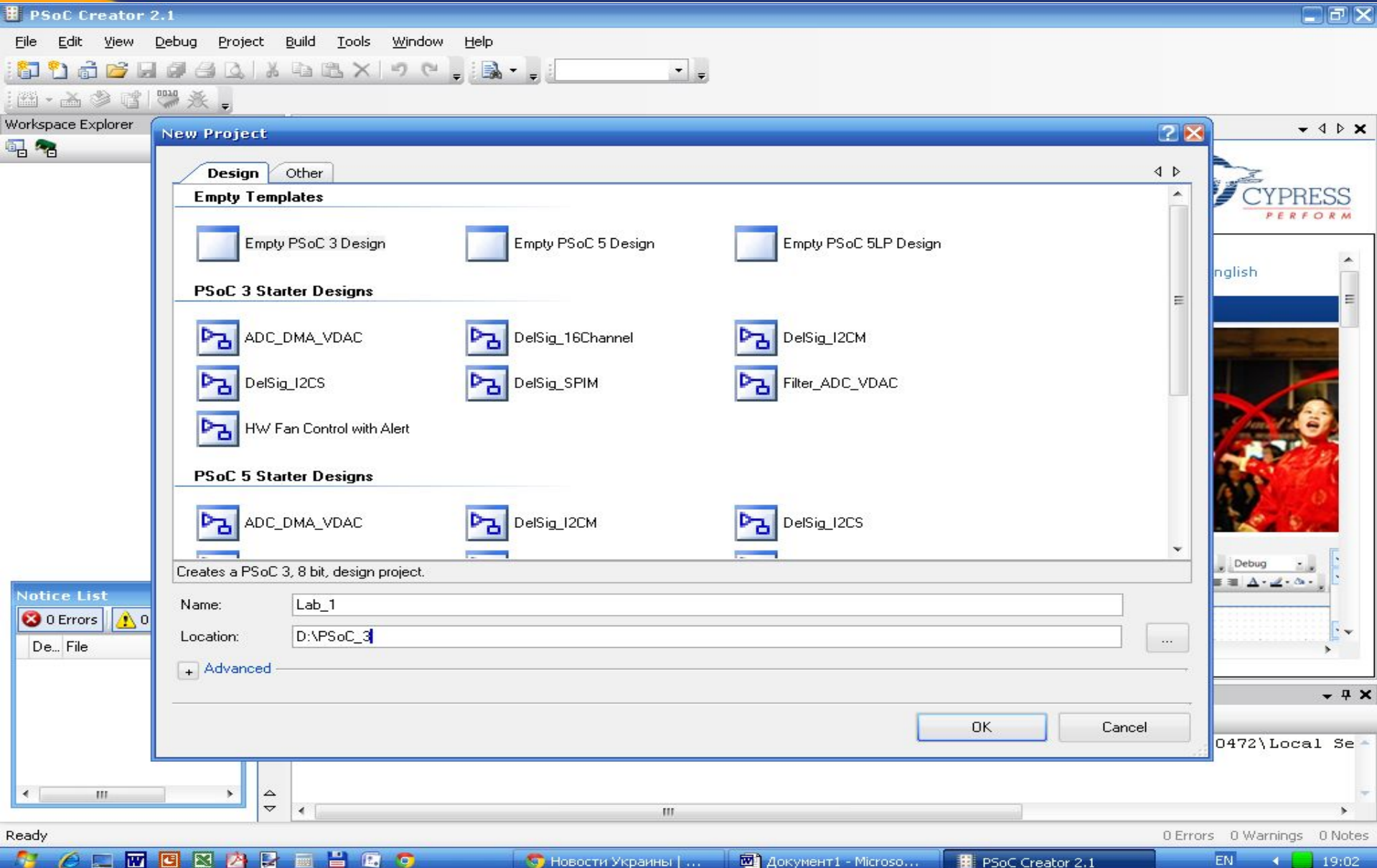
0 Errors 0 Warnings

De... File Error L

Output

Show output from: All

Log file for this session is located at: C:\Documents and Settings\Admin.MICROSOFT-7D0472\Local Se



The screenshot displays the PSoC Creator 2.1 application window. The main menu bar includes File, Edit, View, Debug, Project, Build, Tools, Window, and Help. The toolbar contains various icons for file operations and project management. The 'New Project' dialog box is open, showing the 'Design' tab. It lists several project templates under three categories: 'Empty Templates', 'PSoC 3 Starter Designs', and 'PSoC 5 Starter Designs'. The 'Name' field is set to 'Lab\_1' and the 'Location' field is set to 'D:\PSoC\_3'. The 'Advanced' options are expanded. The 'Notice List' shows 0 errors and 0 warnings. The status bar at the bottom indicates 'Ready' and shows 0 errors, 0 warnings, and 0 notes. The taskbar at the bottom shows the Windows Start button, several open applications, and the system clock showing 19:02 on 0472\Local Se.

**PSoc Creator 2.1**

File Edit View Debug Project Build Tools Window Help

Workspace Explorer

**New Project**

Design Other

**Empty Templates**

- Empty PSoC 3 Design
- Empty PSoC 5 Design
- Empty PSoC 5LP Design

**PSoC 3 Starter Designs**

- ADC\_DMA\_VDAC
- DelSig\_16Channel
- DelSig\_I2CM
- DelSig\_I2CS
- DelSig\_SPIM
- Filter\_ADC\_VDAC
- HW Fan Control with Alert

**PSoC 5 Starter Designs**

- ADC\_DMA\_VDAC
- DelSig\_I2CM
- DelSig\_I2CS

Creates a PSoC 3, 8 bit, design project.

Name: Lab\_1

Location: D:\PSoC\_3

+ Advanced

OK Cancel

Notice List

0 Errors 0 Warnings

De... File

Ready

0 Errors 0 Warnings 0 Notes

Новости Украины | ...

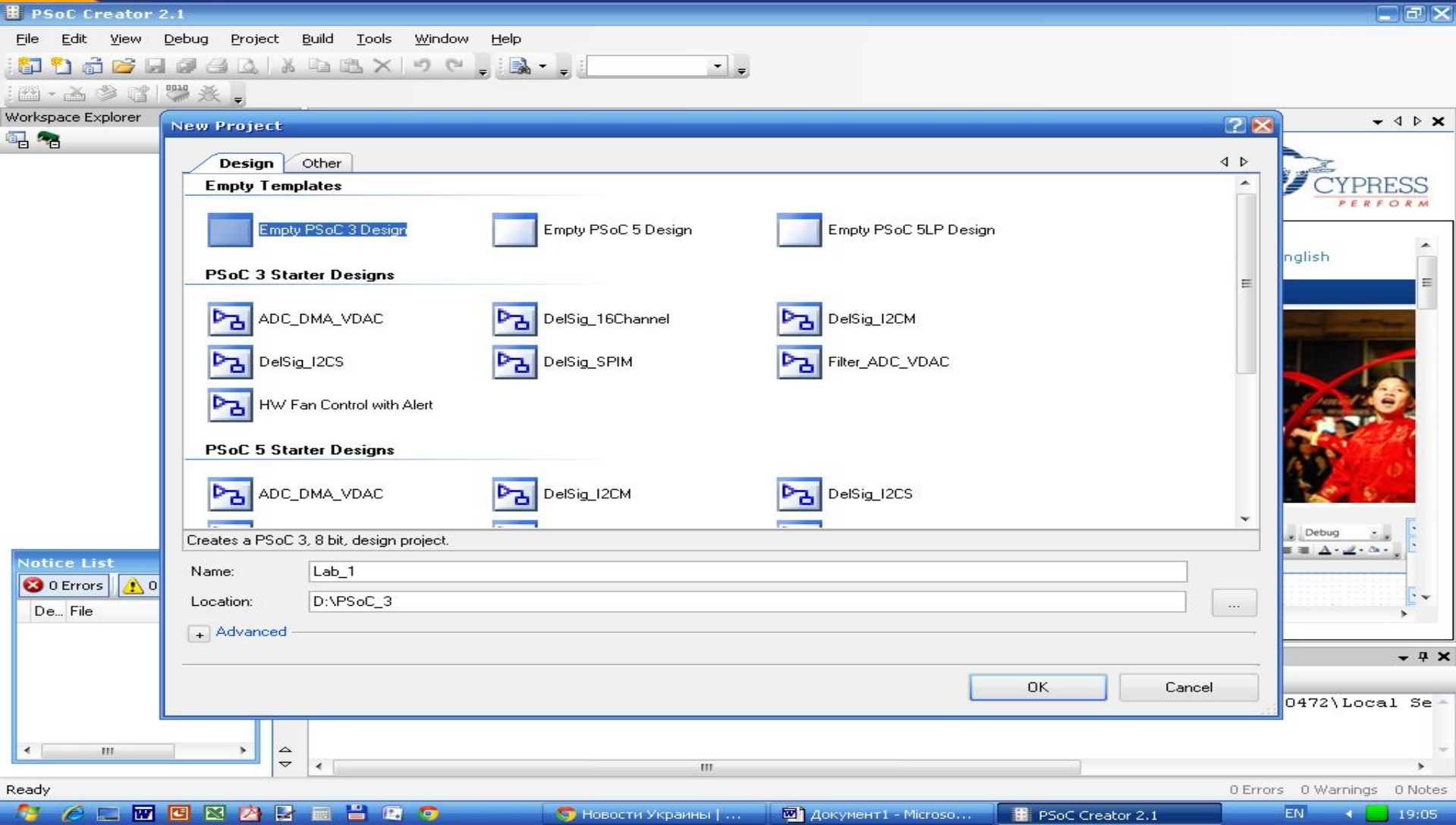
Документ1 - Microso...

PSoc Creator 2.1

EN

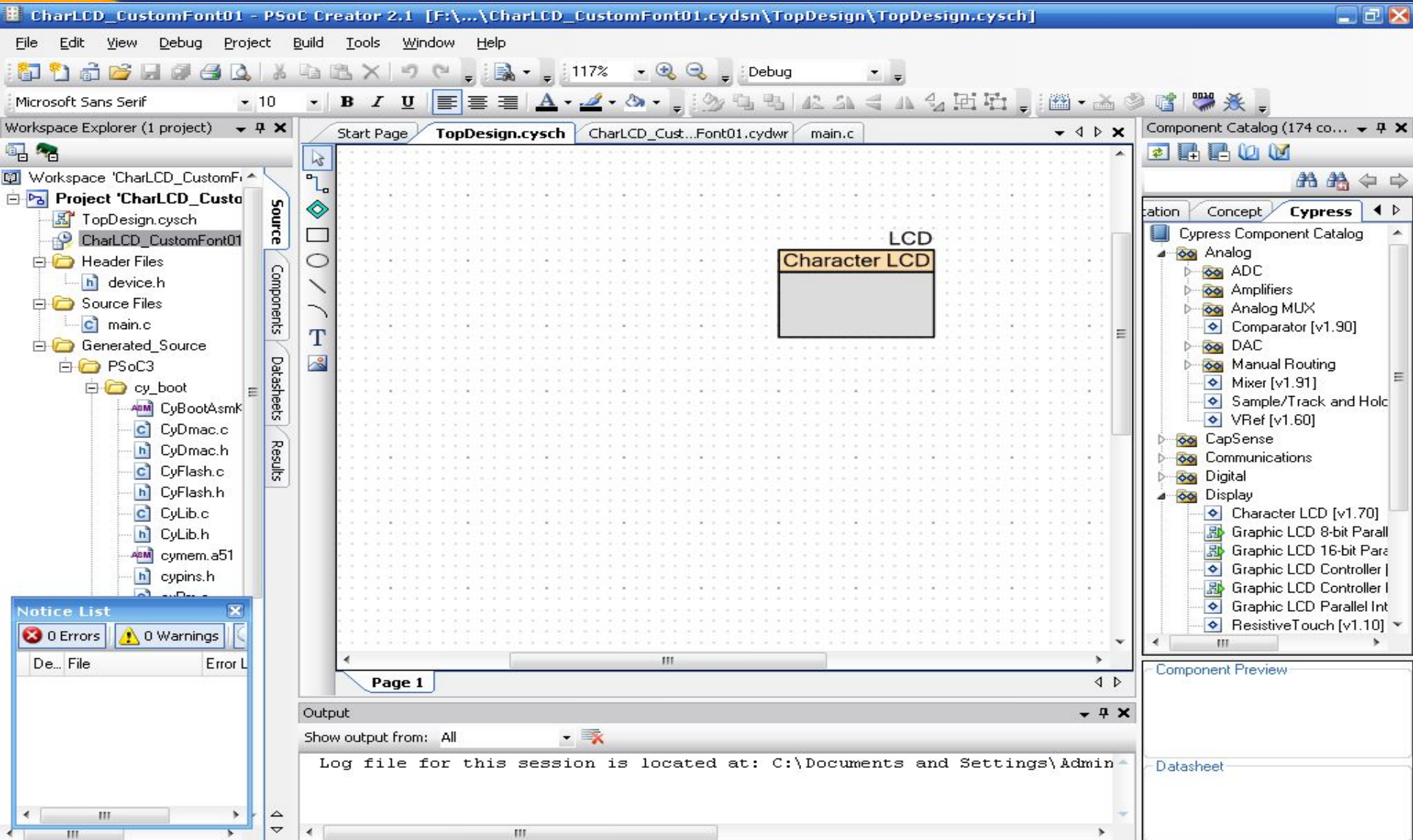
19:02

# Empty PSoC 3/5 Design



The screenshot displays the PSoC Creator 2.1 application window. The main menu includes File, Edit, View, Debug, Project, Build, Tools, Window, and Help. The 'New Project' dialog box is open, showing 'Empty Templates' with options for 'Empty PSoC 3 Design', 'Empty PSoC 5 Design', and 'Empty PSoC 5LP Design'. Below this, there are sections for 'PSoC 3 Starter Designs' and 'PSoC 5 Starter Designs', each containing several pre-configured design templates like 'ADC\_DMA\_VDAC', 'DelSig\_I2CS', 'DelSig\_I2CM', 'DelSig\_16Channel', 'DelSig\_SPIM', and 'Filter\_ADC\_VDAC'. The 'Name' field is set to 'Lab\_1' and the 'Location' is 'D:\PSoC\_3'. The status bar at the bottom indicates '0 Errors 0 Warnings 0 Notes' and the system clock shows '19:05'.

# Lab\_6 ADC+LCD



CharLCD\_CustomFont01 - PSoC Creator 2.1 [F:\...\CharLCD\_CustomFont01.cydsn\TopDesign\TopDesign.cysch]

File Edit View Debug Project Build Tools Window Help

Microsoft Sans Serif 10 B I U

Workspace Explorer (1 project)

Project 'CharLCD\_CustomFont01'

- TopDesign.cysch
- CharLCD\_CustomFont01
  - Header Files
    - device.h
  - Source Files
    - main.c
  - Generated\_Source
    - PSoC3
      - cy\_boot
        - CyBootAsmk
        - CyDmac.c
        - CyDmac.h
        - CyFlash.c
        - CyFlash.h
        - CyLib.c
        - CyLib.h
        - cymem.a51
        - cypins.h

Component Catalog (174 components)

Cypress Component Catalog

- Display
  - Character LCD [v1.70]

Notice List

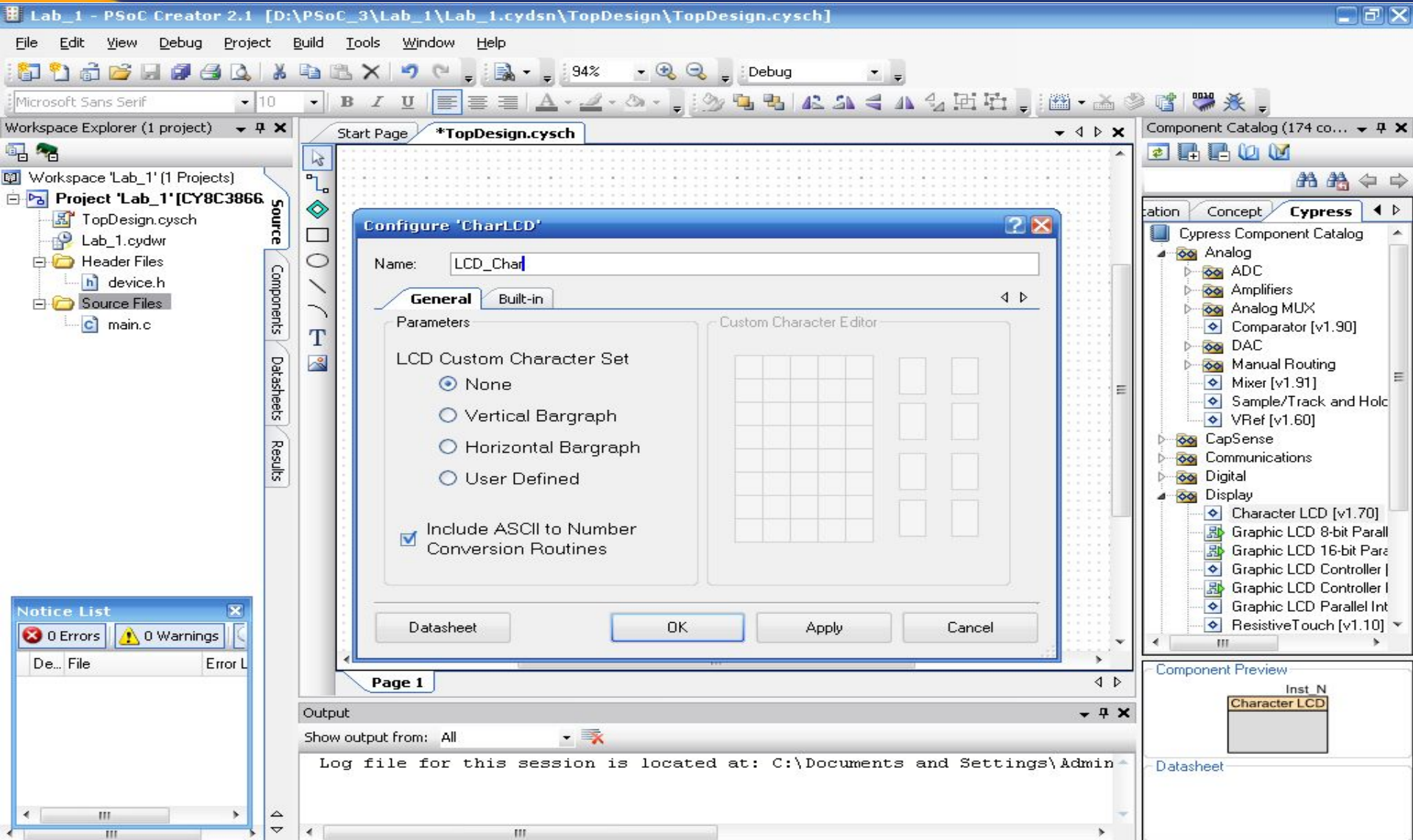
0 Errors 0 Warnings

Output

Show output from: All

Log file for this session is located at: C:\Documents and Settings\Admin...

# Configure LCD



Lab\_1 - PSoC Creator 2.1 [D:\PSoc\_3\Lab\_1\Lab\_1.cydsn\TopDesign\TopDesign.cysch]

File Edit View Debug Project Build Tools Window Help

Microsoft Sans Serif 10 B I U

Workspace Explorer (1 project)

Project 'Lab\_1' [CY8C3866]

- TopDesign.cysch
- Lab\_1.cydwr
- Header Files
- device.h
- Source Files
- main.c

Start Page \*TopDesign.cysch

Component Catalog (174 co...)

Character LCD [v1.70]

Graphic LCD 8-bit Paralle...

Graphic LCD 16-bit Paralle...

Graphic LCD Controller I...

Graphic LCD Controller I...

Graphic LCD Parallel Int...

Resistive Touch [v1.10]

Component Preview

Inst N

Character LCD

Datasheet

Output

Show output from: All

Log file for this session is located at: C:\Documents and Settings\Admin...

Page 1

Notice List

0 Errors 0 Warnings

De... File Error L

Ready {X=295,Y=131} 0 Errors 0 Warnings 0 Notes

Новости Украины | ... Do\_Present\_1.doc - ... PSoC Creator 2.1 EN 19:25

# Lab\_6 ADC+LCD

Lab\_1 - PSoC Creator 2.1 [D:\PSoC\_3\Lab\_1\Lab\_1.cydsn\Lab\_1.cydwr]

File Edit View Debug Project Build Tools Window Help

37% Debug

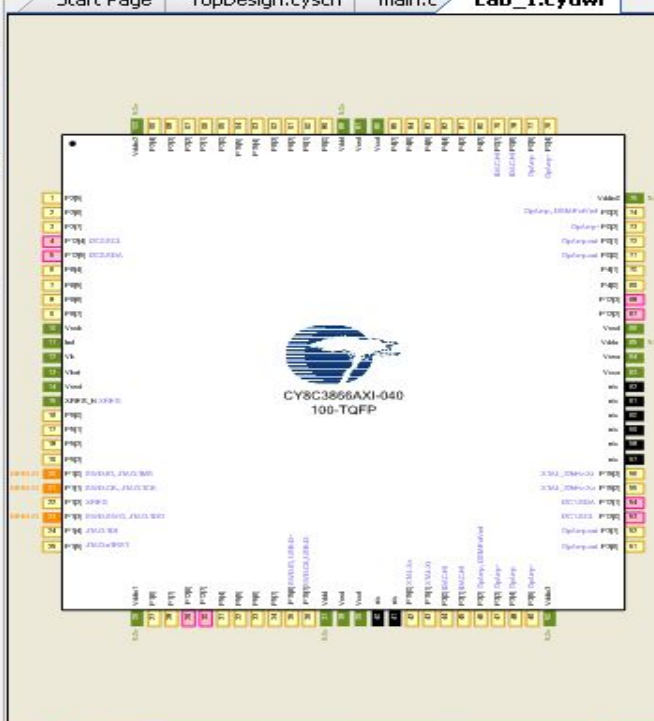
Workspace Explorer (1 project)

Workspace 'Lab\_1' (1 Projects)

- Project 'Lab\_1' [CY8C3866]
  - TopDesign.cysch
  - Lab\_1.cydwr
  - Header Files
    - device.h
  - Source Files
    - main.c

Source Components Datasheets Results

Start Page TopDesign.cysch main.c Lab\_1.cydwr



Alias	Name	Port	Pin	Lock
	\LCD_Char:LCDPort[6:0]\			
	P0[6:0]	IDAC:HC		
	P0[7:1]	IDAC:HC		
	P2[6:0]			
	P2[7:1]			
	P3[6:0]	OpAmp:c		
	P3[7:1]	OpAmp:c		
	P4[6:0]			
	P4[7:1]			
	P5[6:0]			

LCD\_Char\_LCDPort\_6 - Digital  
LCD\_Char\_LCDPort\_5 - Digital  
LCD\_Char\_LCDPort\_4 - Digital

Pins Analog Clocks Interrupts DMA System Directives Flash Security

Output

Show output from: All

Log file for this session is located at: C:\Documents and Settings\Admin.MICROSOFT-7D0472\Local Se

Notice List

0 Errors 0 Warnings

De... File Error L

Ready

0 Errors 0 Warnings 0 Notes

EN 19:33

## **Adding Components**

**To see how the ADC works we need an analog signal to convert. We're going to use a potentiometer to provide one analog signal. A basic potentiometer provides a great diagnostic tool for analog processing since you can slowly sweep the signal through the range of the potentiometer and observe the output. Char LCD to provide visual feedback.**

- 1. Drag an Analog Pin component onto your design.**
- 2. Name it VR\_Pin. This pin will be connected to the potentiometer on the DVK.**
- 3. The potentiometer output will send to the ADC.**

**This design adds only one external pin for the potentiometer.**

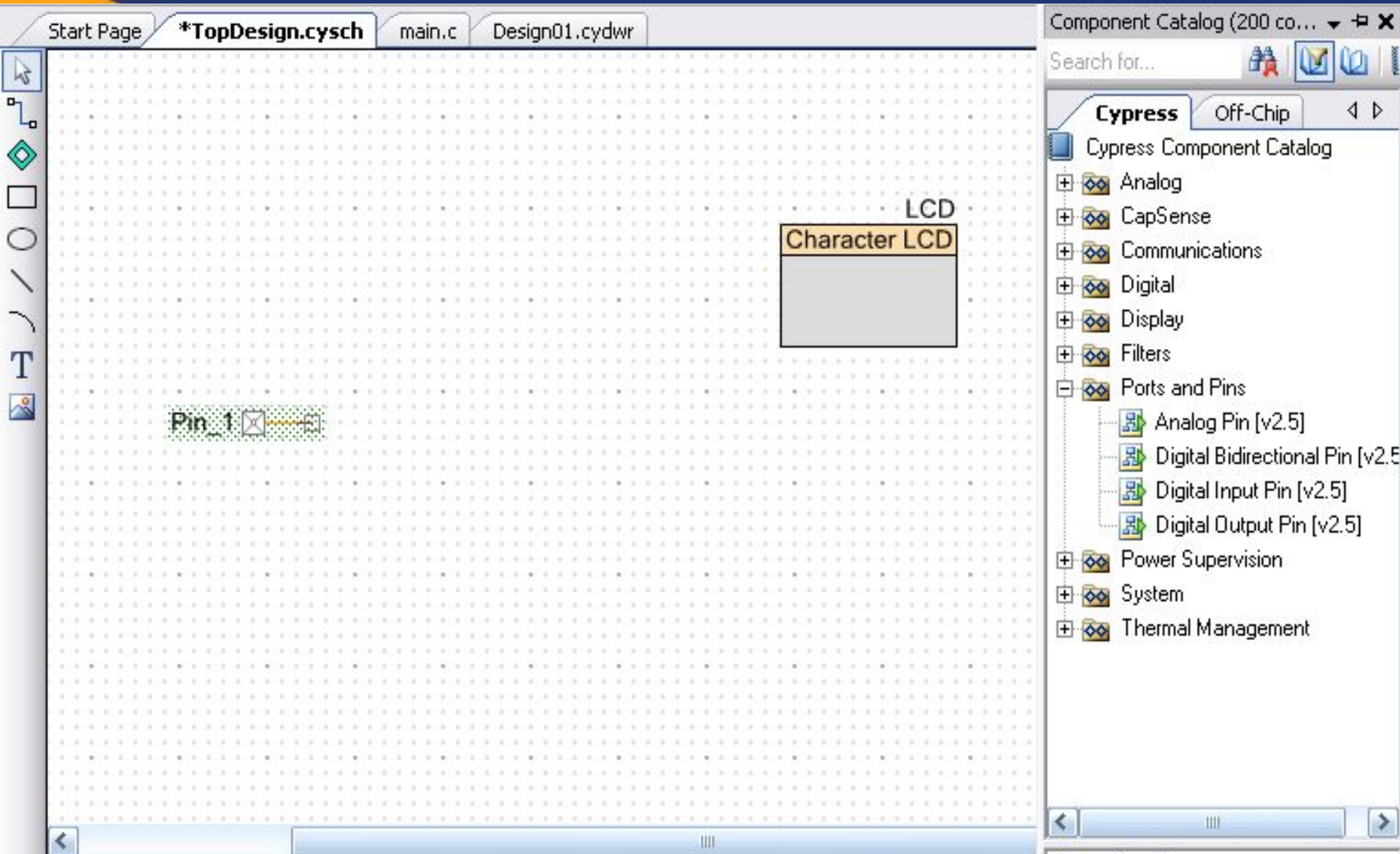
- **Open the design-wide resource file and assign the pins (Рис.1).**
- **Build the project.**
- **Add a wire to the DVK board connecting P0\_7 to the VR.**
- **Make sure the VR\_PWR jumper on the DVK is placed properly to provide power to the potentiometer.**

	\CharLCD:LCDPort\[6:0]	P2[6:0]	▼	☑
	VR_Pin	P0[7]	▼	☑

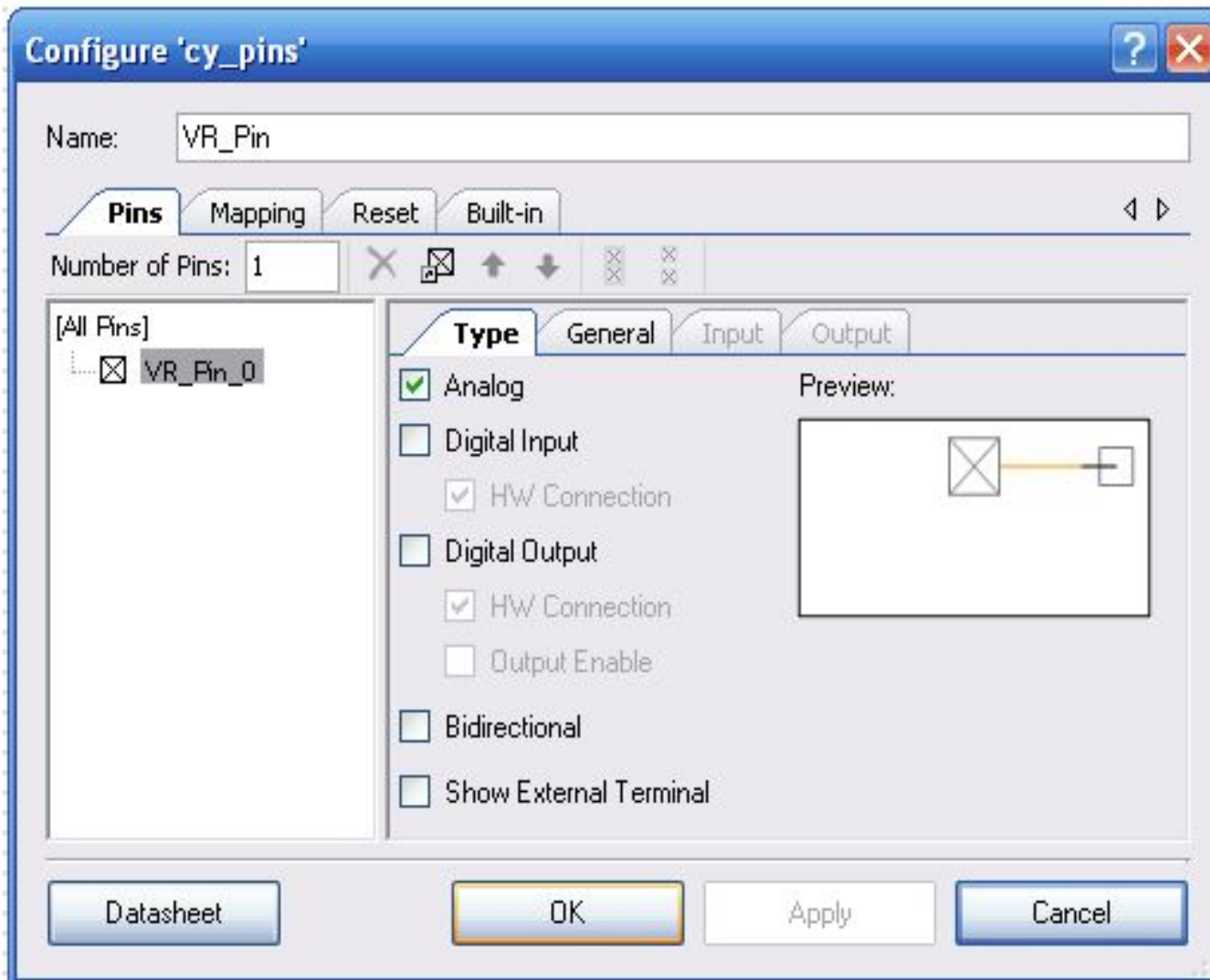
Рис.1



# Lab\_6 ADC+LCD



The screenshot shows the Cypress PSoC Designer IDE interface. The main workspace contains a schematic design on a grid. A component labeled "Character LCD" is placed on the right side, with the text "LCD" above it. On the left side, a component labeled "Pin\_1" is placed, with a small icon next to it. The top of the window shows tabs for "Start Page", "\*TopDesign.cysch", "main.c", and "Design01.cydwr". On the right side, the "Component Catalog" is open, showing a search bar and a tree view of components. The tree view is expanded to show the "Ports and Pins" category, which includes "Analog Pin [v2.5]", "Digital Bidirectional Pin [v2.5]", "Digital Input Pin [v2.5]", and "Digital Output Pin [v2.5]". Other categories visible include "Analog", "CapSense", "Communications", "Digital", "Display", "Filters", "Power Supervision", "System", and "Thermal Management".



Start Page

\*TopDesign.cysch

main.c

Design01.cydwr

## Configure 'cy\_pins'

Name: VR\_Pin

Pins

Mapping

Reset

Built-in

Number of Pins: 1

[All Pins]

 VR\_Pin\_0

Type

General

Input

Output

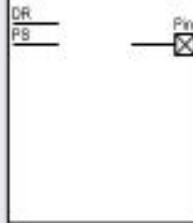
Drive Mode

High Impedance Analog

Initial State:

Low (0)

Minimum Supply Voltage:



Datasheet

OK

Apply

Cancel



## Lab\_6 Adding Components

- Drag an **Analog Pin** component onto your design  
Name it **VR\_Pin**.  
This pin will be connected to the potentiometer on the DVK
- Add a **Delta Sigma ADC** component from the Component Catalog to your design
- Double Click the **ADC** to configure it.  
Name the component **ADC**.
- Set the **Conversion Mode** to **Continuous**.
- Set the **Resolution** to be **14** bits and the **Conversion Rate** to be **5,000 SPS** (samples per second).
- Set the **Input Range** to be **Vssa to Vdda (Single Ended)**
- Set the **Input Buffer Gain** to **1**
- Select **Single Ended** Input mode

Start Page \*TopDesign.cysch main.c Design01.cydwr

Component Catalog (200 co... Search for...

**Cypress** Off-Chip

Cypress Component Catalog

- Analog
  - ADC
    - Delta Sigma ADC [v...
  - Amplifiers
  - Analog MUX
  - Comparators
  - DAC
  - Manual Routing
  - Mixer [v2.0]
  - Sample/Track and Hold
  - VRef [v1.60]
- CapSense
- Communications
- Digital
- Display
- Filters
- Ports and Pins
- Power Supervision
- System

VR\_Pin [07] →

ADC\_DelSig\_1  
ADC\_DelSig

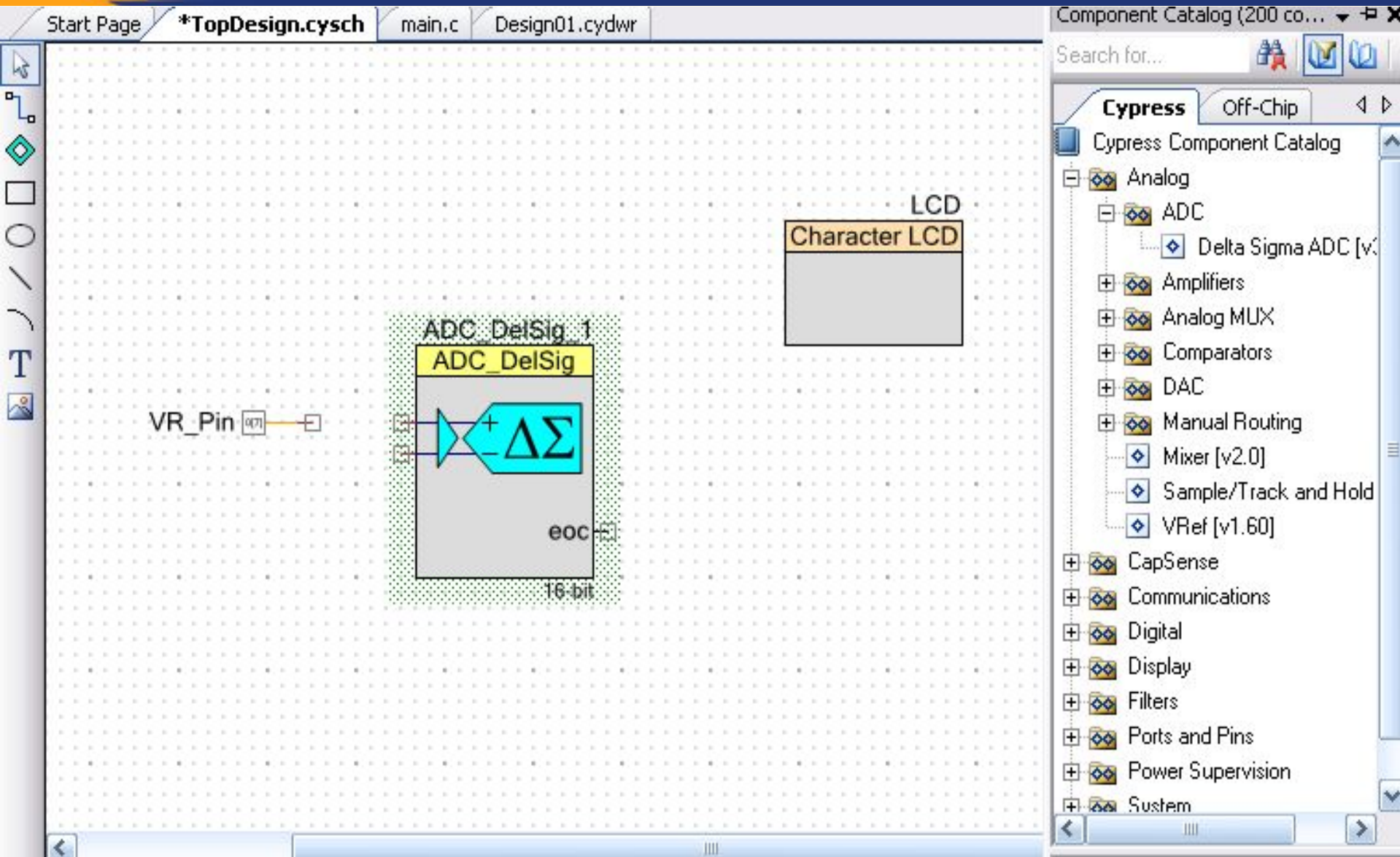
+

ΔΣ

eoc

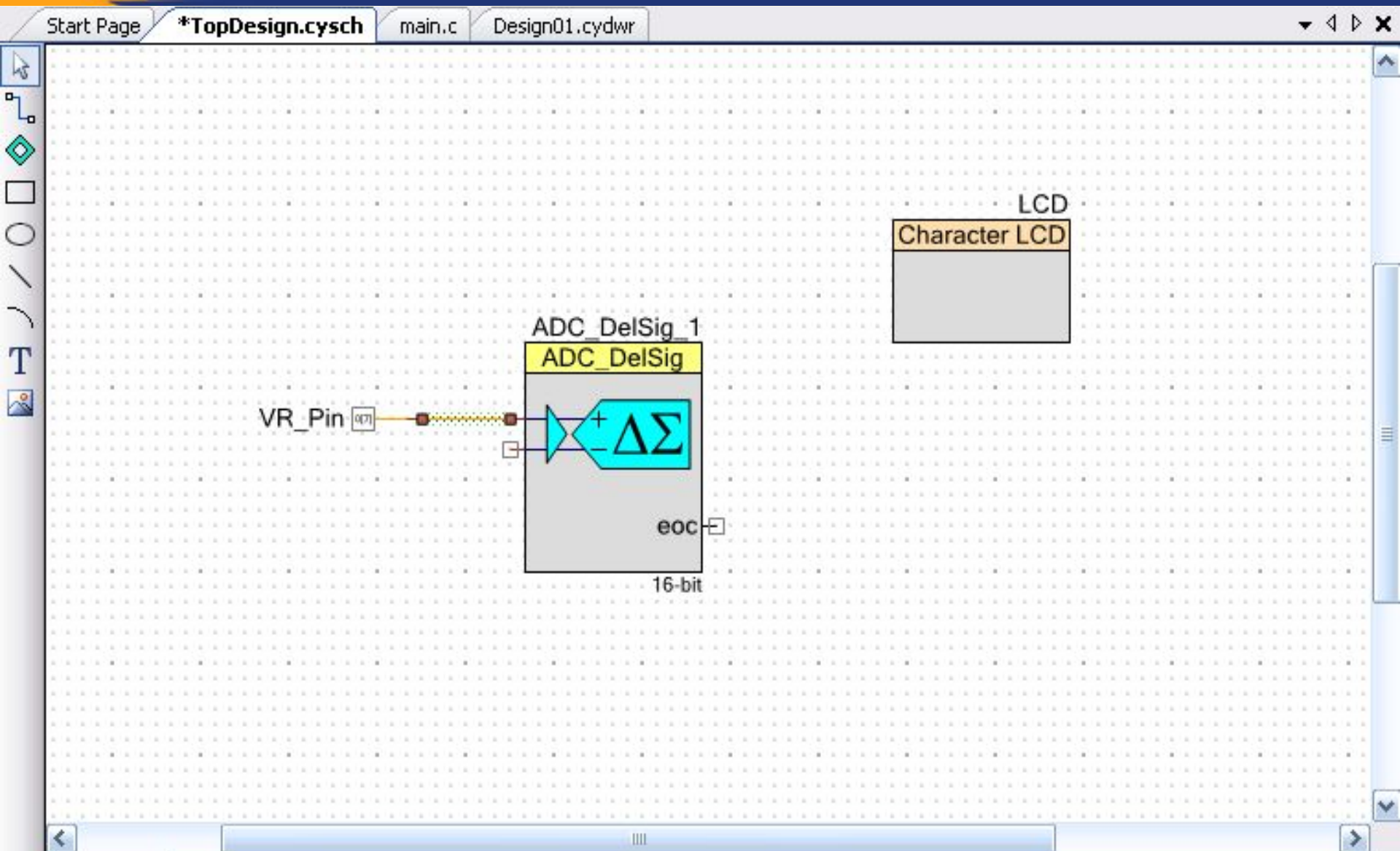
16-bit

LCD  
Character LCD



The screenshot shows the Cypress PSoC Designer interface. The main workspace contains a schematic diagram on a grid. On the left, a component labeled 'VR\_Pin' with a value of '07' is connected to the input of an ADC component. The ADC component is labeled 'ADC\_DelSig\_1' and 'ADC\_DelSig'. It features a cyan-colored Delta-Sigma (ΔΣ) converter symbol. Below the ADC symbol, the text 'eoc' and '16-bit' are visible. To the right of the ADC is a rectangular component labeled 'LCD' and 'Character LCD'. The right-hand side of the window displays the 'Component Catalog' with a search bar and a tree view. The tree view is expanded to show the 'Analog' category, which includes 'ADC', 'Amplifiers', 'Analog MUX', 'Comparators', 'DAC', 'Manual Routing', 'Mixer [v2.0]', 'Sample/Track and Hold', and 'VRef [v1.60]'. Other categories like 'CapSense', 'Communications', 'Digital', 'Display', 'Filters', 'Ports and Pins', 'Power Supervision', and 'System' are also listed.

# Lab\_6 ADC+LCD



**Configure 'ADC\_DeISig'**

Name:

**Config1** | Config2 | Config3 | Config4 | Common | Built-in

Comment:

Configuration name:       ADC\_DeISig\_1\_CFG1

**Modes**

Conversion mode:

Resolution (bits):

Conversion rate (SPS):       Range: 2000 - 48000 SPS

Actual conv. rate (SPS):

Clock frequency (kHz):

**Input options - Differential mode**

Input range:

Buffer gain:

Buffer mode:

**Reference**

Reference:

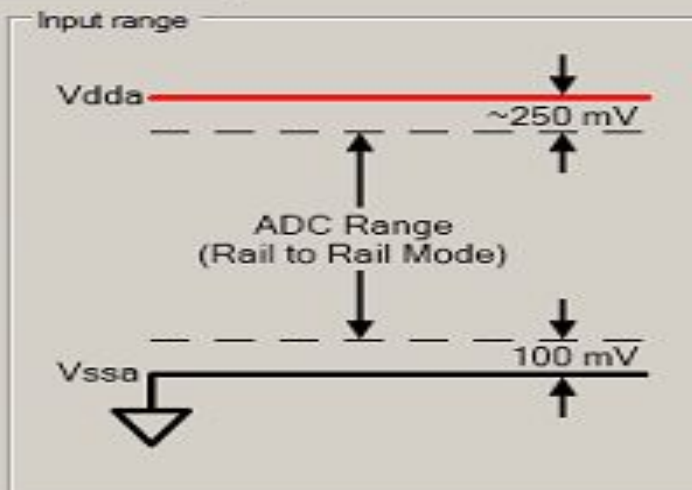
Vref (V):

**Alignment**

Right      Coherency = LOW

Left     

**Input range diagram:**



The diagram illustrates the input range of the ADC in Rail-to-Rail Mode. It shows two supply rails: V<sub>dda</sub> (top) and V<sub>ssa</sub> (bottom). A red horizontal line represents V<sub>dda</sub> and a black horizontal line represents V<sub>ssa</sub>. Two dashed horizontal lines represent the ADC's input range. The top dashed line is approximately 250 mV below V<sub>dda</sub>, and the bottom dashed line is approximately 100 mV above V<sub>ssa</sub>. A double-headed arrow between these dashed lines is labeled "ADC Range (Rail to Rail Mode)".

Buttons:

## Configure 'ADC\_DeISig'

Name: ADC

**Config1** Config2 Config3 Config4 Common Built-in

Comment: Default Config

Configuration name: CFG1 ADC\_CFG1

### Modes

Conversion mode: 2 - Continuous

Resolution (bits): 14

Conversion rate (SPS): 5000 Range: 2783 - 133565 SPS

Actual conv. rate (SPS): 5017

Clock frequency (kHz): 230.000

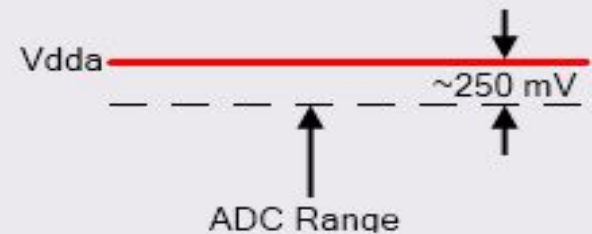
### Input options - Differential mode

Input range: +/-2.048V [ -Input +/- 2\*Vref ]

Buffer gain: 1

Buffer mode: Rail to Rail

### Input range



### Reference

Datasheet

OK

Apply

Cancel



Start Page | TopDesign.cysch | main.c | Design01.cydwr

### Configure 'ADC\_DeISig'

Name: ADC

Config1 | Config2 | Config3 | Config4 | Common | Built-in

Actual conv. rate (SPS): 5017  
 Clock frequency (kHz): 230.000

Input options - Differential mode

Input range: +/-2.048V ( -Input +/- 2\*Vref )  
 Buffer gain: 1  
 Buffer mode: Rail to Rail

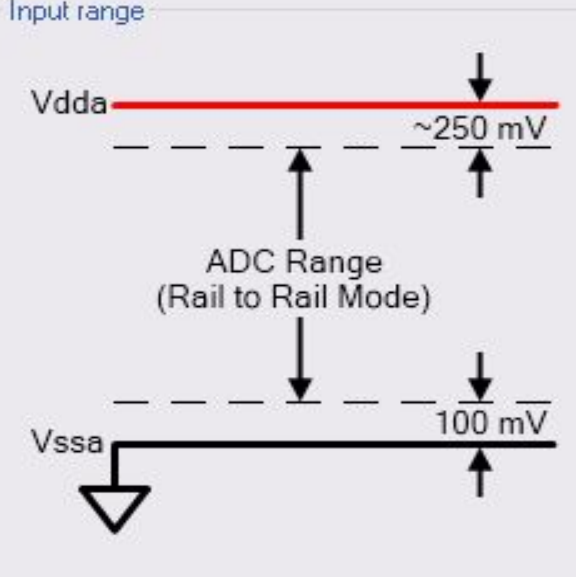
Reference

Reference: Internal 1.024 Volts  
 Vref (V): 1.024

Alignment

Right      Coherency = LOW  
 Left      16 bits (DVF Protected)

Input range diagram:



Vdda

~250 mV

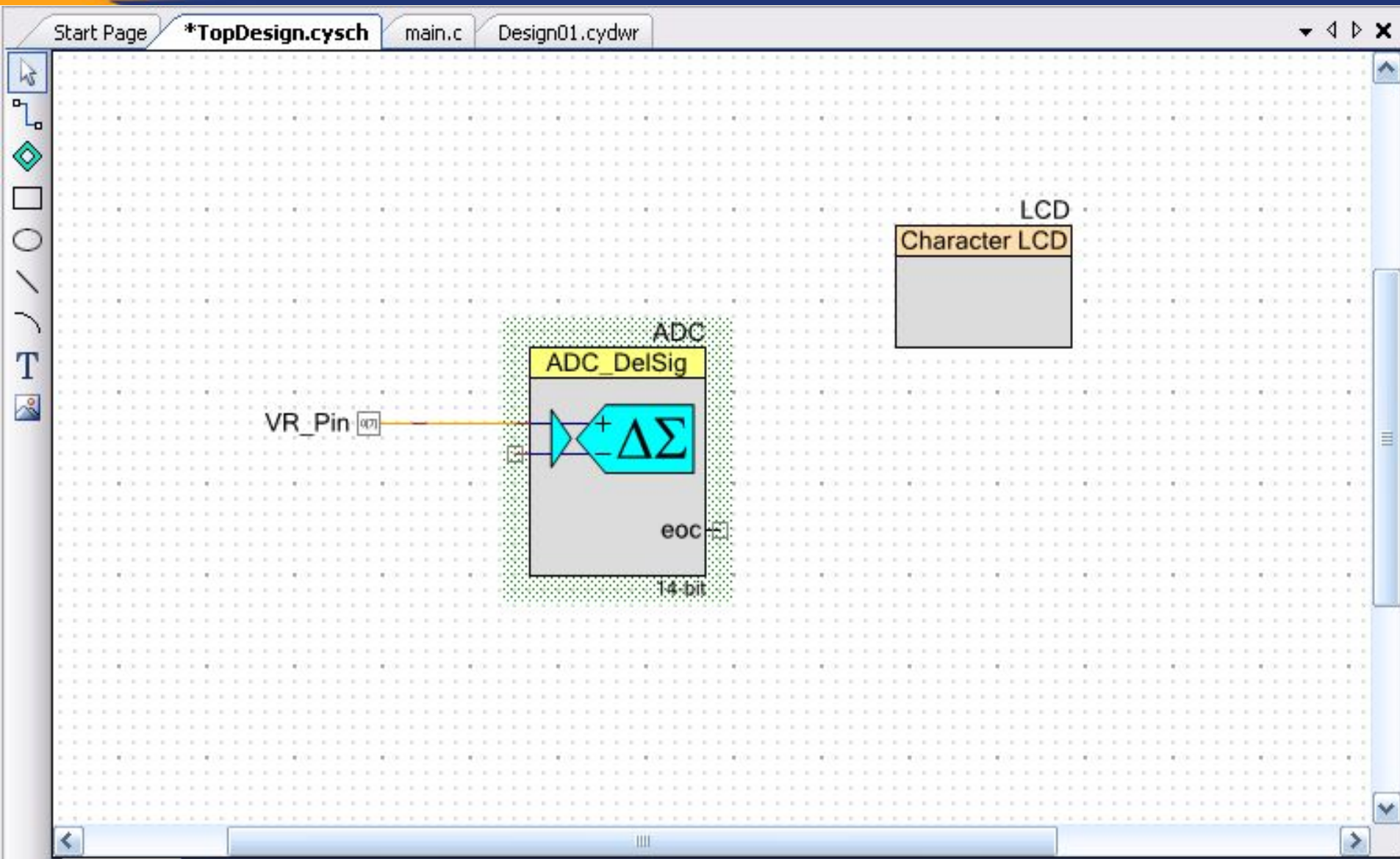
ADC Range (Rail to Rail Mode)

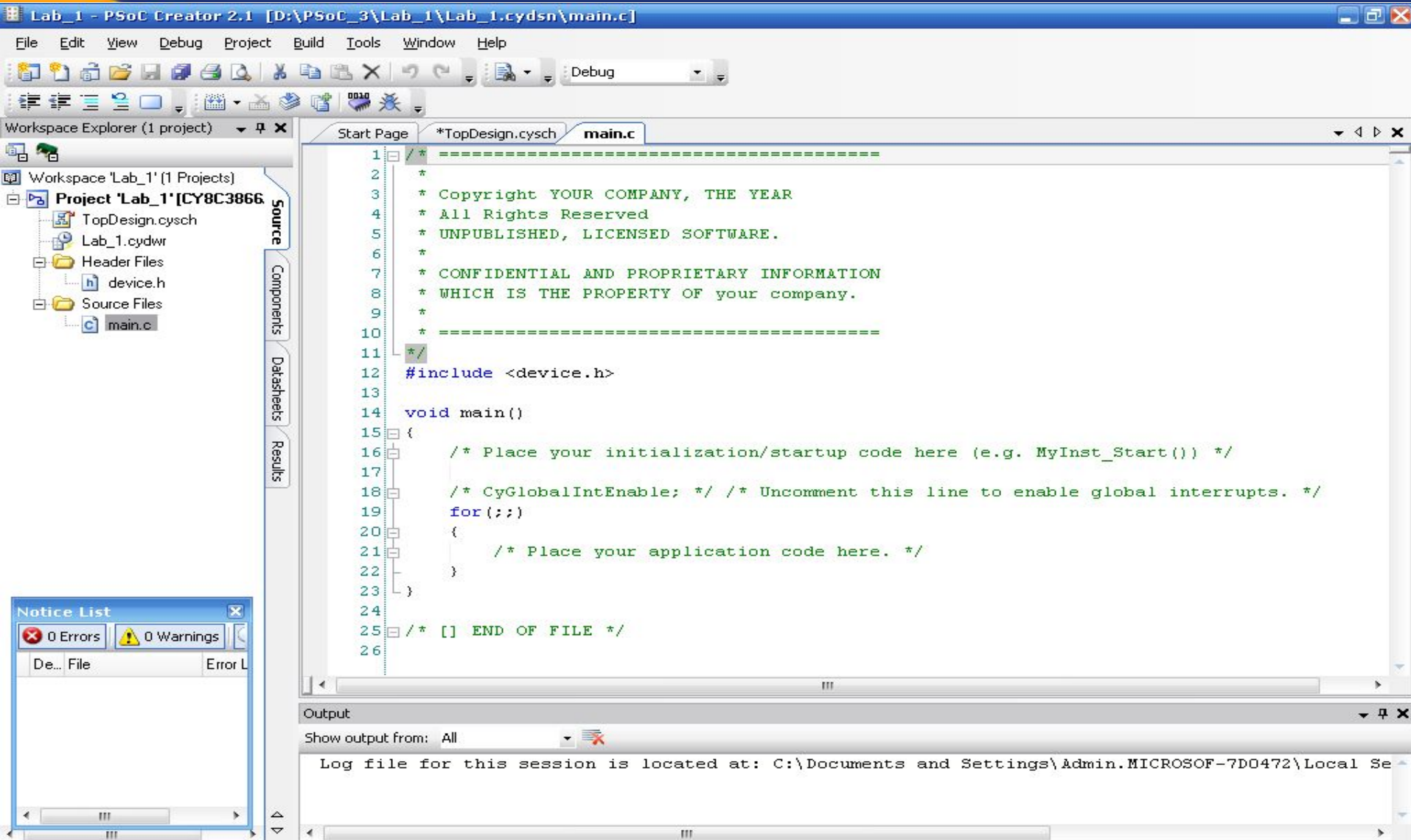
100 mV

Vssa

Datasheet | OK | Apply | Cancel

# Lab\_6 ADC+LCD





The screenshot displays the PSoC Creator 2.1 IDE interface. The main window shows the source code for `main.c` in the `*TopDesign.cysch` project. The code includes a copyright notice, a header file inclusion, and a `main()` function with several comments for initialization and application code.

```
1  /* -----  
2  *  
3  * Copyright YOUR COMPANY, THE YEAR  
4  * All Rights Reserved  
5  * UNPUBLISHED, LICENSED SOFTWARE.  
6  *  
7  * CONFIDENTIAL AND PROPRIETARY INFORMATION  
8  * WHICH IS THE PROPERTY OF your company.  
9  *  
10 * -----  
11 */  
12 #include <device.h>  
13  
14 void main()  
15 {  
16     /* Place your initialization/startup code here (e.g. MyInst_Start()) */  
17  
18     /* CyGlobalIntEnable; */ /* Uncomment this line to enable global interrupts. */  
19     for(;;)  
20     {  
21         /* Place your application code here. */  
22     }  
23 }  
24  
25 /* [] END OF FILE */  
26
```

The `Notice List` window is open in the bottom-left corner, showing 0 Errors and 0 Warnings. The `Output` window at the bottom shows the log file location: `C:\Documents and Settings\Admin.MICROSOFT-7D0472\Local Se...`

**Make the following changes to the beginning of *main.c*.**

```
#include "myADC.h"
```

```
.....
```

```
void main()
```

```
{
```

```
/* Components should be initialized in the following order:
```

```
* 1. interrupts
```

```
* 2. sources of interrupts (clocks are auto-initialized)
```

```
* 3. global interrupt enable
```

```
*/
```

```
InitAdc(); /* source of interrupt */
```

```
CYGlobalIntEnable /* macro */
```

```
/* Initialize other components, not associated with interrupts */
```

```
CharLCD_Start();
```

Create a file called *myADC.c*.

Add the following code to the *myADC.c* file.

```
#include <device.h>
#include "myADC.h"
/*****
* Global Functions
*****/
/*****
* Function Name: InitAdc()
*****/
void InitAdc(void)
{
ADC_Start();
ADC_StartConvert(); /* Starts a continuous conversion process */
} /* end of InitAdc() */
```



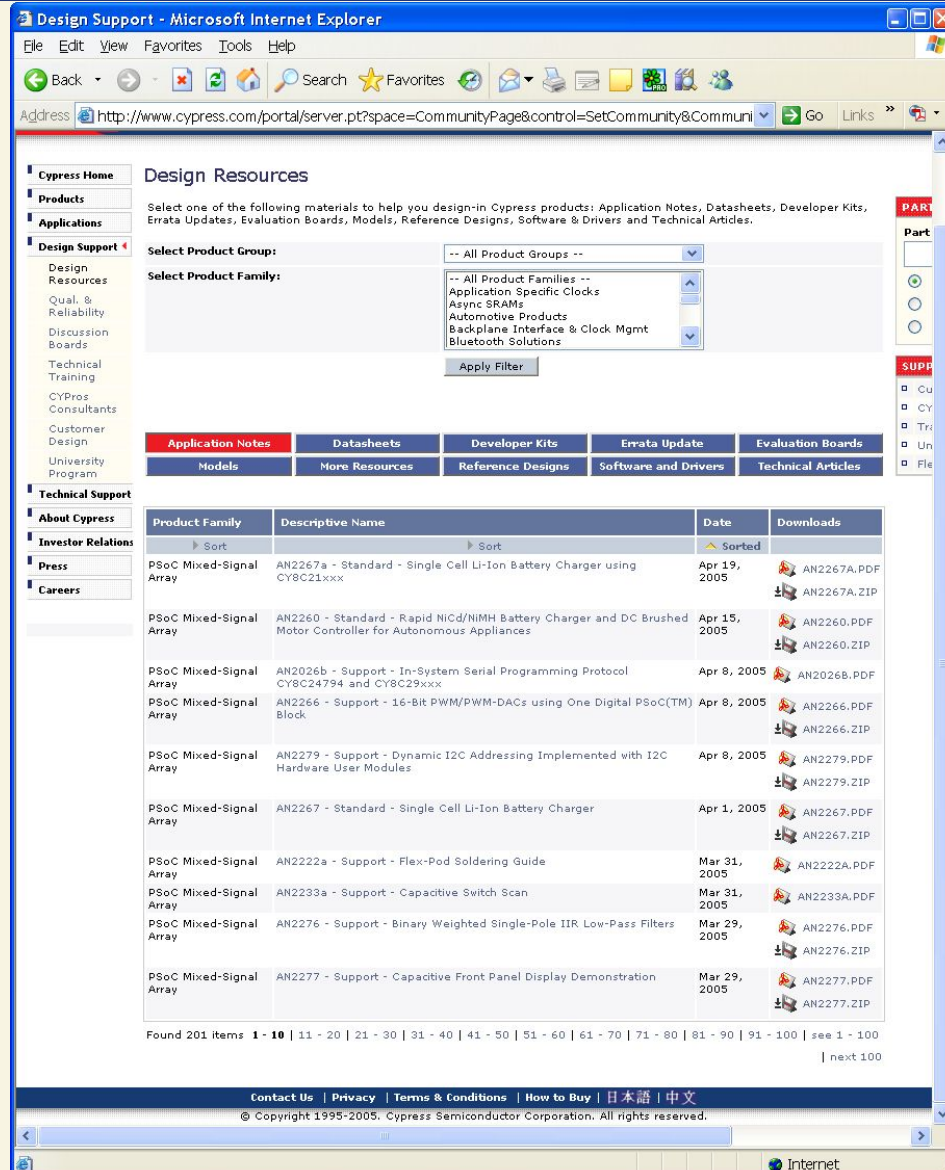
```
/* **** */
* Function Name: UpdateAdc()
* **** */
void UpdateAdc(void)
{
if(ADC_IsEndConversion(ADC_RETURN_STATUS))
{
uint8 adcval8;
/* Get 14-bit conversion reported in a signed 16-bit result, and limit
* negative and positive overflow. */
int16 adcval16 = ADC_GetResult16();
if(adcval16 < 0)
{
adcval16 = 0;
}
else if(adcval16 > 0x3FFF)
{
adcval16 = 0x3FFF;
}
else {} /* value is in range, do nothing */
```



# myADC.c

```
/* Convert to an 8-bit result; grab the 8 MS bits. */  
adcval8 = (uint8)(((uint16)adcval16 >> 6) & 0xFFU);  
if(source != 0U)  
{  
    adcval8 *= 3U;  
}  
/* display the result on the char LCD */  
CharLCD_Position(1U, 6U); /* row, column */  
CharLCD_PrintHexUint8(adcval8);  
* Print (val / 4) (with rounding, add half the divisor) 'X' characters,  
* which creates a horizontal line whose length is proportional to the  
* ADC value.  
*/  
adcval8 = (uint8)(((uint16)adcval8 + 2U) / 4U);  
if (adcval8 == 0U) /* make sure that at least one 'X' is printed */  
{  
    adcval8 = 1U;  
}  
} /* end of if (ADC_IsEndConversion(ADC_RETURN_STATUS)) */  
} /* end of UpdateAdc() */
```

На сайті фірми Cypress знаходиться більше **200** Application Notes і Reference Designs, які ілюструють області застосування мікроконтролерів PSoC.



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(лекція 6, кінець)  
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