



CYPRESS

# Мікропроцесорна техніка

(лекція 4)  
Благітко Б.Я.  
2019 р.

**PSoC Creator 4.2**  
**Designing with PSoC 3/5**



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# PSoC@3/5 Interrupts

**PSoC Creator 4.2**  
**Designing with PSoC 3/5**



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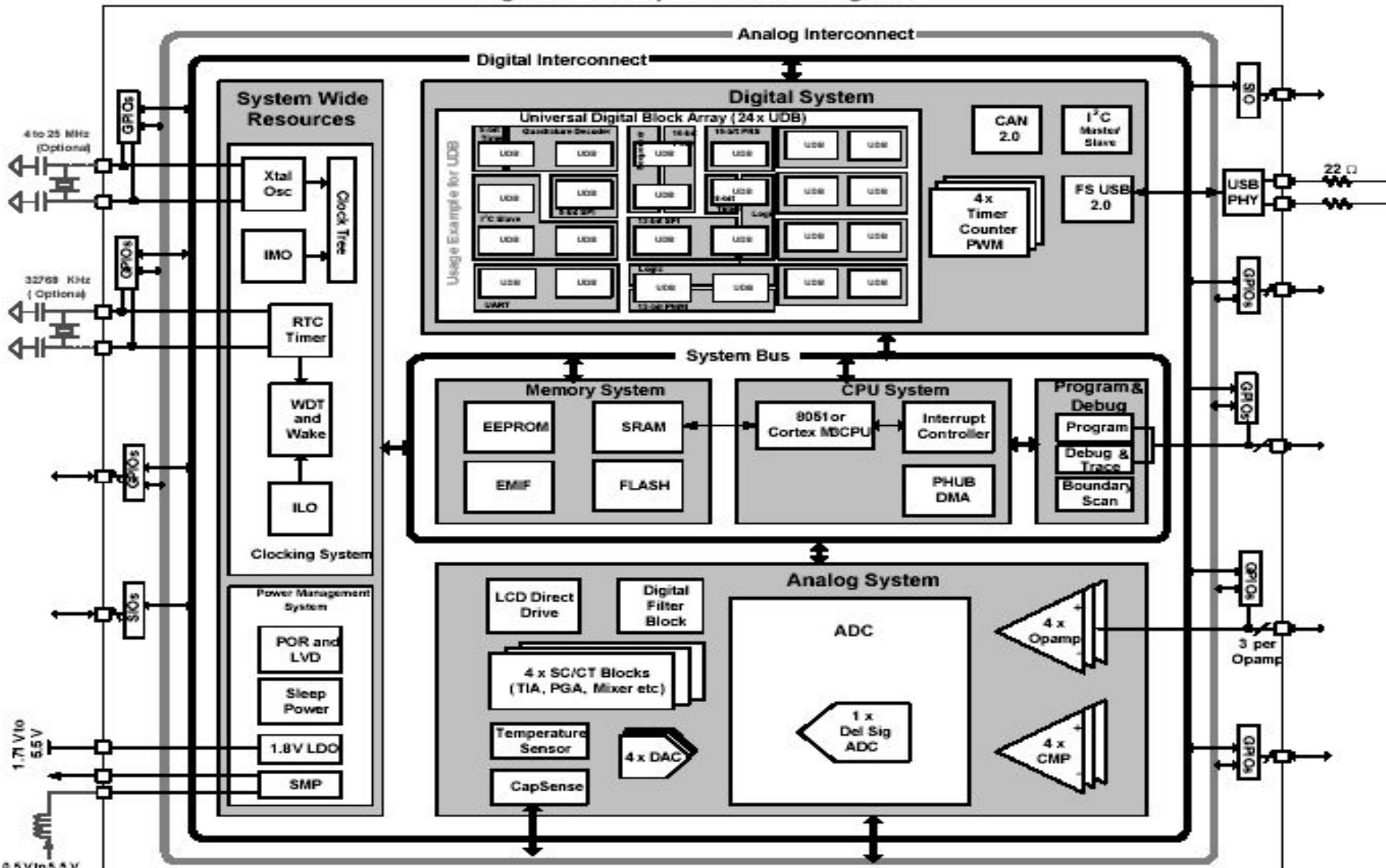
# Interrupts

## Project Objective

- Generate interrupt for rising edge signal on pin
- Set a Flag in Interrupt Service routine (ISR)
- Increment Count variable in main code if Flag is set
- Clear the Flag in main code

# Модулі PSoC@3/5

Figure 1-1. Simplified Block Diagram



# Цифрові модулі

Figure 7-3. Component Catalog

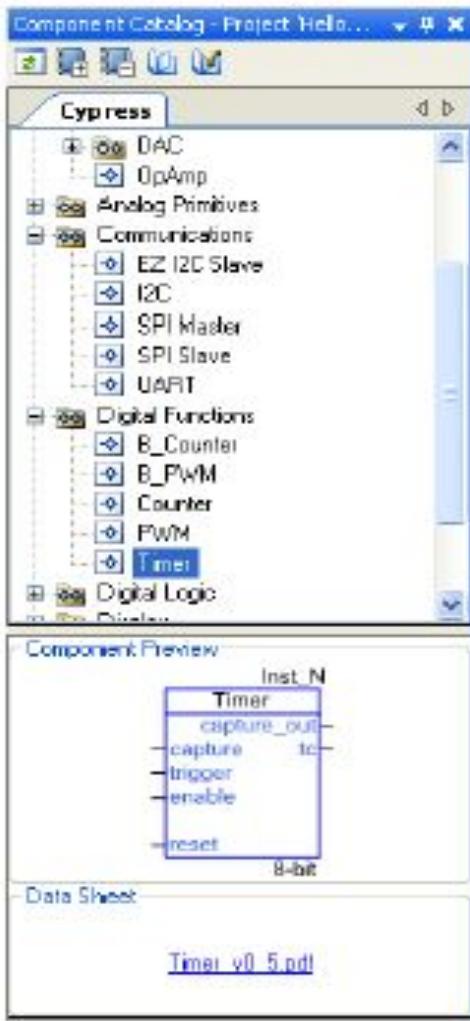
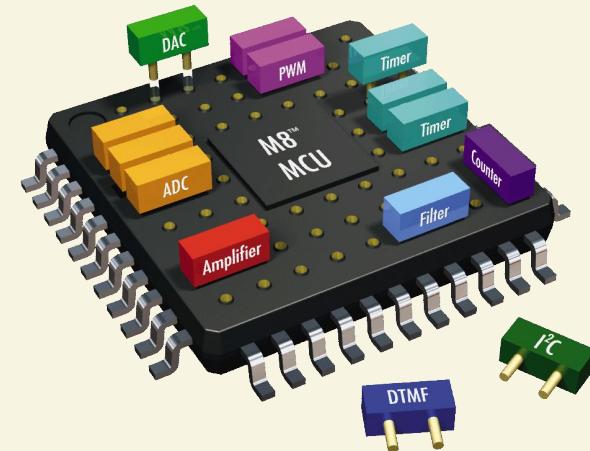
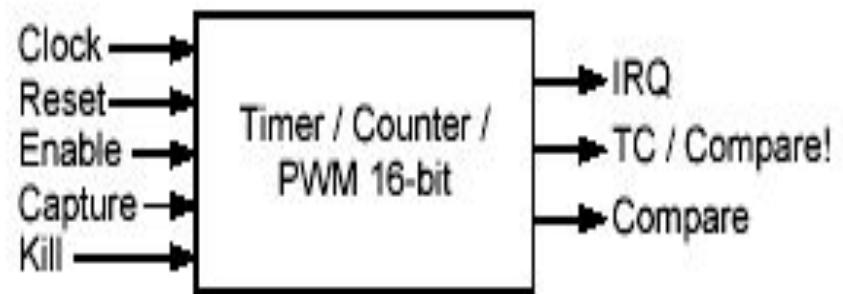


Figure 7-21. Timer/Counter/PWM





**PWMs, Timers** and **Counters** share many capabilities but each provides specific capabilities.

## When to Use a PWM

The most common use of the **PWM** is to generate periodic waveforms with adjustable duty cycles. The PWM also provides optimized features for power control, motor control, switching regulators and lighting control. The PWM can also be used as a clock divider by driving a clock into the clock input and using the terminal count or a PWM output as the divided clock output.

## When to Use a Counter

A **Counter** component is better used in situations that require the counting of a number of events but also provides rising edge capture input as well as a compare output.

## When to Use a Timer

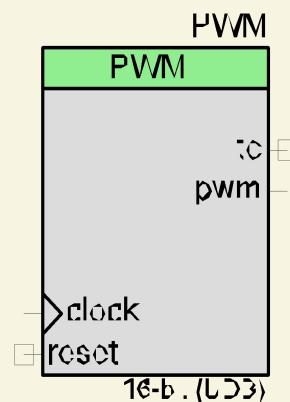
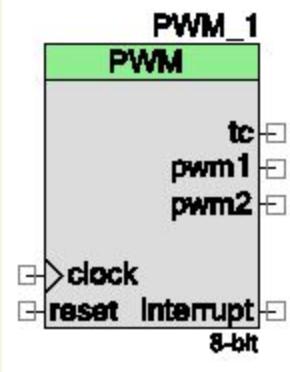
A **Timer** component is better used in situations focused on timing the length of events, measuring the interval of multiple rising and/or falling edges, or for multiple capture events.



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# PWM

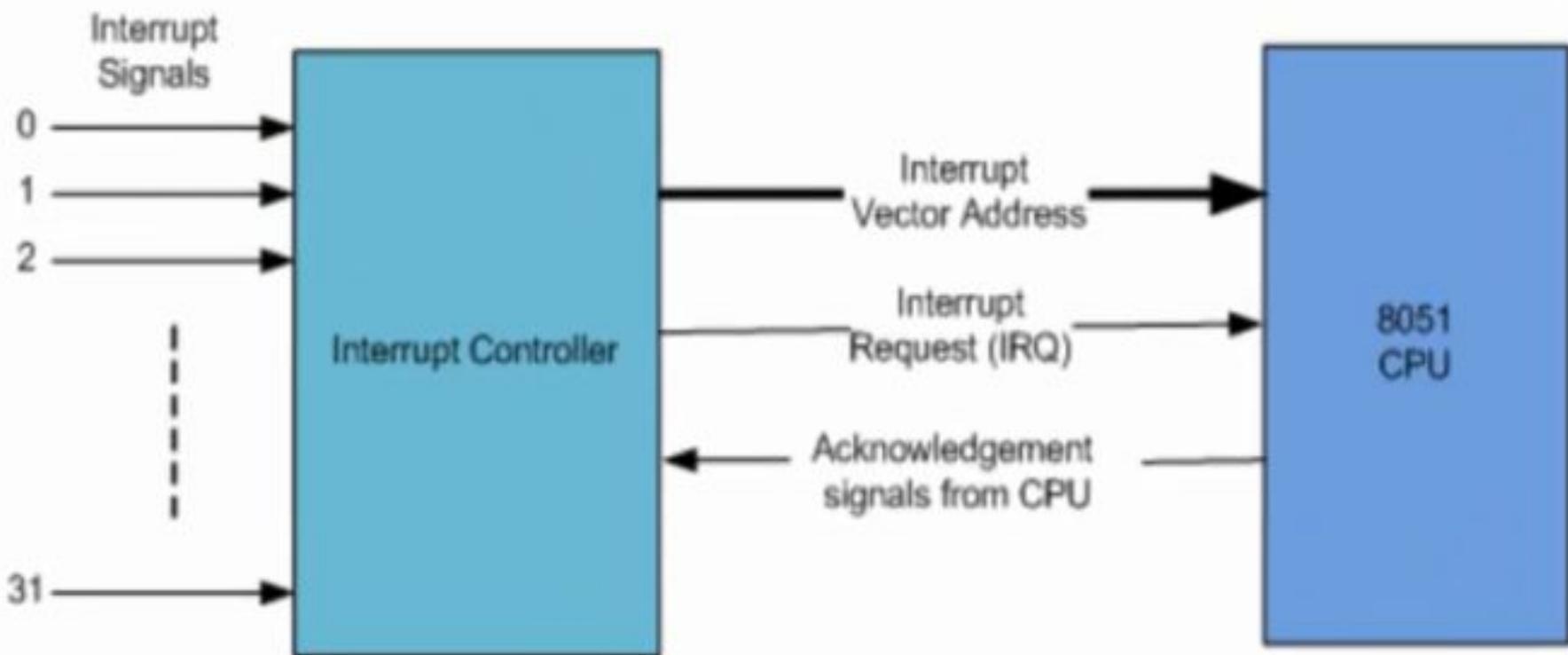
Output	May Be Hidden	Description
tc	N	The terminal count output is '1' when the period counter is equal to zero. In normal operation this output will be '1' for a single cycle where the counter is reloaded with period. If the PWM is stopped with the period counter equal to zero then this signal will remain high until the period counter is no longer zero. This output is synchronized to the block clock input of the component.
interrupt	Y	The interrupt output is the logical OR of the group of possible interrupt sources. This signal will go high while any of the enabled interrupt sources are true. The interrupt output shall remain asserted until the Status Register is read out by the software. In order to receive subsequent interrupts, the interrupt shall be cleared by reading the Status Register using the PWM_ReadStatusRegister() API. The interrupt output is not visible if the Use Interrupt parameter is not set. This allows the status register to be removed for resource optimization as necessary.
pwm/pwm1	Y	The pwm or pwm1 output is the first or only pulse width modulated output. This signal is defined by PWM Mode, compare modes(s), and compare value(s) as indicated in waveforms in the Configure dialog. When the instance is configured in one output, Dual Edged, Hardware Select, Center Aligned, or Dither PWM Modes, then the output "pwm" is visible. Otherwise the output "pwm1" is visible with "pwm2" the other pulse width signal. This output is synchronized to the block clock input of the component.





# Interrupts

## PSoC 3





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# Interrupts

Simple Interrupt - PSoC Creator 1.0 [C:\...\PSoC 3 Interrupts Training.cydsn\TopDesign\TopDesign.cysch]

File Edit View Debug Project Build Tools Window Help

Debug DP8051 Keil 8.16 91%

Workspace Explorer (1 project) Start Page \*TopDesign.cysch Component Catalog (140 components)

Project 'PSoC 3 Interrupts Tr' TopDesign.cysch PSoC 3 Interrupts Training.cy Header Files device.h Source Files main.c Generated\_Source

Components Results

### Interrupt Component in PSoC Creator

iar\_1

iar\_2

Cypress

- Cypress Component Catalog
  - Analog
  - Analog Primitives
  - CapSense
  - Communications
  - Deprecated
  - Digital
  - Display
  - Filters
  - Fixed Function
  - Ports and Pins
  - Primitive
  - System
    - Boost Converter [v1.50]
    - Clock [v1.50]
    - cy\_boot [v2.20]
    - Die Temperature [v1.50]
    - DMA [v1.50]
    - EEPROM [v1.50]
    - EMIF Port
    - Global Signal Ref
    - Interrupt [v1.50]
    - RTC [v1.60]
    - SleepTimer [v1.60]
    - SleepTimer [v1.60][2]
    - Sync
    - UDBClkEn

Component Preview

Inst\_N

Data Sheet

cv\_ir\_v1.50.pdf

Provides a mechanism to associate a hardware/software event with the interrupt Controller

Introduction PSoC 3 Interrupts Interrupt Component Interrupt Source selection Interrupt Type Interrupt Sources- Example 1 Interrupt Sources- Example 2

Output Output



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# Interrupts

Start Page \*TopDesign.cysch Proba\_3.cydwr main.c

Component Catalog (200 compon...)

Search for...

Cypress Off-Chip

- + Display
- + Filters
- + Ports and Pins
- + Power Supervision
- System
  - Boost Converter [v5.0]
  - Bootloadable [v1.20]
  - Bootloader [v1.20]
  - Clock [v2.20]
  - Die Temperature [v2.0]
  - DMA [v1.70]
  - EEPROM [v2.10]
  - Emulated EEPROM [v1.10]
  - External Memory Interface
  - Global Signal Reference [v2.0]
  - ILO Trim [v1.10]
  - Interrupt [v1.70]
  - RTC [v2.0]
  - SleepTimer [v3.20]
  - Thermal Management

11



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# Interrupts

Start Page

\*TopDesign.cysch

Proba\_3.cydwr

main.c

▼ ◀ ▶ ×

Configure 'cy\_isr'

Name: isr\_1

Basic Built-in

Parameter	Value
InterruptType	DERIVED

Parameter Information

Datasheet OK Apply Cancel

The screenshot shows the Cypress PSoC Designer interface. A central dialog box titled "Configure 'cy\_isr'" is open. Inside, the "Name" field contains "isr\_1". Below it, there are two tabs: "Basic" (which is selected) and "Built-in". A table lists a single parameter, "InterruptType", with the value "DERIVED". At the bottom of the dialog, there's a section labeled "Parameter Information" which is currently empty. Along the bottom edge of the dialog are four buttons: "Datasheet" (highlighted in green), "OK", "Apply", and "Cancel". To the left of the dialog, a vertical toolbar displays icons for various tools: a cursor, a line, a diamond, a square, a circle, a diagonal line, a text tool, and a photo tool. The main workspace area to the right of the dialog is a grid-based workspace.



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# Interrupts

Start Page

\*TopDesign.cysch

Proba\_3.cydwr

main.c

▼ ◀ ▶ X

Configure 'cy\_isr'

Name: isr\_1

Basic Built-in

Parameter	Value
InterruptType	RISING_EDGE

Parameter Information

**InterruptType:** DERIVED - infers the interrupt type based on the signal source.

RISING\_EDGE - selects the source connection to the ISR component as a rising edge connection via the DSI.

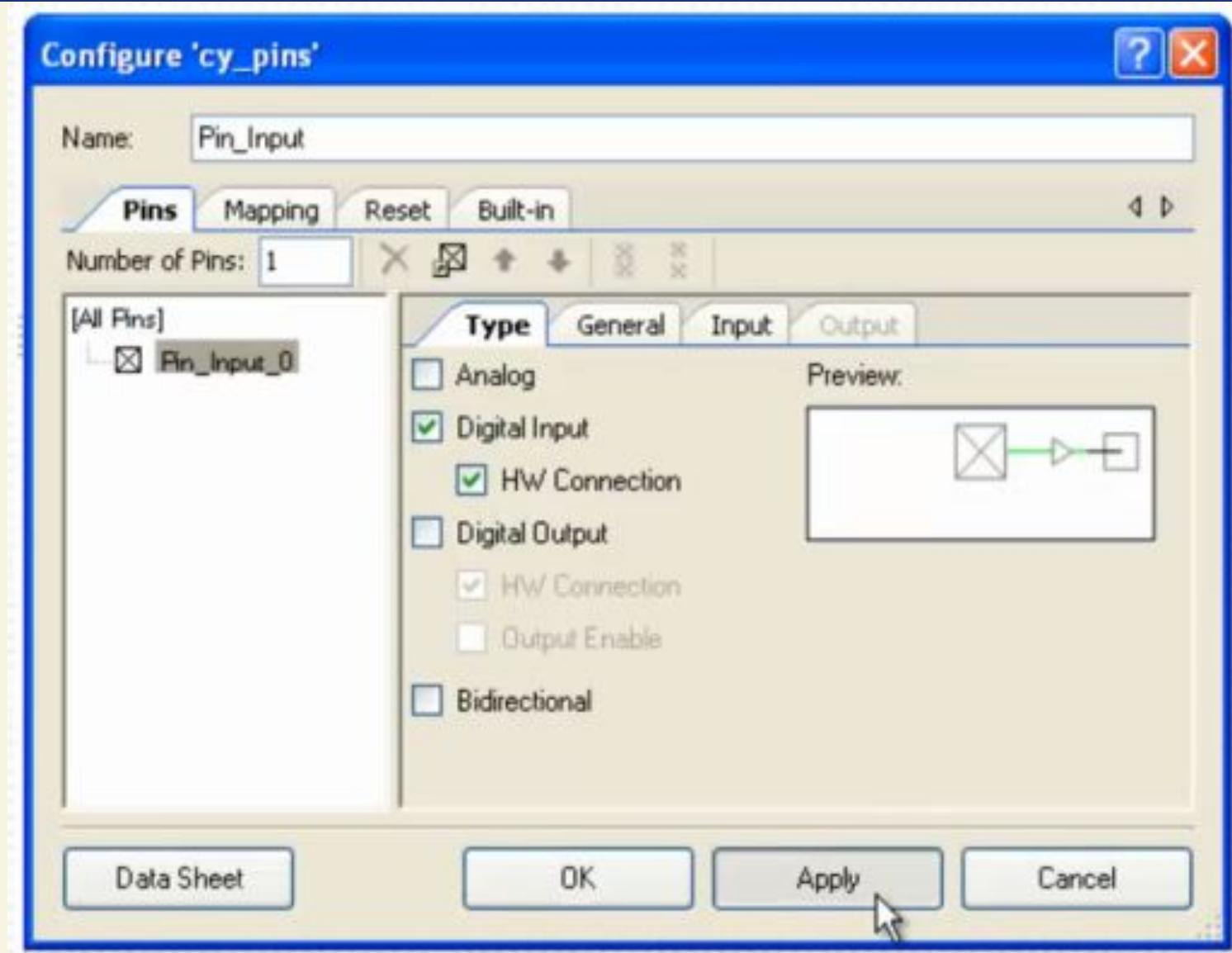
Datasheet OK Apply Cancel

13



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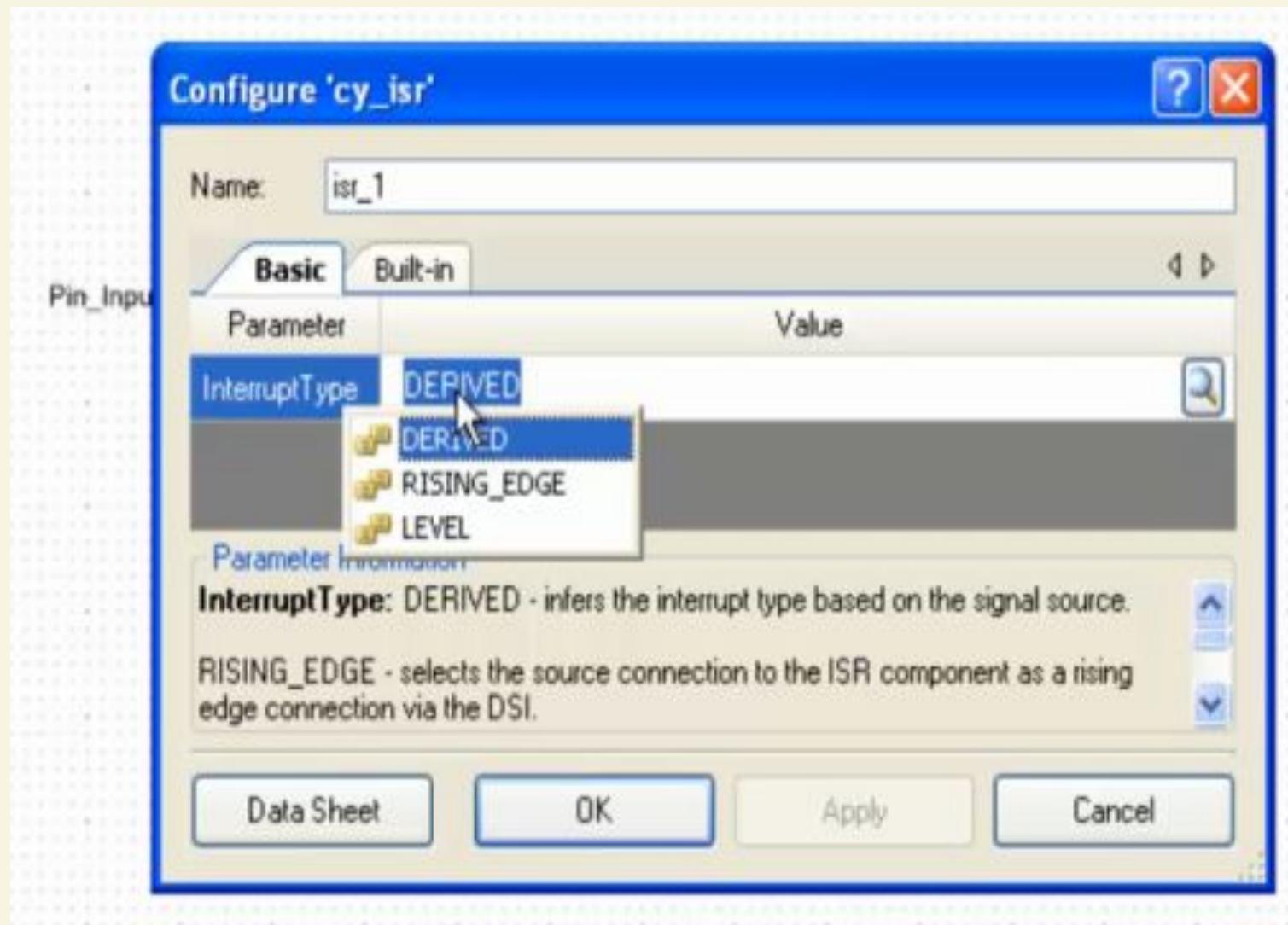
# Interrupts





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# Interrupts





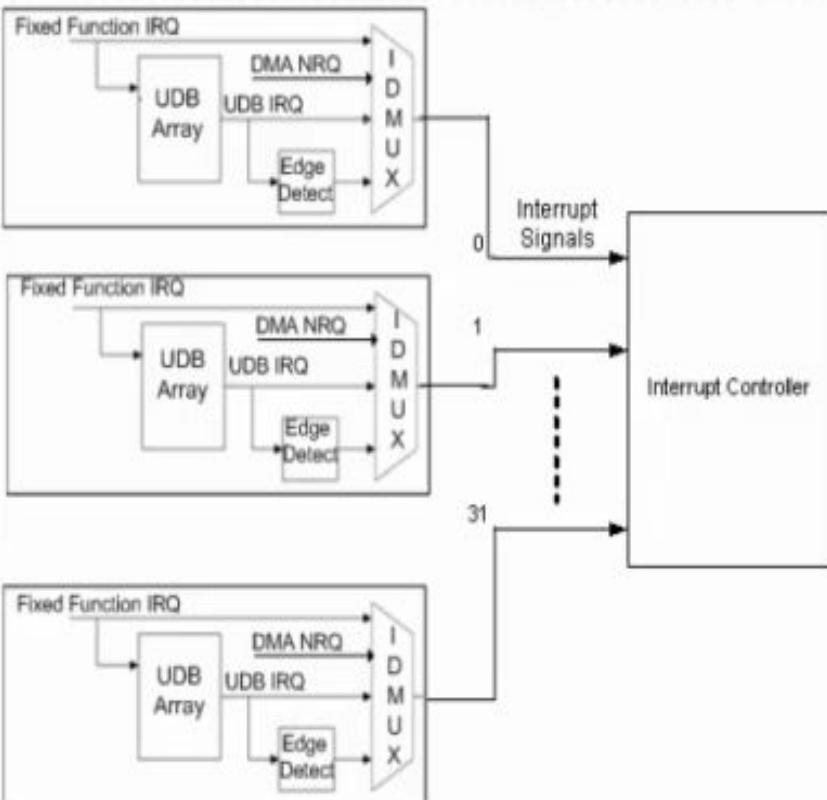
CYPRESS

# Interrupts



# Interrupts

## Interrupt Sources



Interrupt Request Source (IRQ) Type	Examples
Fixed function IRQ's	ADC End of Conversion (EoC), Fixed Function Timer, Counter Interrupts, Port Interrupt Control Unit (PICU), Sleep Timer, Low Voltage Detect (LVD)
Universal Digital Block (UDB) array IRQ's	Any digital output signal on chip, UART, SPI component interrupts, UDB based Timer, Counter, PWM interrupts, Fixed function IRQ's can also be UDB IRQ's
Direct Memory Access (DMA) NRQ's	DMA channel Transfer complete (NRQ) signals

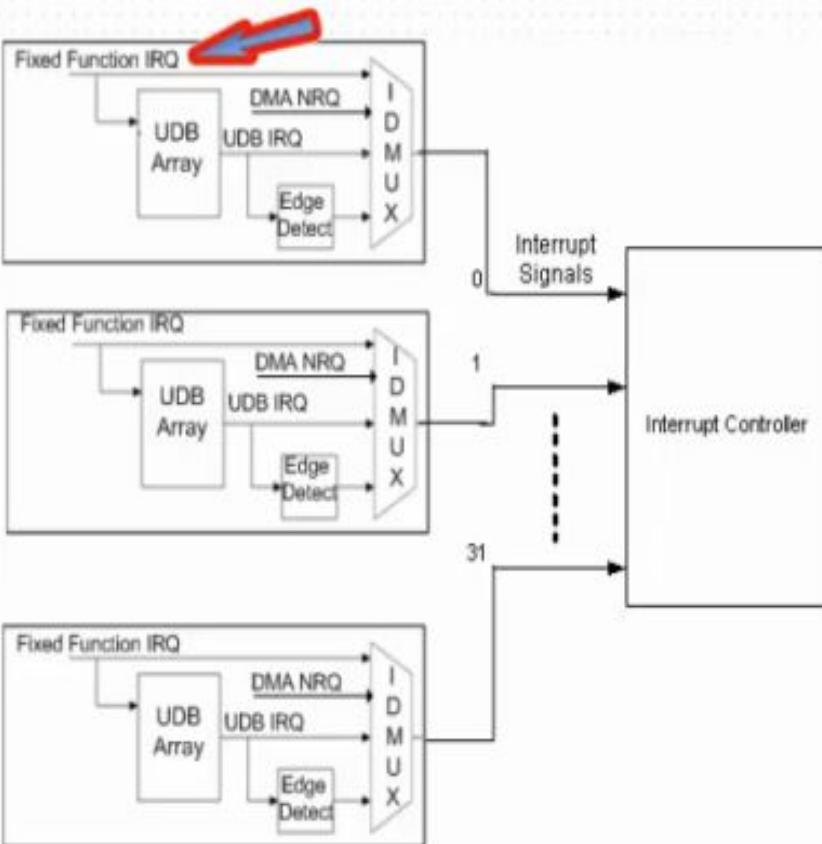




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# Interrupts

## Interrupt Sources



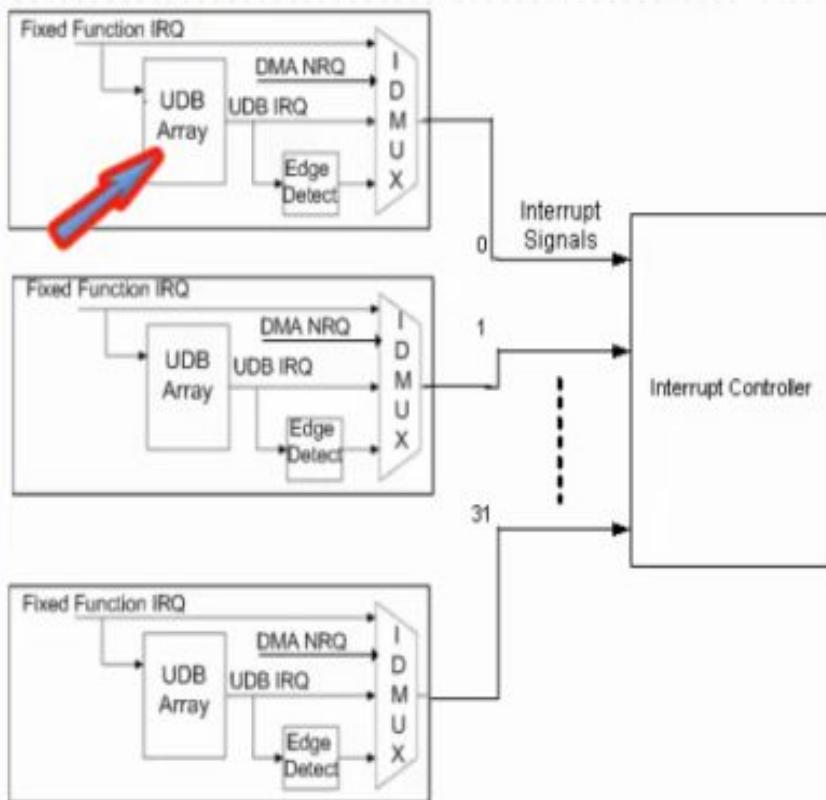
Interrupt Request Source (IRQ) Type	Examples
Fixed function IRQ's	ADC End of Conversion (EoC), Fixed Function Timer, Counter Interrupts, Port Interrupt Control Unit (PICU), Sleep Timer, Low Voltage Detect (LVD)
Universal Digital Block (UDB) array IRQ's	Any digital output signal on chip, UART, SPI component interrupts, UDB based Timer, Counter, PWM interrupts, Fixed function IRQ's can also be UDB IRQ's
Direct Memory Access (DMA) NRQ's	DMA channel Transfer complete (NRQ) signals





# Interrupts

## Interrupt Sources

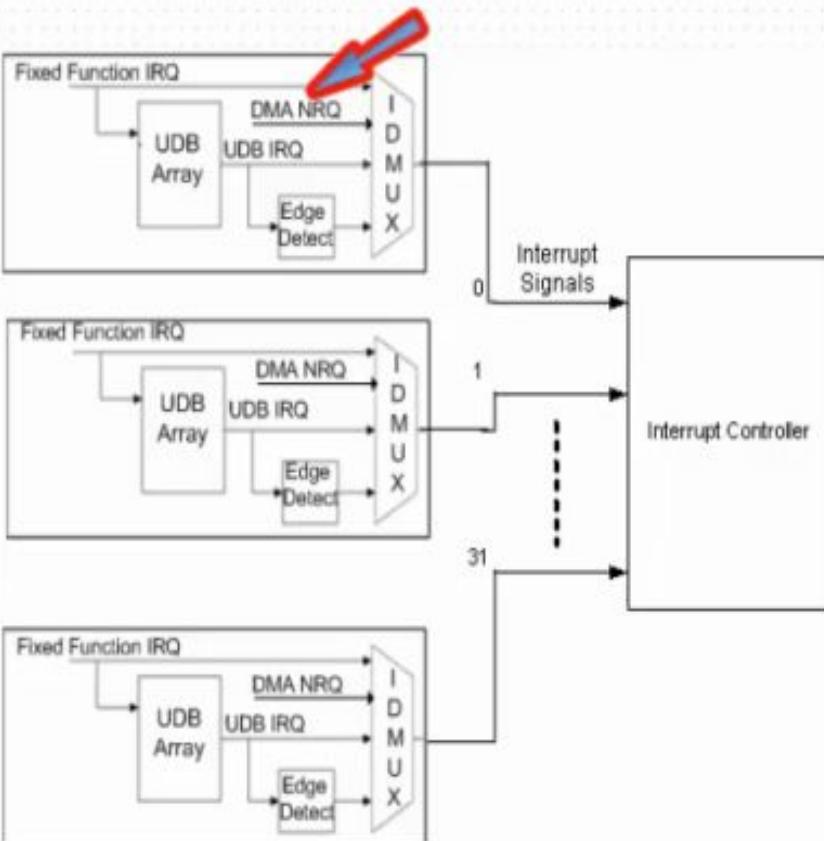


Interrupt Request Source (IRQ) Type	Examples
Fixed function IRQ's	ADC End of Conversion (EoC), Fixed Function Timer, Counter Interrupts, Port Interrupt Control Unit (PICU), Sleep Timer, Low Voltage Detect (LVD)
Universal Digital Block (UDB) array IRQ's	Any digital output signal on chip, UART, SPI component interrupts, UDB based Timer, Counter, PWM interrupts, Fixed function IRQ's can also be UDB IRQ's
Direct Memory Access (DMA) NRQ's	DMA channel Transfer complete (NRQ) signals



# Interrupts

## Interrupt Sources



Interrupt Request Source (IRQ) Type	Examples
Fixed function IRQ's	ADC End of Conversion (EoC), Fixed Function Timer, Counter Interrupts, Port Interrupt Control Unit (PICU), Sleep Timer, Low Voltage Detect (LVD)
Universal Digital Block (UDB) array IRQ's	Any digital output signal on chip, UART, SPI component interrupts, UDB based Timer, Counter, PWM interrupts, Fixed function IRQ's can also be UDB IRQ's
Direct Memory Access (DMA) NRQ's	DMA channel Transfer complete (NRQ) signals





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# Interrupts

## Interrupt Type selection

Configure 'cy\_isr'

Name: isr\_1

Basic Built-in

Parameter	Value
InterruptType	DERIVED
	DERIVED
	RISING_EDGE
	LEVEL

Parameter Information

**InterruptType:** DERIVED - infers the interrupt type based on the signal source.

RISING\_EDGE - selects the source connection to the ISR component as a rising edge connection via the DSI.

LEVEL - selects the source connected to the ISR component as a level sensitive connection via the DSI.

**Value:** DERIVED  
**Type:** IntTypeEnum

Data Sheet OK Apply Cancel

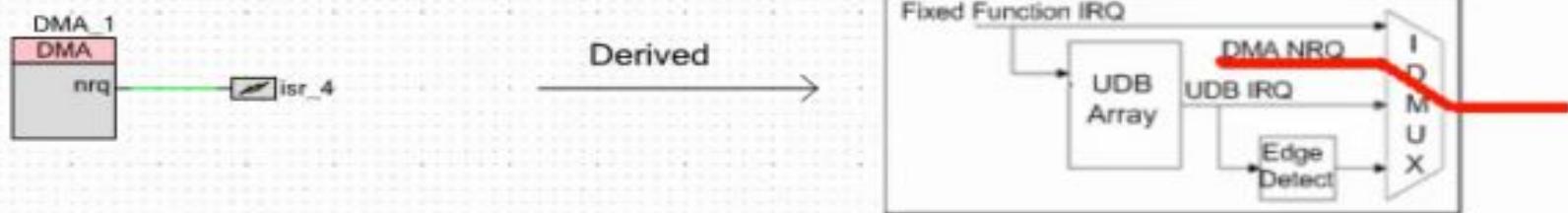


# Interrupts

## Interrupt Sources

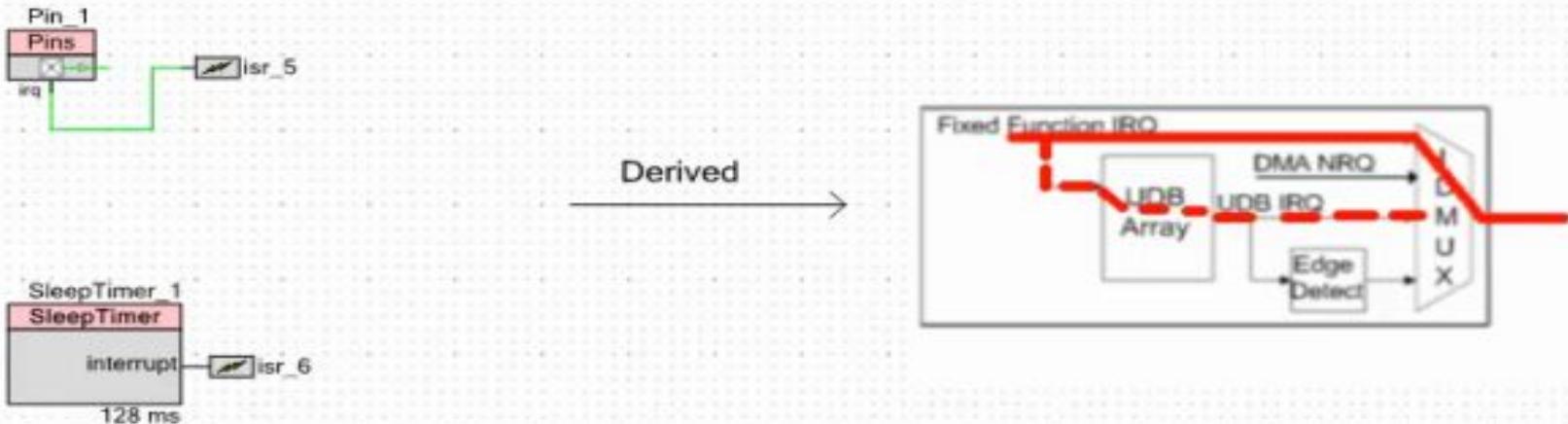
1.)

### DMA nrq Interrupt



2.)

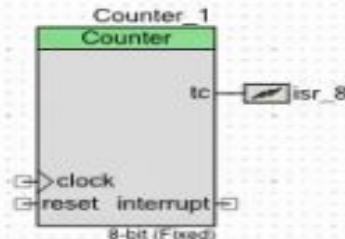
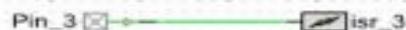
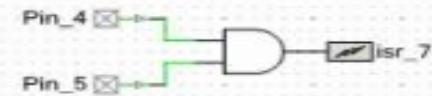
### Fixed Function Interrupts



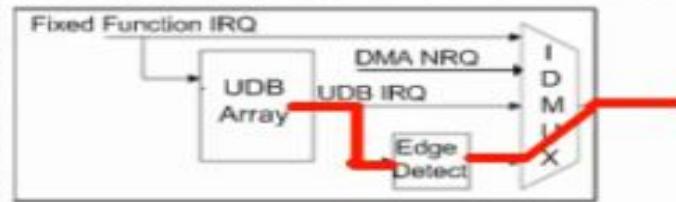


# Interrupts

## 3.) Edge Triggered Interrupts



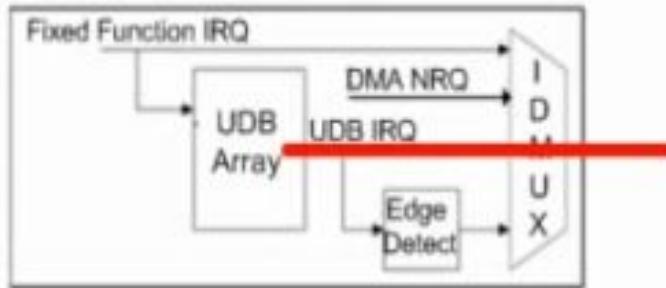
Derived  
(or)  
Rising Edge →



## 4.) Level Interrupt



Level →





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# Creator

PSoC Creator 2.1

File Edit View Debug Project Build Tools Window Help

Workspace Explorer

Source Components Datasheets Results

Notice List  
0 Errors 0 Warnings Error L  
De... File Error L

Start Page

## PSoC® Creator™

Recent Projects

- HelloWorld\_Blinky01.cywrk
- CapSense\_CSD\_Design01...
- CapSense\_CSD\_Design01...
- CharLCD\_CustomFont01.c...
- CharLCD\_CustomFont01.c...

Create New Project...  
Open Existing Project...

Getting Started

- PSoC Creator Start Page
- Quick Start Guide
- Intro to PSoC
- Intro to PSoC Creator
- PSoC Creator Training
- Help Tutorials
- Getting Started With PSoC 3
- Getting Started With PSoC 5

Examples and Kits

- Find Example Project...
- No Kit Packages Installed

Output  
Show output from: All

Log file for this session is located at: C:\Documents and Settings\Admin.MICROSOFT\Local Se

简体中文 日本語 한국어 English

### PSoC Creator News and Information

[Happy Lunar New Year!](#)  
Posted on 02/11/2013

Gong Xi Fa Cai! As many of my friends and colleagues are celebrating the New Year and welcoming in the year of the water snake, I wanted to take a minute and wish you all well. May the New Year bring each of you prosperity, good luck and a new PSoC design.

[Read More](#)

[Tips + Tricks: Menu Customization](#)  
Posted on 01/24/2013

Did you know you can create a customized menu in PSoC® Creator? Right click in a blank area of the top menu and select customize from the

Help  
5% Debug  
x u e = ▲ ▼





# File – New - Projekt

PSoC Creator 2.1

File Edit View Debug Project Build Tools Window Help

Workspace Explorer

New Project

Design Other

Empty Templates

- Empty PSoC 3 Design
- Empty PSoC 5 Design
- Empty PSoC 5LP Design

PSoC 3 Starter Designs

- ADC\_DMA\_VDAC
- DelSig\_16Channel
- DelSig\_I2CM
- DelSig\_I2CS
- DelSig\_SPIM
- Filter\_ADC\_VDAC
- HW Fan Control with Alert

PSoC 5 Starter Designs

- ADC\_DMA\_VDAC
- DelSig\_I2CM
- DelSig\_I2CS

Creates a PSoC 3, 8 bit, design project.

Name: Lab\_1

Location: D:\PSoC\_3

Advanced

OK Cancel

Notice List

0 Errors 0 Warnings 0 Notes

De... File

0472\Local Se...

Ready

Новости Украины | ...

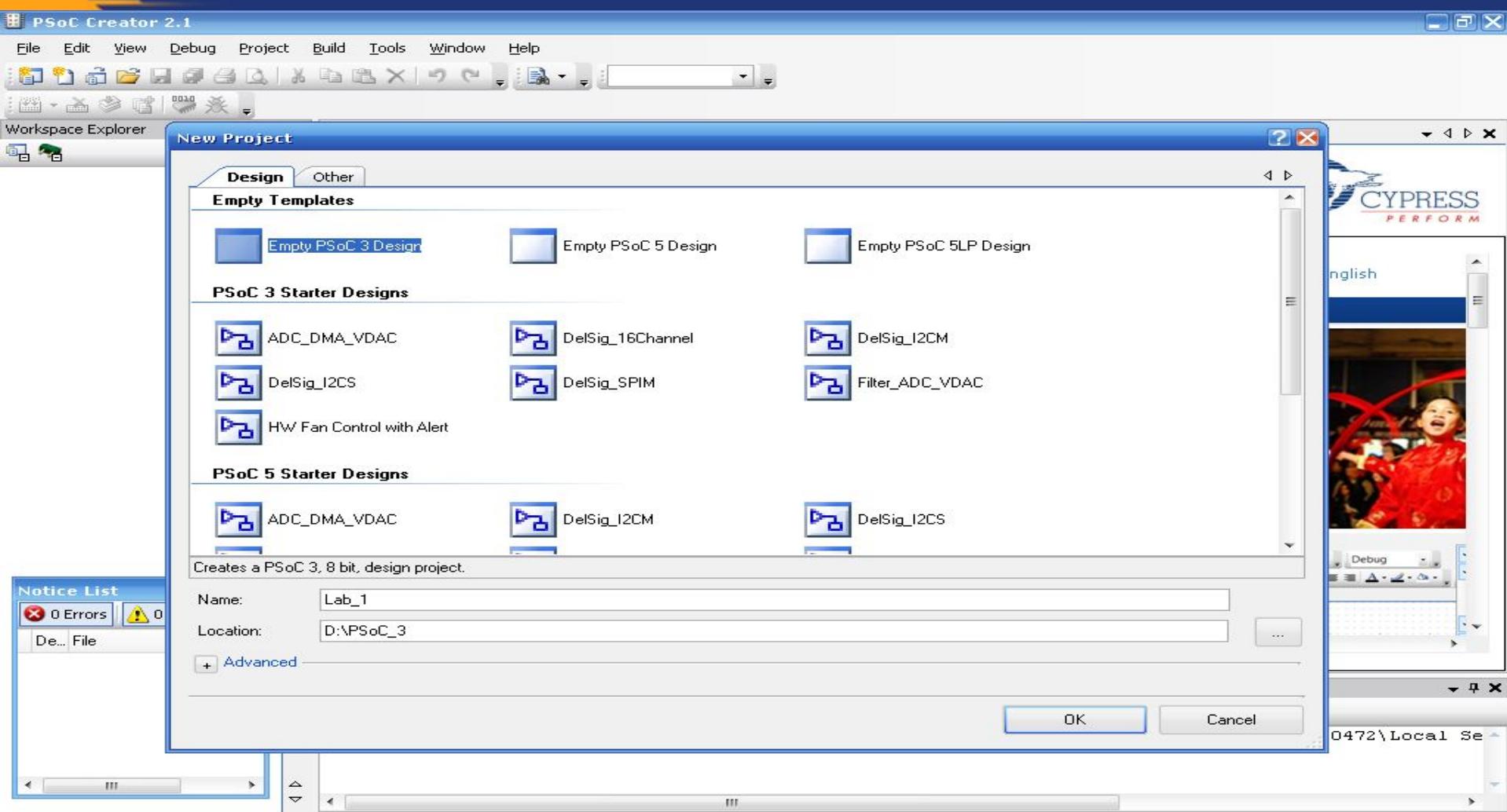
Документ1 - Microsoft...

PSoC Creator 2.1

EN 19:02



# Empty PSoC 3 Design





# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\A\_MyFirstInterruptProject.cydsn\TopDesign\TopDesig...]

File Edit View Debug Project Build Tools Window Help

Microsoft Sans Serif 10 B I U Debug

Workspace Explorer Start Page A\_MyFirstInte...tProject.cydw TopDesign.cysch main.c isr\_1.c Component Catalog...

Source Components Datasheets Results

timer\_clock 1 kHz

0

reset

Character LCD

LCD

Timer\_1

Timer

tc

interrupt

LED1

Notice List

0 Errors 0 Warnings

Output

Show output from: All

Protecting...

Verify Checksum...

Device 'PSoC 3 CY8C3866AX\*-040' was successfully programmed at 03/18/2013

Component Catalog Concept Cypress

- PrISM [v2.10]
- PRS [v2.10]
- PWM [v2.20]
- Quadrature De
- Shift Register
- Timer [v2.30]
- Logic
- Registers
  - Control Registr
  - Status Registr
- Display
  - Character LCD [v1]
  - Graphic LCD 8-bit
  - Graphic LCD 16-b
  - Graphic LCD Cont
  - Graphic LCD Cont
  - Graphic LCD Para
  - ResistiveTouch [v
  - Segment LCD - St
  - Segment LCD [v3.

Filters

Component Preview Inst N Character LCD

Datasheet

Character LCD Component

Ready 0 Errors 0 Warnings 2 Notes



# Configure LCD

Lab\_1 - PSoC Creator 2.1 [D:\PSoC\_3\Lab\_1\Lab\_1.cydsn\TopDesign\TopDesign.cysch]

File Edit View Debug Project Build Tools Window Help

Microsoft Sans Serif 10

Workspace Explorer (1 project)

Project 'Lab\_1' [CY8C3866]

- TopDesign.cysch
- Lab\_1.cydwr
- Header Files
- device.h
- Source Files
- main.c

Source Components Datasheets Results

Configure 'CharLCD'

Name: LCD\_Char

General Built-in

Parameters

LCD Custom Character Set

- None
- Vertical Bargraph
- Horizontal Bargraph
- User Defined

Include ASCII to Number Conversion Routines

Datasheet OK Apply Cancel

Custom Character Editor

Notice List

0 Errors 0 Warnings

Page 1

Output

Show output from: All

Log file for this session is located at: C:\Documents and Settings\Admin

Component Catalog (174 co...)

Cypress Component Catalog

- Analog
  - ADC
  - Amplifiers
  - Analog MUX
  - Comparator [v1.90]
  - DAC
- Manual Routing
  - Mixer [v1.91]
  - Sample/Track and Hold
  - VRef [v1.60]
- CapSense
- Communications
- Digital
- Display
  - Character LCD [v1.70]
  - Graphic LCD 8-bit Parallel
  - Graphic LCD 16-bit Parallel
  - Graphic LCD Controller I
  - Graphic LCD Controller II
  - Graphic LCD Parallel Interface
  - ResistiveTouch [v1.10]

Component Preview

Inst\_N Character LCD

Datasheet

(X=295, Y=131)

0 Errors 0 Warnings 0 Notes



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# Main.c

Lab\_1 - PSoC Creator 2.1 [D:\PSoC\_3\Lab\_1\Lab\_1.cydsn\main.c]

File Edit View Debug Project Build Tools Window Help

Debug

Workspace Explorer (1 project) X

Project 'Lab\_1' [CY8C3866]

- TopDesign.cysch
- Lab\_1.cydwr
- Header Files
  - device.h
- Source Files
  - main.c

Source Components Datasheets Results

Start Page \*TopDesign.cysch main.c

```
1 /* ===== */
2 *
3 * Copyright YOUR COMPANY, THE YEAR
4 * All Rights Reserved
5 * UNPUBLISHED, LICENSED SOFTWARE.
6 *
7 * CONFIDENTIAL AND PROPRIETARY INFORMATION
8 * WHICH IS THE PROPERTY OF your company.
9 *
10 * =====
11 */
12 #include <device.h>
13
14 void main()
15 {
16     /* Place your initialization/startup code here (e.g. MyInst_Start()) */
17
18     /* CyGlobalIntEnable; */ /* Uncomment this line to enable global interrupts. */
19     for(;;)
20     {
21         /* Place your application code here. */
22     }
23 }
24
25 /* [] END OF FILE */
```

Notice List X

0 Errors 0 Warnings

De... File Error L

Output

Show output from: All X

Log file for this session is located at: C:\Documents and Settings\Admin.MICROSOFT\Local Se

Ready

Ln 1 Col 1 INS 0 Errors 0 Warnings 0 Notes



# Lab\_4.cywr

Lab\_1 - PSoC Creator 2.1 [D:\PSoC\_3\Lab\_1\Lab\_1.cydsn\Lab\_1.cydwr]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer (1 project) Start Page TopDesign.cysch main.c Lab\_1.cydwr

Project 'Lab\_1' [CY8C3866] Source Components Datasheets Results

Notice List 0 Errors 0 Warnings

Pins Analog Clocks Interrupts DMA System Directives Flash Security

Output Show output from: All Log file for this session is located at: C:\Documents and Settings\Admin.MICROSOFT\Local Se

Alias Name Port Pin Lock

\LCD_Char:LCDPort[6:0]\	PO[6:0] IDAC:H		
	PO[7:1] IDAC:H		
	P2[6:0]		
	P2[7:1]		
	P3[6:0] OpAmp:C		
	P3[7:1] OpAmp:C		
	P4[6:0]		
	P4[7:1]		
	P5[6:0]		

CY8C3866AXI-040 100-TQFP

0 Errors 0 Warnings 0 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\A\_MyFirstInterruptProject.cydsn\TopDesign\TopDesig...]

File Edit View Debug Project Build Tools Window Help

Microsoft Sans Serif 10 B I U Debug

Workspace Explorer Start Page A\_MyFirstInte...tProject.cydw TopDesign.cysch main.c isr\_1.c Component Catalog...

Configure 'Timer'

Name: Timer\_1

Configure Built-in

Resolution: 16-Bit

Implementation: UDB

Period: 1000 Max Period = 1s

Trigger Mode: None

Capture Mode: None

Enable Mode: Software Only

Run Mode: Continuous

Interrupts: On TC

Datasheet OK Apply Cancel

Output

Show output from: All Protecting... Verify Checksum... Device 'PSoC 3 CY8C3866AX\*-040' was successfully programmed at 03/18/2013

Notice List 0 Errors 0 Warnings

Component Catalog Concept Cypress

- PrISM [v2.10]
- PRS [v2.10]
- PWM [v2.20]
- Quadrature D
- Shift Register
- Timer [v2.30]
- Logic
- Registers
  - Control Registr
  - Status Registr
- Display
  - Character LCD [v1
  - Graphic LCD 8-bit
  - Graphic LCD 16-b
  - Graphic LCD Cont
  - Graphic LCD Cont
  - Graphic LCD Para
  - ResistiveTouch [v
  - Segment LCD - St
  - Segment LCD [v3.

Component Preview Inst\_N Character LCD

Datasheet Character LCD Component

(X=659, Y=498) 0 Errors 0 Warnings 2 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\A\_MyFirstInterruptProject.cydsn\TopDesign\TopDesig...]

File Edit View Debug Project Build Tools Window Help

Microsoft Sans Serif 10 B I U Debug

Workspace Explorer Component Catalog

Start Page A\_MyFirstInte...tProject.cydwv \*TopDesign.cysch main.c isr\_1.c

Configure 'cy\_clock'

Name: timer\_clock

Configure Clock Advanced Built-in

Clock Type: New Existing

Source: <Auto>

Specify: Frequency 1 kHz  
Tolerance: -5% +5%

Summary

API Generated: Yes  
Uses Clock Tree Resource: Yes

By default, all clocks are marked as 'start on reset'. The setting can be changed in the Design Wide Resources editor.

Datasheet OK Apply Cancel

Output

Show output from: All Protecting... Verify Checksum... Device 'PSoC 3 CY8C3866AX\*-040' was successfully programmed at 03/18/2013

Component Catalog

Concept Cypress

Functions Counter [v2.20] CRC [v2.20] Debouncer Glitch Filter [v2.20] PrISM [v2.10] PRS [v2.10] PWM [v2.20] Quadrature Decoder Shift Register Timer [v2.30]

Logic Registers Control Register Status Register

Display Character LCD [v1.0] Graphic LCD 8-bit Graphic LCD 16-bit Graphic LCD Control Graphic LCD Control

Component Preview

Datasheet 8, 16, 24 or 32-bit Timer

Notice List

0 Errors 0 Warnings

Device File

Ready (X=545, Y=481) 0 Errors 0 Warnings 2 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\A\_MyFirstInterruptProject.cydsn\TopDesign\TopDesig...]

File Edit View Debug Project Build Tools Window Help

Microsoft Sans Serif 10 B I U Debug

Workspace Explorer Component Catalog

Start Page A\_MyFirstInte...tProject.cydw \*TopDesign.cysch main.c isr\_1.c

Configure 'cy\_isr'

Name: isr\_1

Basic Built-in

Parameter	Value
InterruptType	LEVEL

Parameter Information

Datasheet OK Apply Cancel

Output

Show output from: All Protecting... Verify Checksum... Device 'PSoC 3 CY8C3866AX\*-040' was successfully programmed at 03/18/2013

Component Catalog

Concept Cypress

- Digital Bidirectional
- Digital Input Pin [v1.60]
- Digital Output Pin
- Power Supervision
- System
  - Boost Converter [v1.60]
  - Bootloadable
  - Bootloader
  - Clock [v1.70]
  - Die Temperature [v1.60]
  - DMA [v1.60]
  - EEPROM [v2.0]
  - External Memory Interface
  - Global Signal Reference
  - Interrupt [v1.60]
  - RTC [v1.70]
  - SleepTimer [v3.10]
  - Sync
  - UDBClockEn
- Thermal Management

Component Preview

Datasheet

8, 16, 24 or 32-bit Timer

Notice List

0 Errors 0 Warnings

Device File

Ready 0 Errors 0 Warnings 2 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\A\_MyFirstInterruptProject.cydsn\TopDesign\TopDesig...]

File Edit View Debug Project Build Tools Window Help

Microsoft Sans Serif 10 B I U Debug

Workspace Explorer Start Page A\_MyFirstInte...tProject.cydw \*TopDesign.cysch main.c isr\_1.c Component Catalog...

Configure 'cy\_pins'

Name: LED1

Pins Mapping Reset Built-in

Number of Pins: 1

[All Pins] Type General Input Output

LED1\_0

Analog  
Digital Input  
 HW Connection  
 Digital Output  
Clock [v1.70]  
Die Temperature [v1.60]  
DMA [v1.60]  
EEPROM [v2.0]  
External Memory [v1.60]  
Global Signal Refe  
Interrupt [v1.60]  
RTC [v1.70]  
SleepTimer [v3.10]  
Sync  
UDBClkEn  
Thermal Management

Datasheet OK Apply Cancel

Output

Show output from: All

Protecting... Verify Checksum... Device 'PSoC 3 CY8C3866AX\*-040' was successfully programmed at 03/18/2013

Component Preview

Datasheet

8, 16, 24 or 32-bit Timer

Notice List

0 Errors 0 Warnings

Device File

Ready (X=470,Y=312) 0 Errors 0 Warnings 2 Notes

This screenshot shows the PSoC Creator 2.1 software interface for a project titled 'A\_MyFirstInterruptProject'. The central window displays the 'Configure 'cy\_pins'' dialog for pin 'LED1'. The 'Type' tab is selected, showing 'Digital Output' is checked. A preview icon shows a green arrow pointing to a terminal. The workspace sidebar shows the project structure with files like 'main.c' and 'isr\_1.c'. The status bar at the bottom indicates the device is successfully programmed.



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\A\_MyFirstInterruptProject.cydsn\A\_MyFirstInterruptProject.cy...]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer

Start Page A\_MyFirstIn...object.cydwr \*TopDesign.cysch main.c isr\_1.c

Project 'A\_MyFirstInterrupt' (4 Projects)

- TopDesign.cysch
- A\_MyFirstInterruptProject.c
- Header Files: device.h
- Source Files: main.c
- Generated\_Source: PSoC3\cy\_boot
  - CyBootAsmKeil
  - CyDmac.c
  - CyDmac.h
  - CyFlash.c
  - CyFlash.h
  - CyLib.c
  - CyLib.h
  - cymem.a51
  - cupins.h

Source Components Datasheets Results

Pins Analog Clocks Interrupts DMA System Directives Flash Security

Output  
Show output from: All  
Protecting...  
Verify Checksum...  
Device 'PSoC 3 CY8C3866AX\*-040' was successfully programmed at 03/18/2013 05:06:14.

Notice List  
0 Errors 0 Warnings

Ready 0 Errors 0 Warnings 2 Notes

The screenshot shows the PSoC Creator 2.1 software interface. The workspace contains a project named 'A\_MyFirstInterrupt' with four files: TopDesign.cysch, A\_MyFirstInterruptProject.c, device.h, and main.c. The main window displays the 'TopDesign.cysch' schematic. The schematic shows a CY8C3866AXI-040 100-TQFP chip with various pins and components connected. On the right side of the schematic, there is a pin assignment table:

Alias	Name	Port	Pin
\LCD:LCDPort[6:0]\	P2[6:0]		95..99,1..2
LED1	PO[0] OpAmp:out		71

The bottom status bar indicates 'Ready' and shows error, warning, and note counts: 0 Errors, 0 Warnings, and 2 Notes.



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\AN54460\A\_MyFirstInterruptProject.cydsn\main.c]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer

Project 'A\_MyFirstInterrupt'

- TopDesign.cysch
- A\_MyFirstInterruptProject.c
- Header Files
  - device.h
- Source Files
  - main.c
- Generated\_Source
  - PSoC3
    - cy\_boot
      - CyBootAsmKeil
      - CyDmac.c
      - CyDmac.h
      - CyFlash.c
      - CyFlash.h
      - CyLib.c
      - CyLib.h
      - cymem.a51
      - cupins.h

Source Components Datasheets Results

Start Page A\_MyFirstInte...tProject.cydw \*TopDesign.cysch \*main.c isr\_1.c

```
1 /* =====
2  * Copyright YOUR COMPANY, THE YEAR
3  * All Rights Reserved
4  * UNPUBLISHED, LICENSED SOFTWARE.
5  * CONFIDENTIAL AND PROPRIETARY INFORMATION
6  * WHICH IS THE PROPERTY OF your company.
7  *
8  * =====
9 */
10 #include <device.h>
11
12 /* Global variable defined in Timer ISR file isr_1.c */
13 extern volatile uint8 toggle_flag;
14
15 void main()
16 {
17     CYGlobalIntEnable; /* Enable global interrupts. */
18
19     /* Initialize, start components */
20     Timer_1_Start();
21     isr_1_Start();
22     LCD_Start();
23     LCD_Position(0,2);
24     LCD_PrintString("My Name");
25 }
```

Notice List

0 Errors 0 Warnings

Output

Show output from: All

Protecting...  
Verify Checksum...  
Device 'PSoC 3 CY8C3866AX\*-040' was successfully programmed at 03/18/2013 05:06:14.



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\AN54460\A\_MyFirstInterruptProject.cydsn\main.c]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer

Start Page A\_MyFirstInte...tProject.cydw \*TopDesign.cysch \*main.c isr\_1.c

Source Components Datasheets Results

```
18     /* Initialize, start components */
19     Timer_1_Start();
20     isr_1_Start();
21     LCD_Start();
22     LCD_Position(0,2);
23     LCD_PrintString("My Name");
24
25     for(;;)
26     {
27         /* Check if flag is set in ISR */
28         if(toggle_flag == 1)
29         {
30             /* Toggle the LED1 pin */
31             LED1_Write(~LED1_ReadDataReg());
32
33             /* Clear the flag */
34             toggle_flag = 0;
35         }
36     }
37 }
38
39 /* [] END OF FILE */
40
41
```

Notice List

0 Errors 0 Warnings

Output

Show output from: All

Protecting... Verify Checksum... Device 'PSoC 3 CY8C3866AX\*-040' was successfully programmed at 03/18/2013 05:06:14.

Ln 5 Col 2 INS 0 Errors 0 Warnings 2 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\PicuInterruptProject.cydsn\Generated\_Source\PSO...]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer (4 ...)

Start Page A\_MyFirstInb...tProject.cydw \*TopDesign.cysch \*main.c isr\_1.c

Header.Files device.h

Source Files main.c

Generated\_Source

PSoC3

- cy\_boot
- isr\_1
  - isr\_1.c
  - isr\_1.h
- LCD
  - LCD.c
  - LCD.h
  - LCD\_P
- LCD\_LCDP
  - LCD\_LC
  - LCD\_LC
  - LCD\_LC
- LED1
  - LED1.c

Source Components Datasheets Results

Notice List

0 Errors 0 Warnings

De... File

Output

Show output from: All

Protecting...

Verify Checksum...

Device 'PSoC 3 CY8C3866AXT-040' was successfully programmed at 03/18/2013 05:06:14.

Ln 9 Col 1 INS 0 Errors 0 Warnings 2 Notes

```
1  ****
2  * File Name: isr_1.c
3  * Version 1.60
4  *
5  * Description:
6  *   API for controlling the state of an interrupt.
7  *
8  * Note:
9  *
10 ****
11 * Copyright 2008-2010, Cypress Semiconductor Corporation. All rights reserved.
12 * You may use this file only in accordance with the license, terms, conditions,
13 * disclaimers, and limitations in the end user license agreement accompanying
14 * the software package with which this file was provided.
15 ****
16 ****
17
18
19 #include <CYDEVICE.H>
20 #include <CYDEVICE_TRM.H>
21 #include <CYLIB.H>
22 #include <isr_1.H>
23
24 ****
```



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\\AN54460\B\_PicuInterruptProject.cydsn\Generated\_Source\PSo...]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer (4 ...)

Source Components Datasheets Results

Start Page A\_MyFirstInb...tProject.cydw \*TopDesign.cysch \*main.c \*isr\_1.c

```
25  ****
26  * Place your includes, defines and code here
27  ****
28  /* `#START isr_1_intc` */
29  /* `#END` */
30  ****
31  * Function Name: isr_1_Start
32  ****
33  * Summary:
34  * Set up the interrupt and enable it.
35  * Parameters:
36  * void.
37  * Return:
38  * void.
39  ****
40  void isr_1_Start(void)
41  {
42  /* For all we know the interrupt is active. */
43  isr_1_Disable();
44
45  /* Set the ISR to point to the isr_1 Interrupt. */
46  isr_1_SetVector(isr_1_Interrupt);
47
48  /* Set the priority. */
49  isr_1_SetPriority(isr_1_INTC_PRIOR_NUMBER);
```

Notice List

0 Errors 0 Warnings

Output

Show output from: All

Protecting...

Verify Checksum...

Device 'PSoC 3 CY8C3866AXT-040' was successfully programmed at 03/18/2013 05:06:14.

Ln 39 Col 1 INS 0 Errors 0 Warnings 2 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\PicuInterruptProject.cydsn\Generated\_Source\PSO...]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer (4 ...)

Source Components Datasheets Results

```
Start Page A_MyFirstInb...tProject.cydw *TopDesign.cysch *main.c *isr_1.c
50     /* Enable it. */
51     isr_1_Enable();
52 }
53 ****
54 * Function Name: isr_1_StartEx
55 ****
56 * Summary:
57 * Set up the interrupt and enable it.
58 * Parameters:
59 *   address: Address of the ISR to set in the interrupt vector table.
60 * Return:
61 *   void.
62 ****
63 void isr_1_StartEx(cyisraddress address)
64 {
65     /* For all we know the interrupt is active. */
66     isr_1_Disable();
67
68     /* Set the ISR to point to the isr_1 Interrupt. */
69     isr_1_SetVector(address);
70
71     /* Set the priority. */
72     isr_1_SetPriority(isr_1_INTC_PRIOR_NUMBER);
73
74 }
```

Notice List

0 Errors 0 Warnings

Output

Show output from: All

Protecting...

Verify Checksum...

Device 'PSoC 3 CY8C3866AXT-040' was successfully programmed at 03/18/2013 05:06:14.

Ln 63 Col 1 INS 0 Errors 0 Warnings 2 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\PicuInterruptProject.cydsn\Generated\_Source\PSO...]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer (4 ...)

Source Components Datasheets Results

```
Start Page A_MyFirstInb...tProject.cydw *TopDesign.cysch *main.c *isr_1.c
74:     /* Enable it. */
75:     isr_1_Enable();
76:
77: }
78:
79: /*****
80: * Function Name: isr_1_Stop
81: ****
82: * Summary:
83: *   Disables and removes the interrupt.
84: *
85: * Parameters:
86: *
87: *
88: * Return:
89: *   void.
90: *
91: ****/
92: void isr_1_Stop(void)
93: {
94:     /* Disable this interrupt. */
95:     isr_1_Disable();
96: }
97:
98: /*****
```

Notice List

0 Errors 0 Warnings

Output

Show output from: All

Protecting...

Verify Checksum...

Device 'PSoC 3 CY8C3866AXT-040' was successfully programmed at 03/18/2013 05:06:14.

Ln 63 Col 1 INS 0 Errors 0 Warnings 2 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\PicuInterruptProject.cydsn\Generated\_Source\PSO...]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer (4 ...)

Source Components Datasheets Results

Start Page A\_MyFirstIn...tProject.cydw \*TopDesign.cysch \*main.c \*isr\_1.c

```
98  ****
99  * Function Name: isr_1 Interrupt
100 ****
101 * Summary:
102 *   The default Interrupt Service Routine for isr_1.
103 *   Add custom code between the comments to keep the next version of this file
104 *   from over writing your code.
105 * Parameters:
106 * Return:
107 *   void.
108 ****
109 CY_ISR(isr_1 Interrupt)
110 {
111     /* Place your Interrupt code here. */
112     /* '#START isr_1 Interrupt' */
113
114     /* '#END' */
115
116     /* PSoC3 ES1, ES2 RTC ISR PATCH */
117     #if(CYDEV_CHIP_FAMILY_USED == CYDEV_CHIP_FAMILY_PSOC3)
118         #if((CYDEV_CHIP_REVISION_USED <= CYDEV_CHIP_REVISION_3A_ES2) && (isr_1_ES2_PATCH))
119             isr_1_ISR_PATCH();
120         #endif
121     #endif
122 }
```

Notice List

0 Errors 0 Warnings

Output

Show output from: All

```
Protecting...
Verify Checksum...
Device 'PSoC 3 CY8C3866AXT-040' was successfully programmed at 03/18/2013 05:06:14.
```

Ln 108 Col 1 INS 0 Errors 0 Warnings 2 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\PicuInterruptProject.cydsn\Generated\_Source\PSO...]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer (4 ...)

Source Components Datasheets Results

Start Page A\_MyFirstInb...tProject.cydwv \*TopDesign.cysch \*main.c \*isr\_1.c

```
124 // ****
125 * Function Name: isr_1_SetVector
126 ****
127 * Summary:
128 *   Change the ISR vector for the Interrupt. Note calling isr_1_Start
129 *   will override any effect this method would have had. To set the vector before
130 *   the component has been started use isr_1_StartEx instead.
131 * Parameters:
132 *   address: Address of the ISR to set in the interrupt vector table.
133 * Return:
134 *   void.
135 /**
136 void isr_1_SetVector(cyisraddress address)
137 {
138     CY_SET_REG16(isr_1_INTC_VECTOR, (uint16) address);
139 }
140 /**
141 * Function Name: isr_1_GetVector
142 ****
143 * Summary:
144 *   Gets the "address" of the current ISR vector for the Interrupt.
145 * Parameters:
146 *   void.
147 *
148 */
```

Notice List

0 Errors 0 Warnings

Output

Show output from: All

Protecting...

Verify Checksum...

Device 'PSoC 3 CY8C3866AXT-040' was successfully programmed at 03/18/2013 05:06:14.

Ln 146 Col 1 INS 0 Errors 0 Warnings 2 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\PicuInterruptProject.cydsn\Generated\_Source\PSO...]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer (4 ...)

Source Components Datasheets Results

Start Page A\_MyFirstIn...tProject.cydwr \*TopDesign.cysch \*main.c \*isr\_1.c

```
146 * Parameters:
147 *   void.
148 * Return:
149 *   Address of the ISR in the interrupt vector table.
150 ****
151 cyisraddress isr_1_GetVector(void)
152 {
153     return (cyisraddress) CY_GET_REG16(isr_1_INTC_VECTOR);
154 }
155 ****
156 * Function Name: isr_1_SetPriority
157 ****
158 * Summary:
159 *   Sets the Priority of the Interrupt. Note calling isr_1_Start
160 *   or isr_1_StartEx will override any effect this method would have had.
161 *   This method should only be called after isr_1_Start or
162 *   isr_1_StartEx has been called. To set the initial
163 *   priority for the component use the cydwr file in the tool.
164 * Parameters:
165 *   priority: Priority of the interrupt. 0 - 7, 0 being the highest.
166 * Return:
167 *   void.
168 *
169 ****
170 ****
```

Notice List

0 Errors 0 Warnings

Output

Show output from: All

Protecting...

Verify Checksum...

Device 'PSoC 3 CY8C3866AXT-040' was successfully programmed at 03/18/2013 05:06:14.

Ln 169 Col 1 INS 0 Errors 0 Warnings 2 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\PicuInterruptProject.cydsn\Generated\_Source\PSO...]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer (4 ...)

Source Components Datasheets Results

```
170  ****
171  void isr_1_SetPriority(uint8 priority)
172  {
173      *isr_1_INTC_PRIOR = priority << 5;
174  }
175
176  ****
177  * Function Name: isr_1_GetPriority
178  ****
179  * Summary:
180  *     Gets the Priority of the Interrupt.
181  * Parameters:
182  *     void.
183  * Return:
184  *     Priority of the interrupt. 0 - 7, 0 being the highest.
185  ****
186  uint8 isr_1_GetPriority(void)
187  {
188      uint8 priority;
189
190
191      priority = *isr_1_INTC_PRIOR >> 5;
192
193
194 }
```

Notice List

0 Errors 0 Warnings

Output

Show output from: All

```
Protecting...
Verify Checksum...
Device 'PSoC 3 CY8C3866AXT-040' was successfully programmed at 03/18/2013 05:06:14.
```

Ln 185 Col 1 INS 0 Errors 0 Warnings 2 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\PicuInterruptProject.cydsn\Generated\_Source\PSO...]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer (4 ...)

Source Components Datasheets Results

Start Page A\_MyFirstInb...tProject.cydw \*TopDesign.cysch \*main.c \*isr\_1.c

```
196 // ****
197 * Function Name: isr_1_Enable
198 ****
199 * Summary:
200 *   Enables the interrupt.
201 * Parameters:
202 *   void.
203 * Return:
204 *   void.
205 ****
206 void isr_1_Enable(void)
207 {
208     /* Enable the general interrupt. */
209     *isr_1_INTC_SET_EN = isr_1__INTC_MASK;
210 }
211 // ****
212 * Function Name: isr_1_GetState
213 ****
214 * Summary:
215 *   Gets the state (enabled, disabled) of the Interrupt.
216 * Parameters:
217 *   void.
218 * Return:
219 *   1 if enabled, 0 if disabled.
220 ****
```

Notice List

0 Errors 0 Warnings

Output

Show output from: All

Protecting...

Verify Checksum...

Device 'PSoC 3 CY8C3866AXT-040' was successfully programmed at 03/18/2013 05:06:14.

Ln 211 Col 1 INS 0 Errors 0 Warnings 2 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\PicuInterruptProject.cydsn\Generated\_Source\PSO...]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer (4 ...)

Source Components Datasheets Results

Start Page A\_MyFirstInte...tProject.cydwv \*TopDesign.cysch \*main.c \*isr\_1.c

```
220 ****
221 uint8 isr_1_GetState(void)
222 {
223     /* Get the state of the general interrupt. */
224     return (*isr_1_INTC_SET_EN & isr_1__INTC_MASK) ? 1:0;
225 }
226
227 /**
228 * Function Name: isr_1_Disable
229 ****
230 * Summary:
231 *     Disables the Interrupt.
232 * Parameters:
233 *     void.
234 * Return:
235 *     void.
236 *
237 */
238 void isr_1_Disable(void)
239 {
240     /* Disable the general interrupt. */
241     *isr_1_INTC_CLR_EN = isr_1__INTC_MASK;
242 }
243
244 /**
```

Notice List

0 Errors 0 Warnings

Output

Show output from: All

Protecting...

Verify Checksum...

Device 'PSoC 3 CY8C3866AX\*-040' was successfully programmed at 03/18/2013 05:06:14.

Ready

Ln 211 Col 1 INS 0 Errors 0 Warnings 2 Notes



# Lab\_4 Interrupts

AN54460 - PSoC Creator 2.1 [D:\...\AN54460\PicuInterruptProject.cydsn\Generated\_Source\PSo...]

File Edit View Debug Project Build Tools Window Help

Workspace Explorer (4 ...) Start Page A\_MyFirstInte...tProject.cydw \*TopDesign.cysch \*main.c \*isr\_1.c

Header Files device.h  
Source Files main.c  
Generated\_Source PSoC3  
cy\_boot  
isr\_1  
isr\_1.c  
isr\_1.h  
LCD  
LCD.c  
LCD.h  
LCD\_Pt  
LCD\_LCDP  
LCD\_LC  
LCD\_LC  
LCD\_LC  
LED1  
LED1.c

Source Components Datasheets Results

Notice List 0 Errors 0 Warnings

Output

Show output from: All Protecting... Verify Checksum... Device 'PSoC 3 CY8C3866AXT-040' was successfully programmed at 03/18/2013 05:06:14.

```
246 ****
247 * Summary:
248 * Causes the Interrupt to enter the pending state, a software method of
249 * generating the interrupt.
250 * Parameters:
251 * void.
252 * Return:
253 * void.
254 ****
255 void isr_1_SetPending(void)
256 {
257     *isr_1_INTC_SET_PD = isr_1__INTC_MASK;
258 }
259 ****
260 * Function Name: isr_1_ClearPending
261 ****
262 * Summary:
263 * Clears a pending interrupt.
264 * Parameters:
265 * void.
266 * Return:
267 * void.
268 *
269 ****
270 ****
```

Ln 269 Col 1 INS 0 Errors 0 Warnings 2 Notes

File Explorer (4 ...)

Source Components Datasheets Results

Device List

0 Errors 0 Warnings

Start Page A\_MyFirstInte...tProject.cydw \*TopDesign.cysch \*main.c \*isr\_1.c

```
252 * Return:  
253 * void.  
254 ****  
255 void isr_1_SetPending(void)  
256 {  
257     *isr_1_INTC_SET_PD = isr_1__INTC_MASK;  
258 }  
259  
260 ****  
261 * Function Name: isr_1_ClearPending  
262 ****  
263 * Summary:  
264 * Clears a pending interrupt.  
265 * Parameters:  
266 * void.  
267 * Return:  
268 * void.  
269 */  
270 ****  
271 void isr_1_ClearPending(void)  
272 {  
273     *isr_1_INTC_CLR_PD = isr_1__INTC_MASK;  
274 }
```

Output

Show output from: All

Protecting...

Verify Checksum...

Device 'PSoC 3 CY8C3866AX\*-040' was successfully programmed at 03/18/2013 05:06:14.

Ln 269 Col 1 INS 0 Errors 0 Warnings 2 N

На сайті фірми Cypress знаходиться більше 200 Application Notes і Reference Designs, які ілюструють області застосування мікроконтролерів PSOC.

**Design Support - Microsoft Internet Explorer**

File Edit View Favorites Tools Help

Address: http://www.cypress.com/portal/server.pt?space=Community/Page&control=SetCommunity&Community

**Design Resources**

Select one of the following materials to help you design-in Cypress products: Application Notes, Datasheets, Developer Kits, Errata Updates, Evaluation Boards, Models, Reference Designs, Software & Drivers and Technical Articles.

**Select Product Group:** All Product Groups

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- Application Specific Clocks
- Async SRAM
- Auto Power Products
- Backplane Interface & Clock Mgmt
- Bluetooth Solutions

**Apply Filter**

Application Notes		Datasheets	Developer Kits	Errata Update	Evaluation Boards
Models	More Resources	Reference Designs	Software and Drivers	Technical Articles	
PSoC Mixed-Signal Array	AN2267a - Standard - Single Cell Li-Ion Battery Charger using CY8C21xxx	Sort	Date	Downloads	
PSoC Mixed-Signal Array	AN2260 - Standard - Rapid NiCd/NiMH Battery Charger and DC Brushed Motor Controller for Autonomous Appliances	Apr 19, 2005	AN2267A.PDF AN2267A.ZIP		
PSoC Mixed-Signal Array	AN2026b - Support - In-System Serial Programming Protocol CY8C24794 and CY8C29xxx	Apr 8, 2005	AN2260.PDF AN2260.ZIP		
PSoC Mixed-Signal Array	AN2266 - Support - 16-bit PWM/PWM-DACs using One Digital PSOC(TM) Block	Apr 8, 2005	AN2266.PDF AN2266.ZIP		
PSoC Mixed-Signal Array	AN2279 - Support - Dynamic I2C Addressing Implemented with I2C Hardware User Modules	Apr 8, 2005	AN2279.PDF AN2279.ZIP		
PSoC Mixed-Signal Array	AN2267 - Standard - Single Cell Li-Ion Battery Charger	Apr 1, 2005	AN2267.PDF AN2267.ZIP		
PSoC Mixed-Signal Array	AN2222a - Support - Flex-Pod Soldering Guide	Mar 31, 2005	AN2222A.PDF		
PSoC Mixed-Signal Array	AN2233a - Support - Capacitive Switch Scan	Mar 31, 2005	AN2233A.PDF		
PSoC Mixed-Signal Array	AN2276 - Support - Binary Weighted Single-Pole IIR Low-Pass Filters	Mar 29, 2005	AN2276.PDF AN2276.ZIP		
PSoC Mixed-Signal Array	AN2277 - Support - Capacitive Front Panel Display Demonstration	Mar 29, 2005	AN2277.PDF AN2277.ZIP		

Found 201 items 1 - 10 | 11 - 20 | 21 - 30 | 31 - 40 | 41 - 50 | 51 - 60 | 61 - 70 | 71 - 80 | 81 - 90 | 91 - 100 | see 1 - 100 | next 100

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