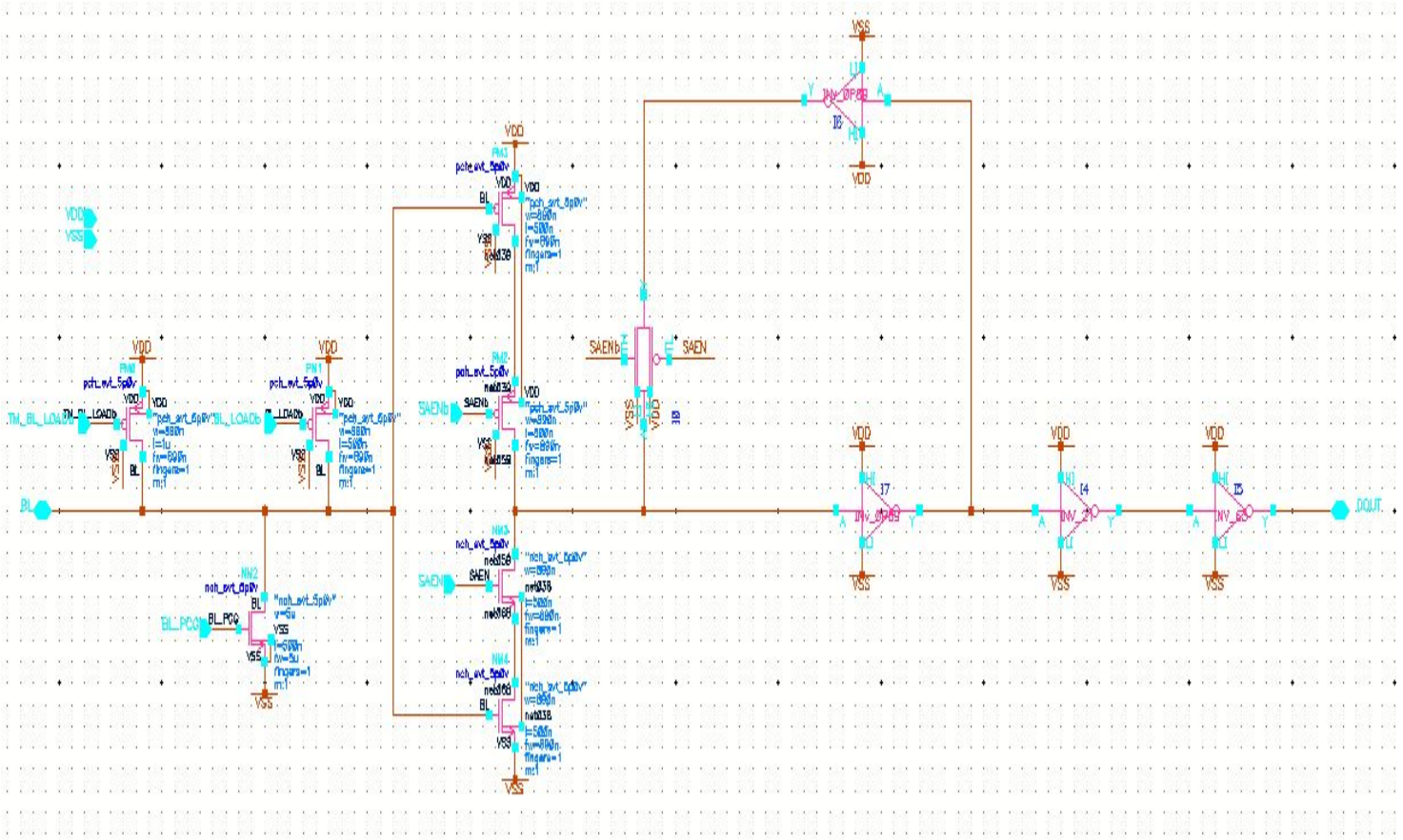
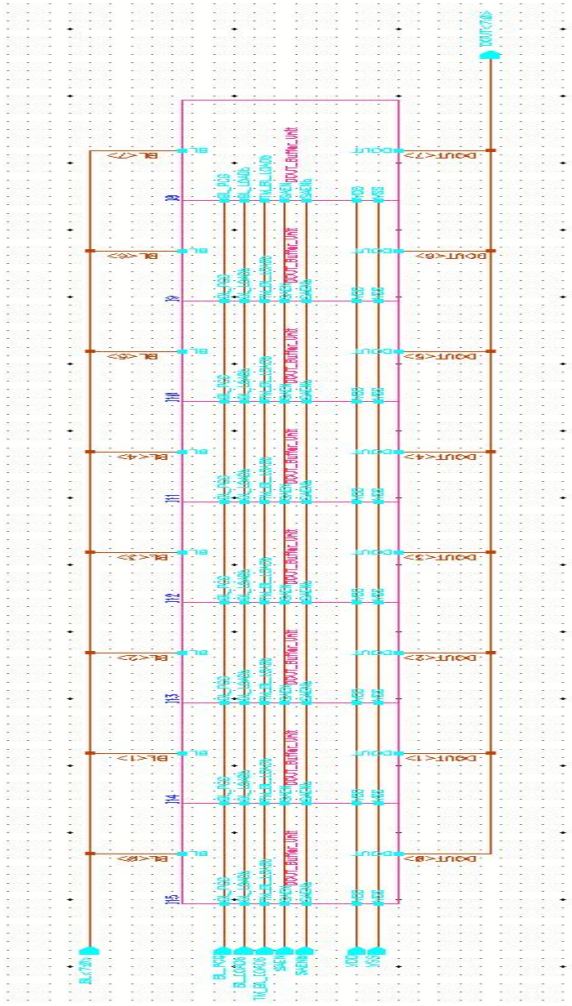
DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic

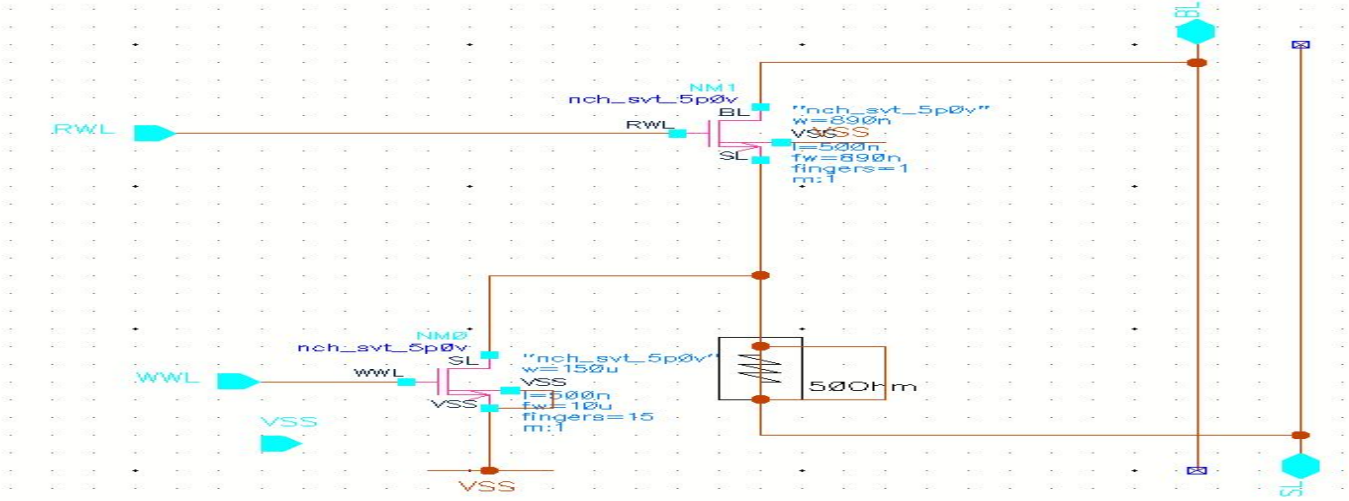


DOUT_Buffer_Unit
_Schematic

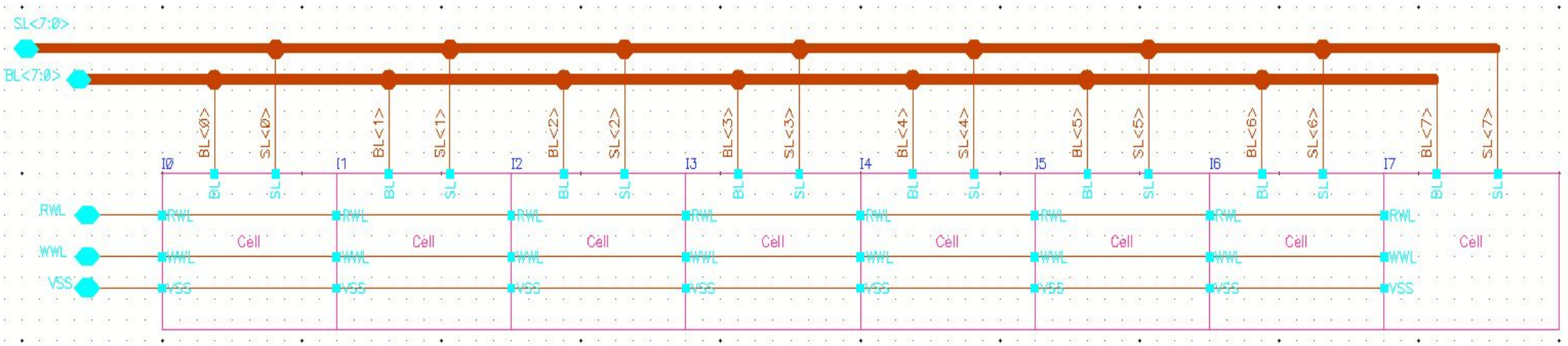


DOUT_Buffer_Unit_8C_Schematic

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic

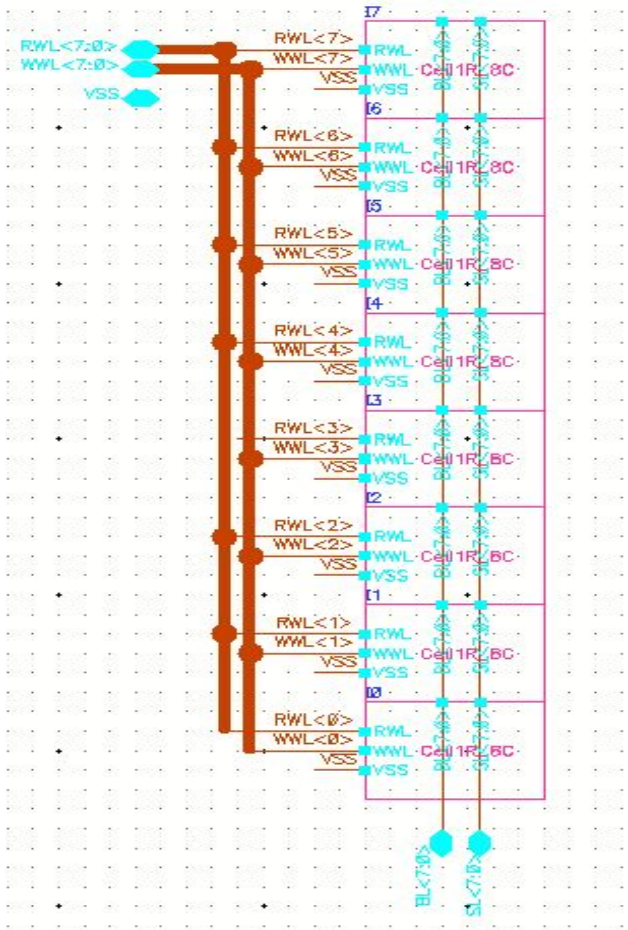


Cell_Schematic

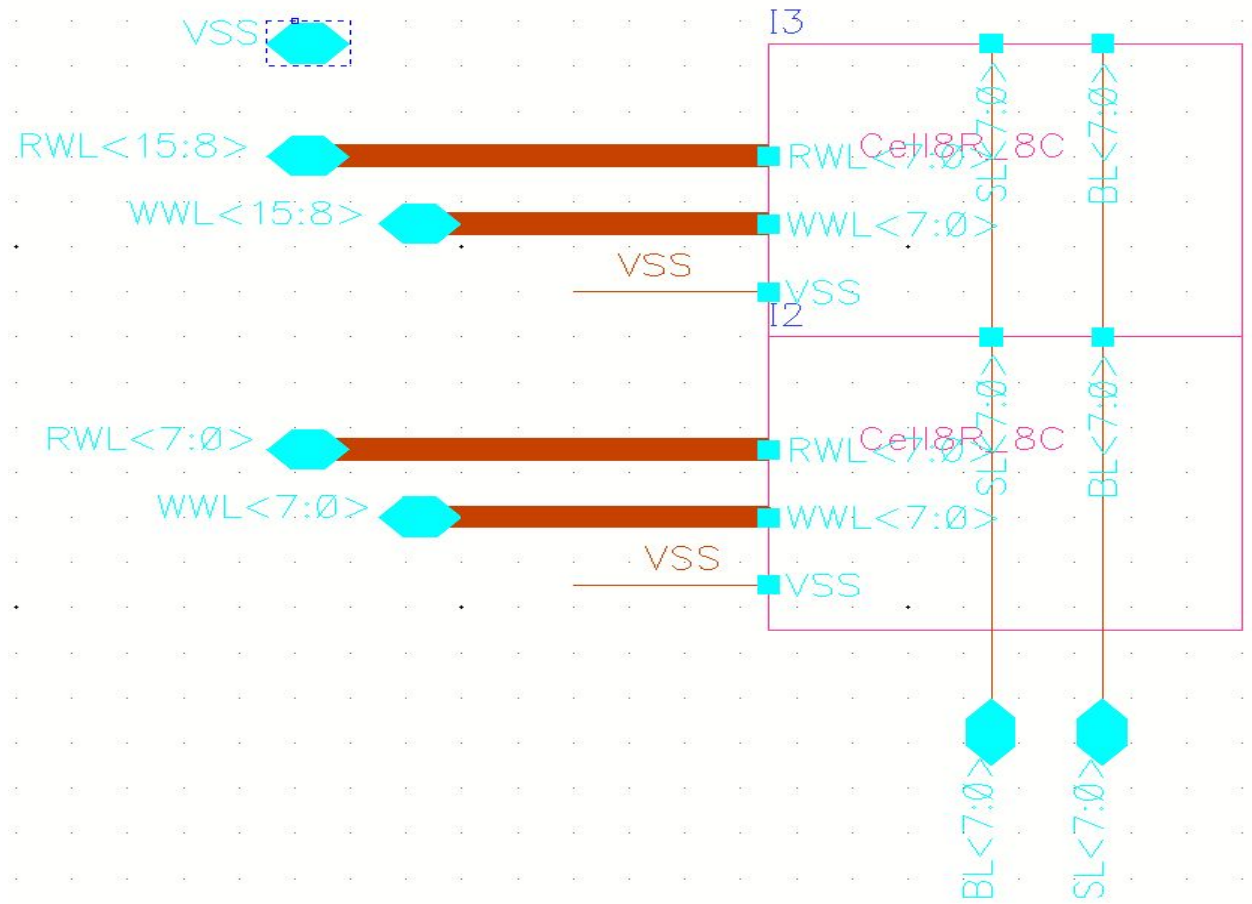


Cell1R_8C_Schematic

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic

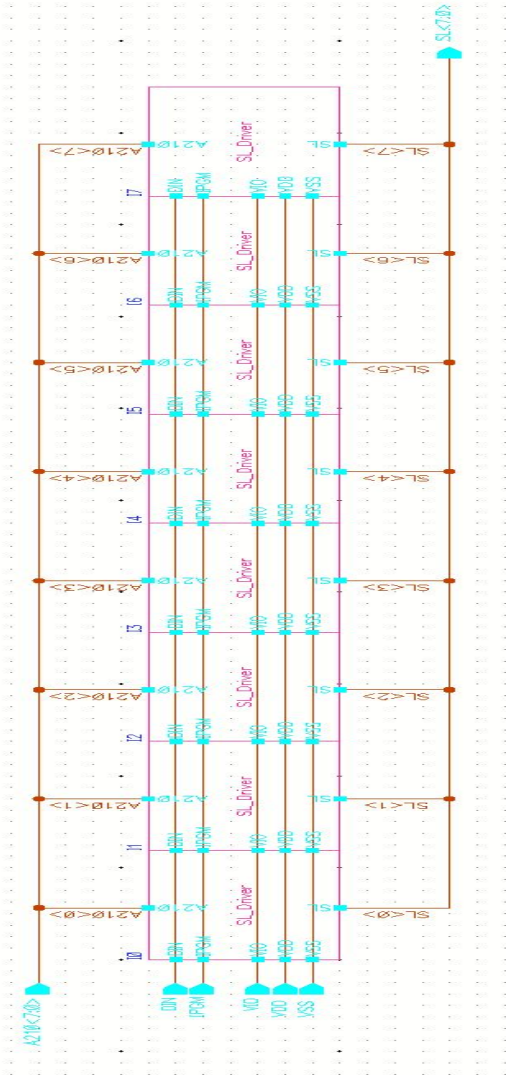


Cell8R_8C_Schematic

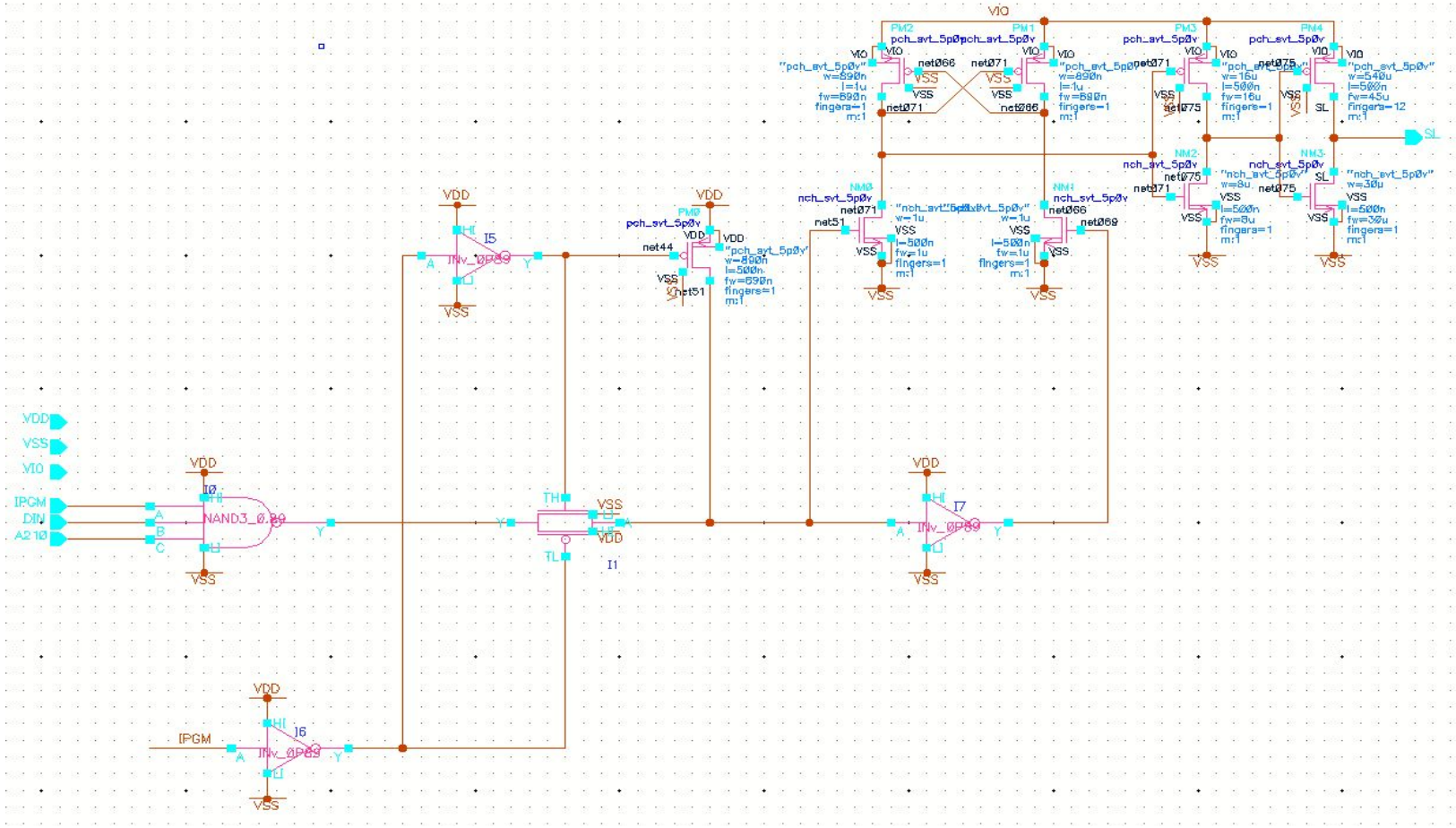


Cell16R_8C_Schematic

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic

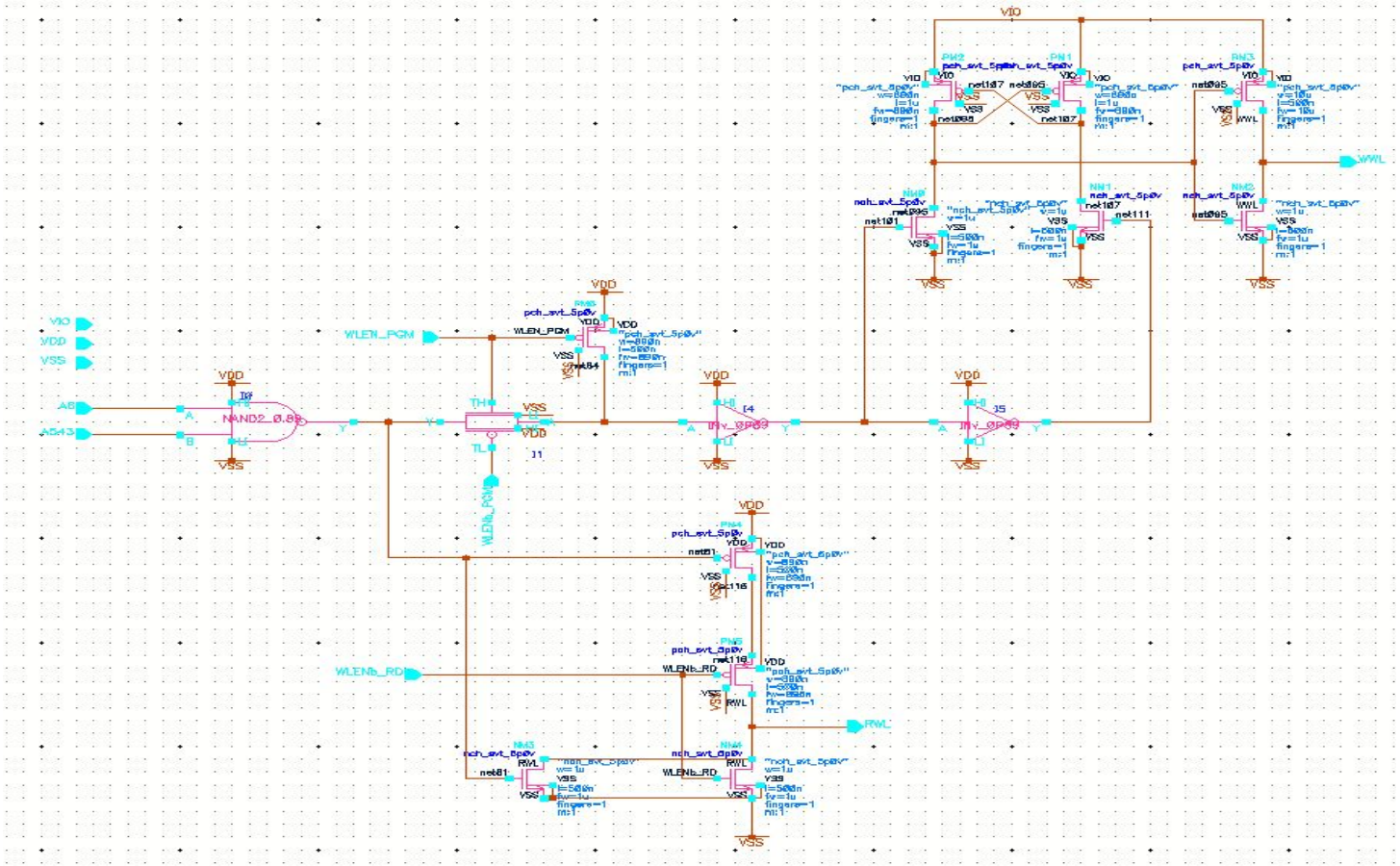


SL_Driver
_8C_Schematic



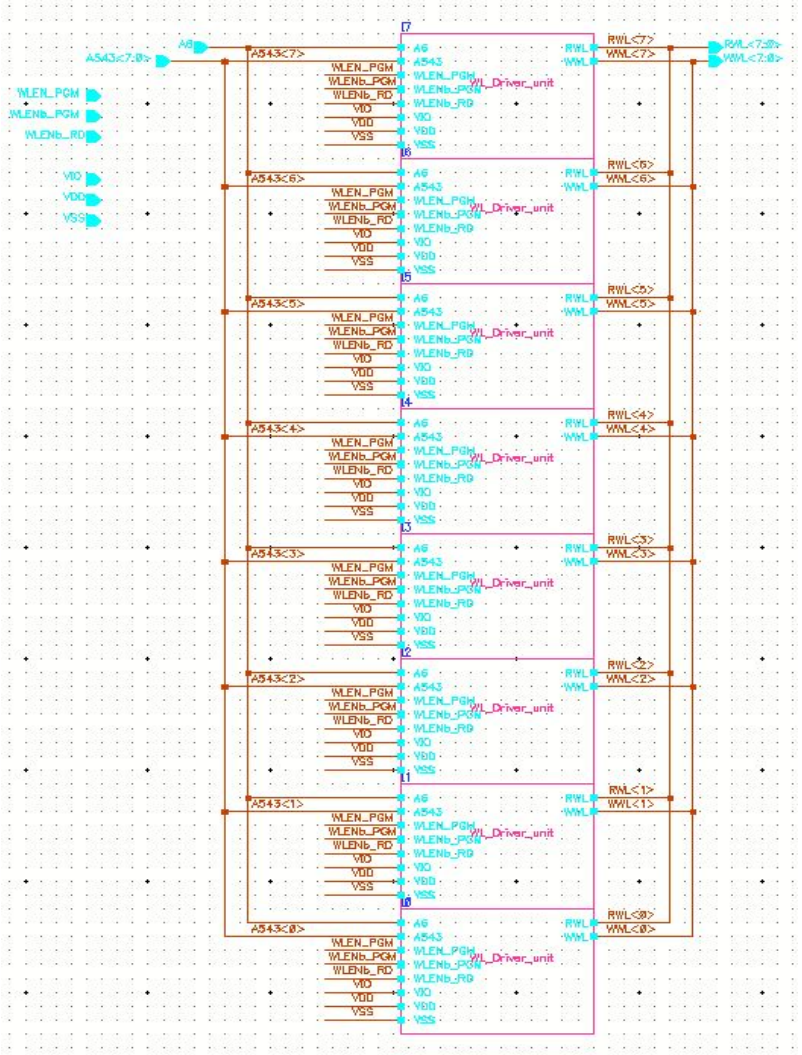
SL_Driver_Schematic

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic

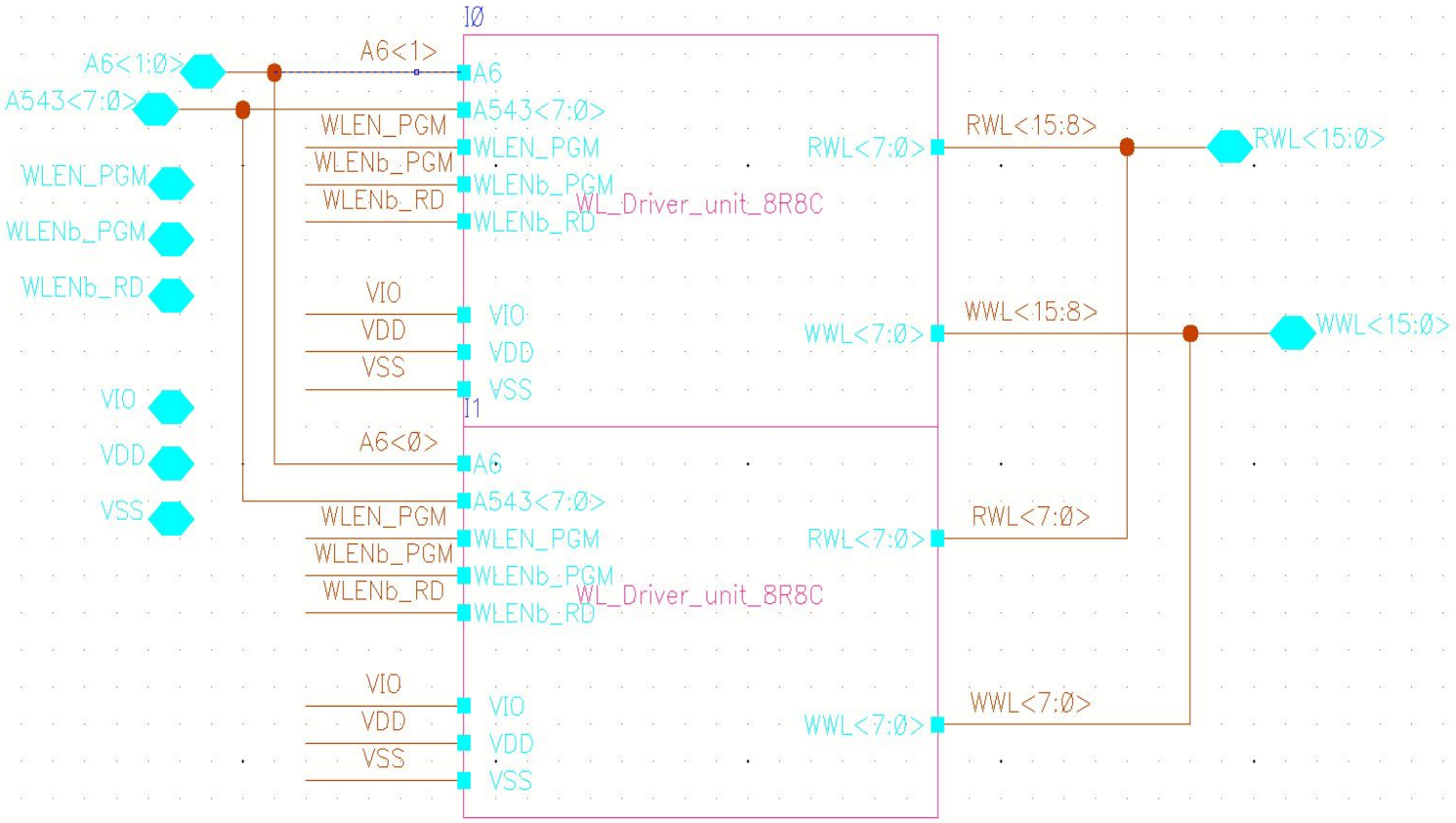


WL_Driver_Unit_Schematic

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic

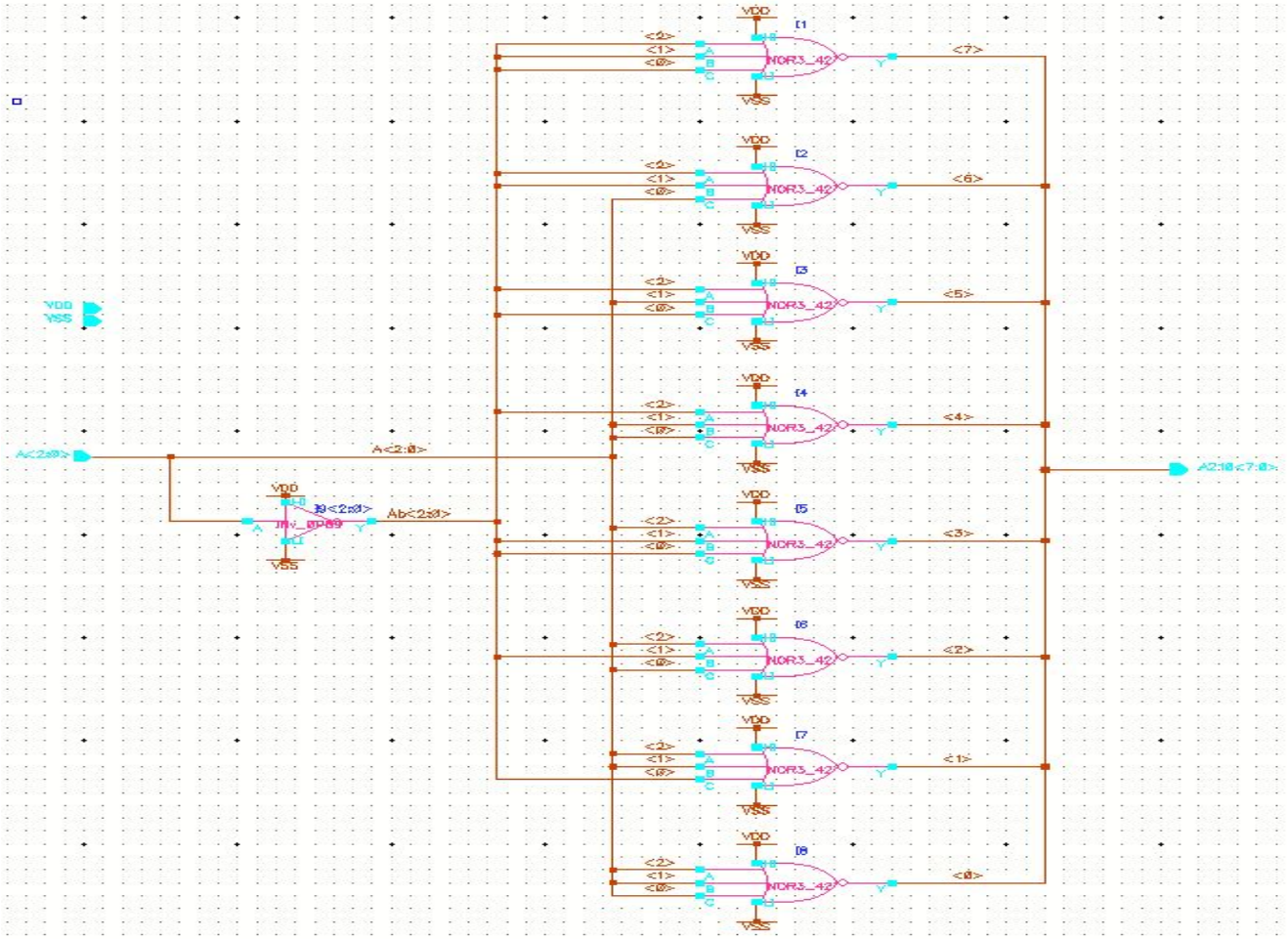


WL_Driver_Unit_1R8C



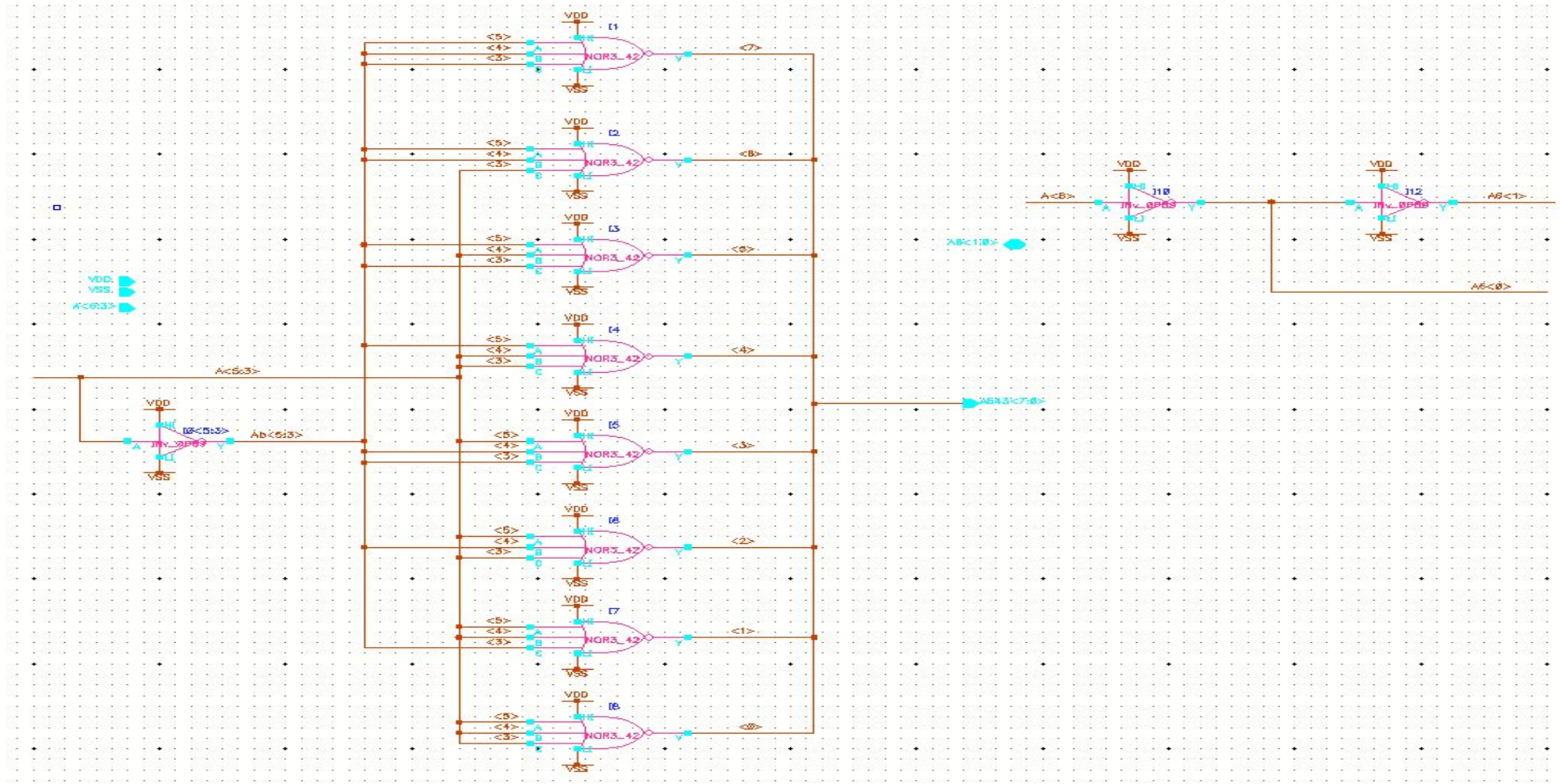
WL_Driver_Unit_8R8C

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic



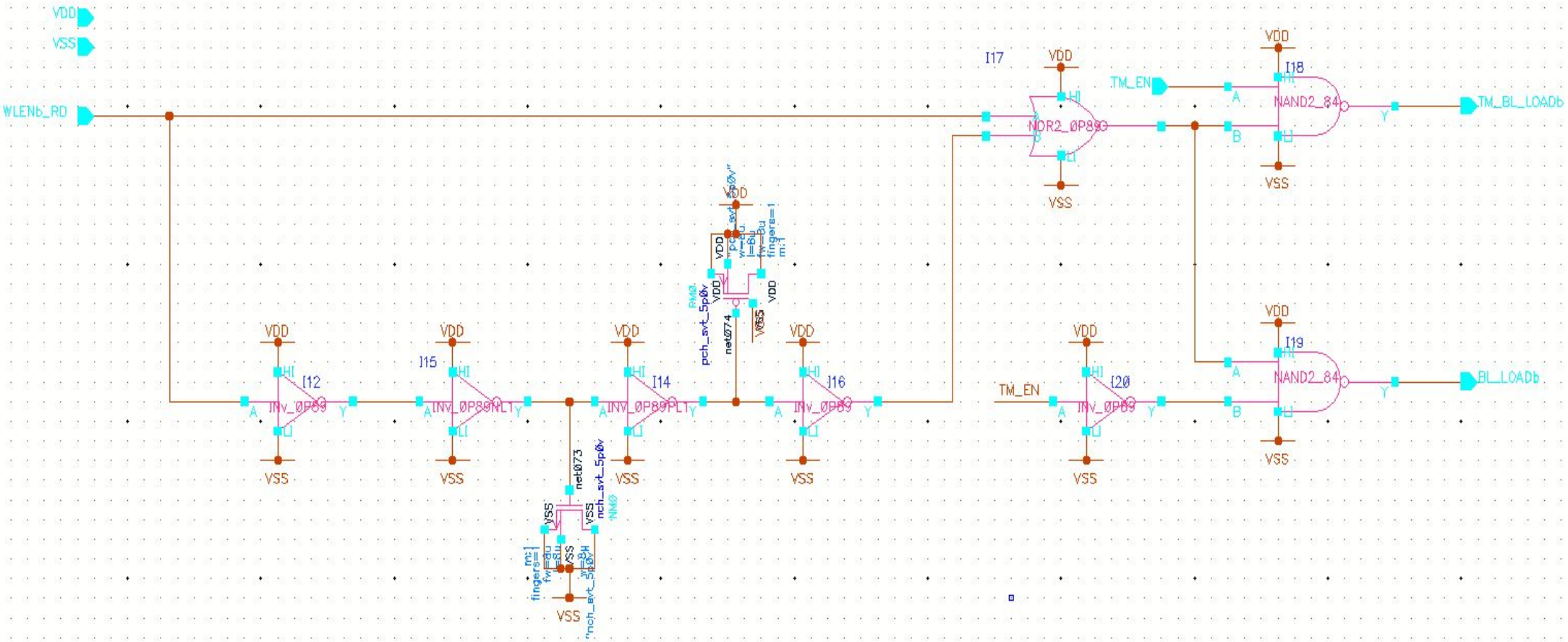
Ypre_Decoder_Schemati
c

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic



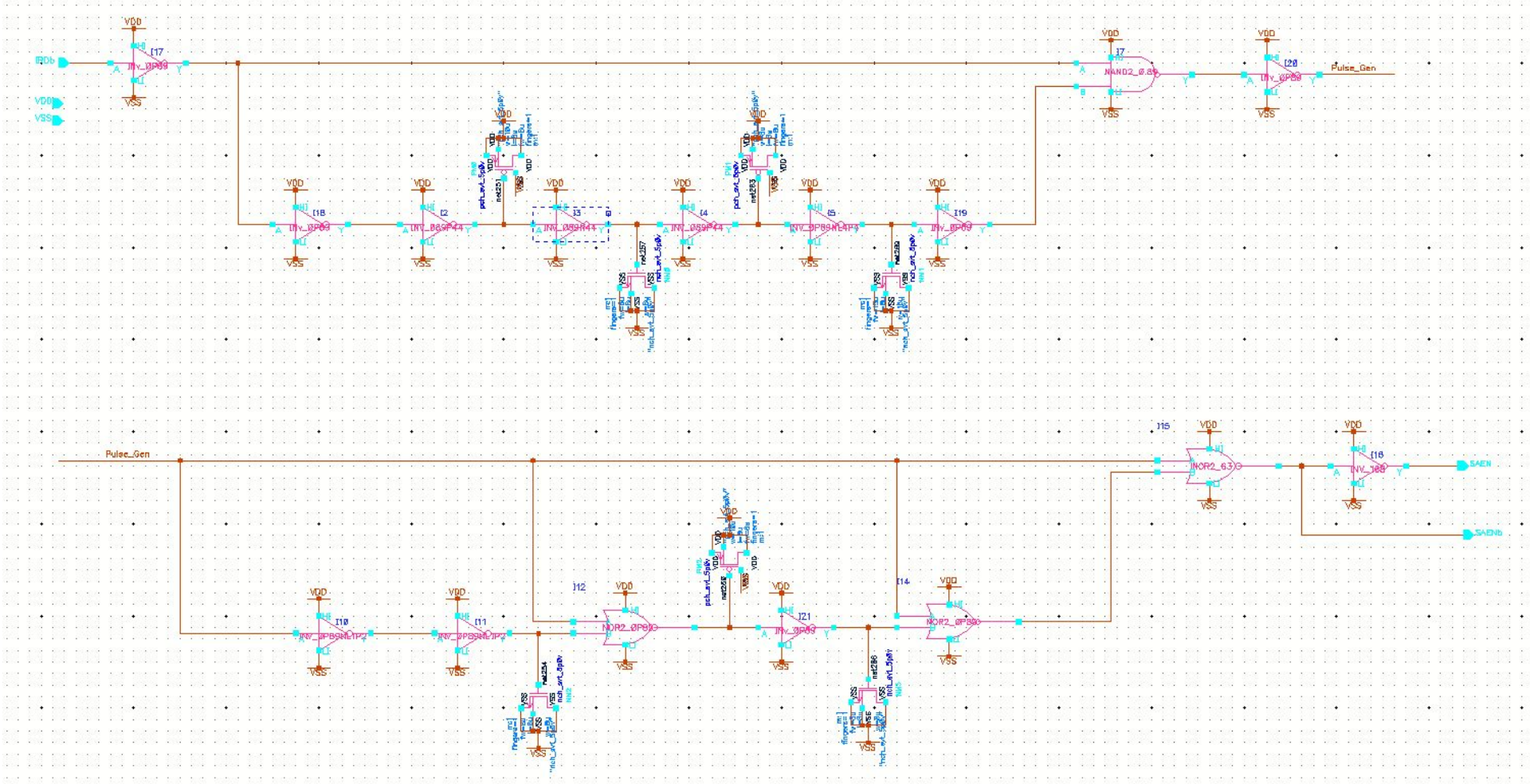
Xpre_Decoder_Schematic

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic



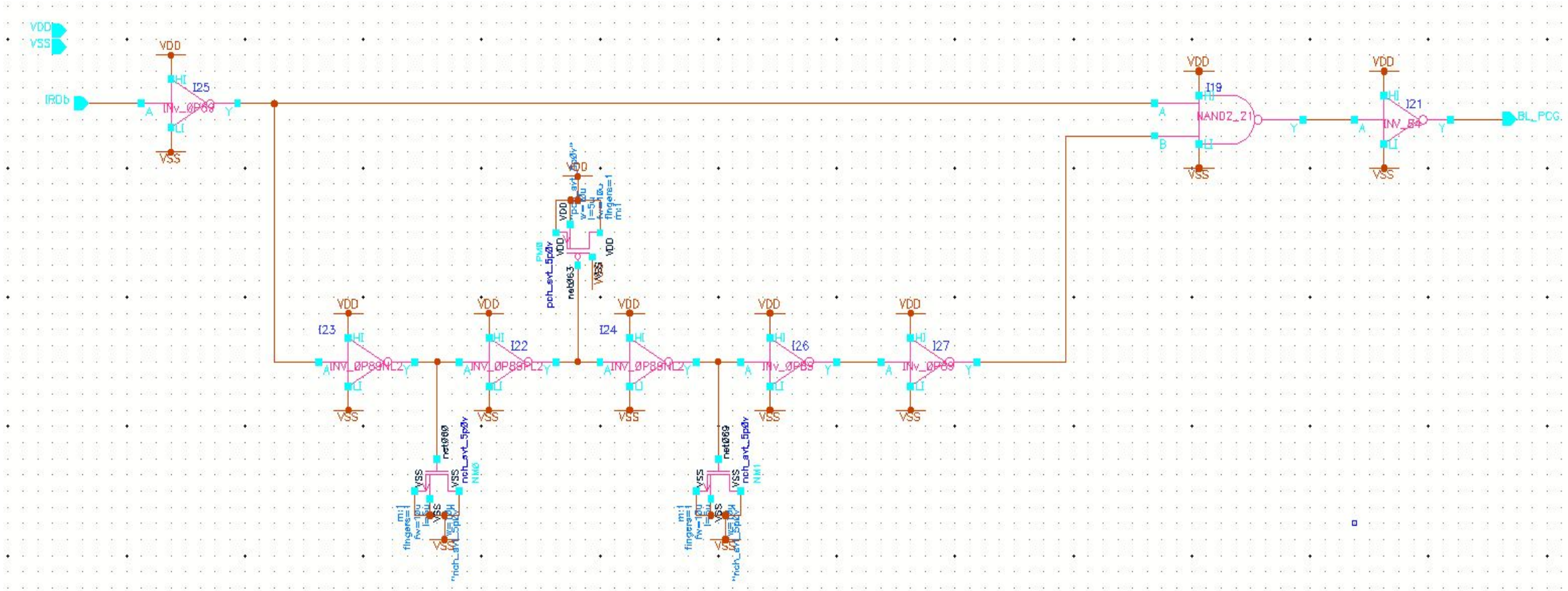
BL_LoADb_Schemati
c

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic



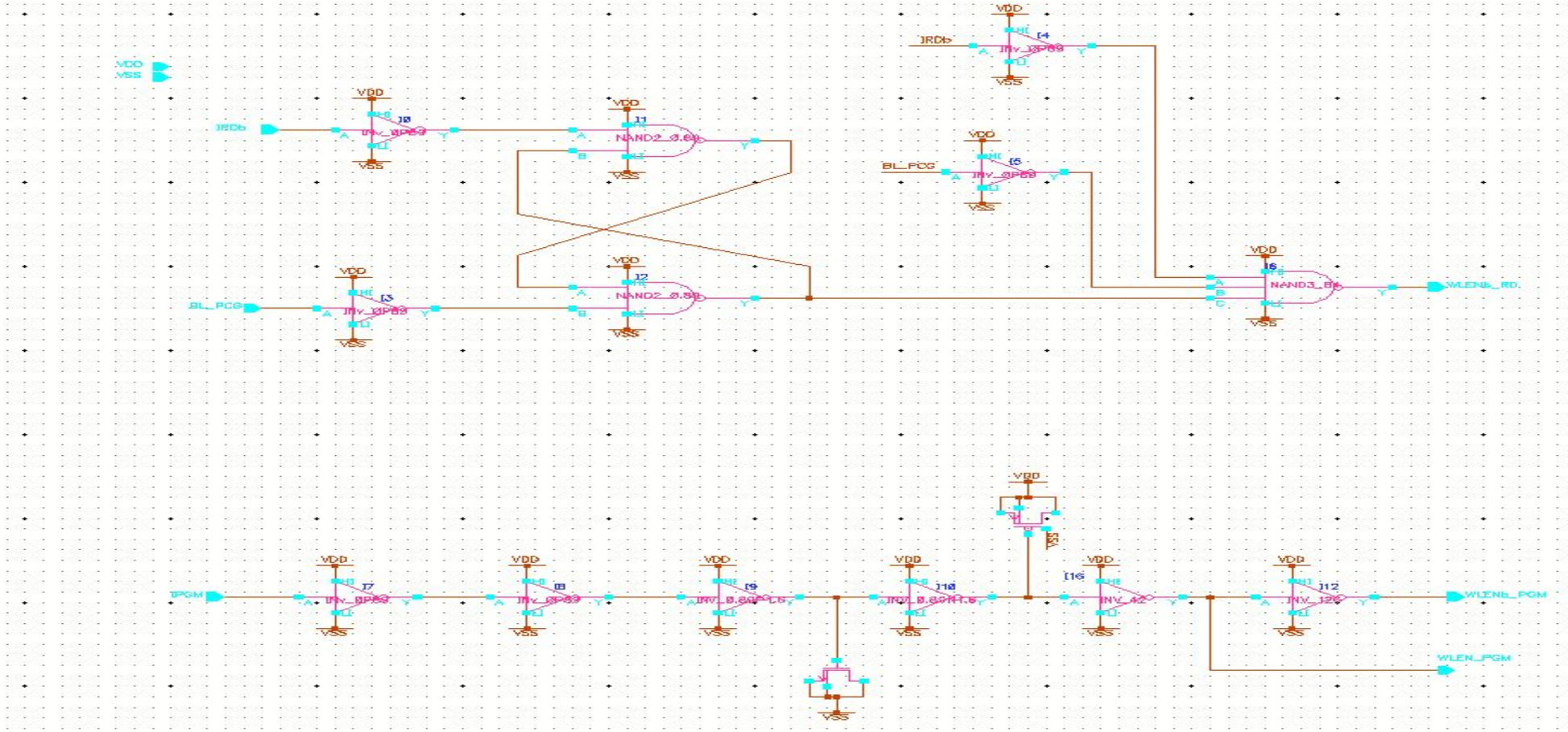
SAENb_Schematic

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic



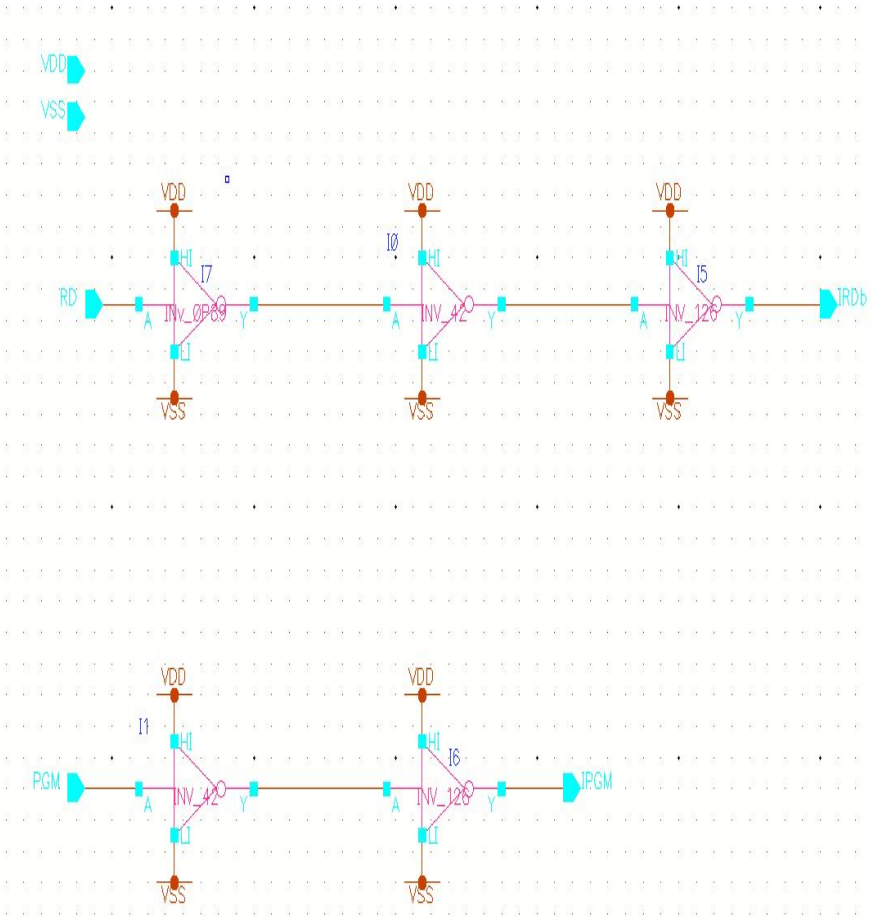
BL_PCG_Schematic

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic



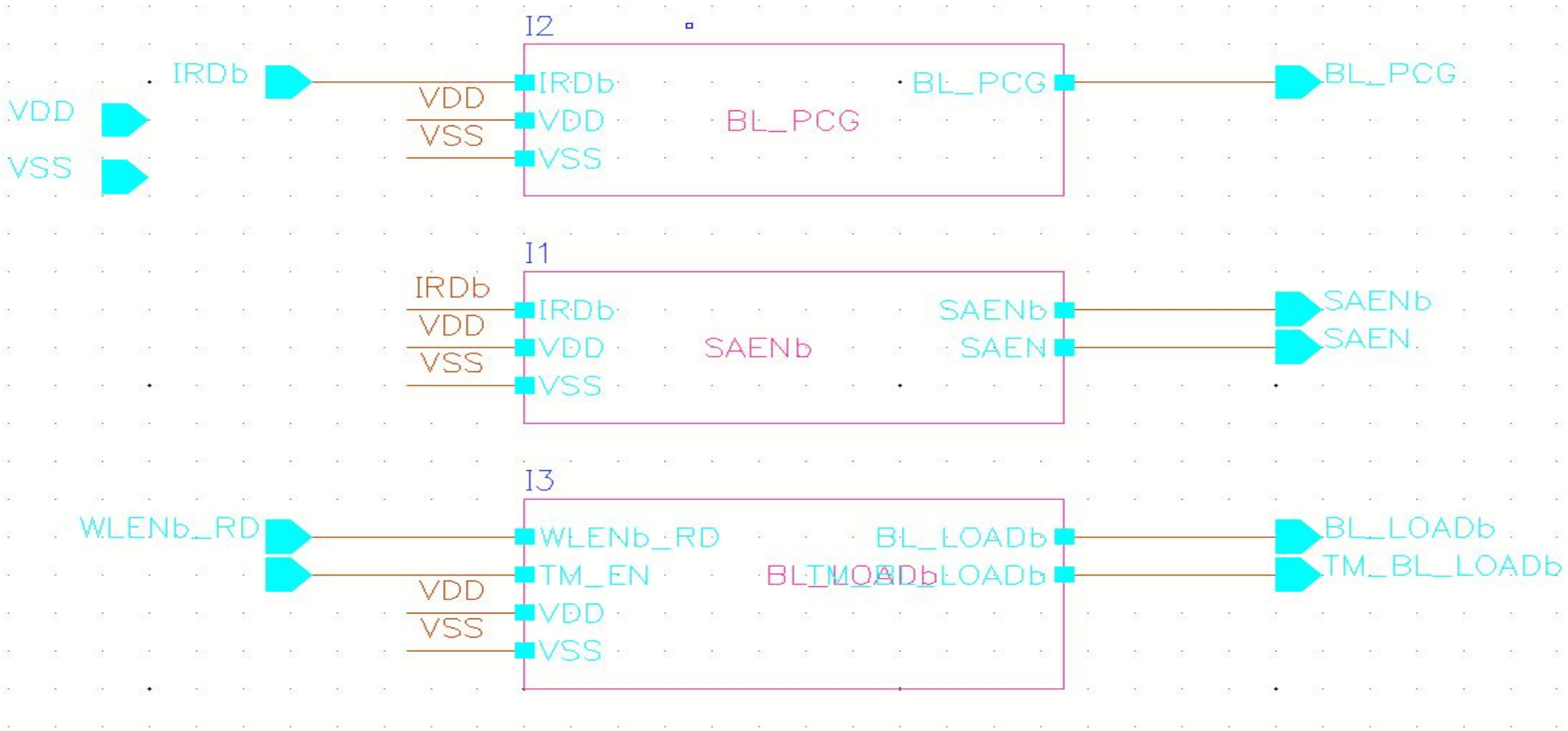
WL_CTRL_Schematic

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic



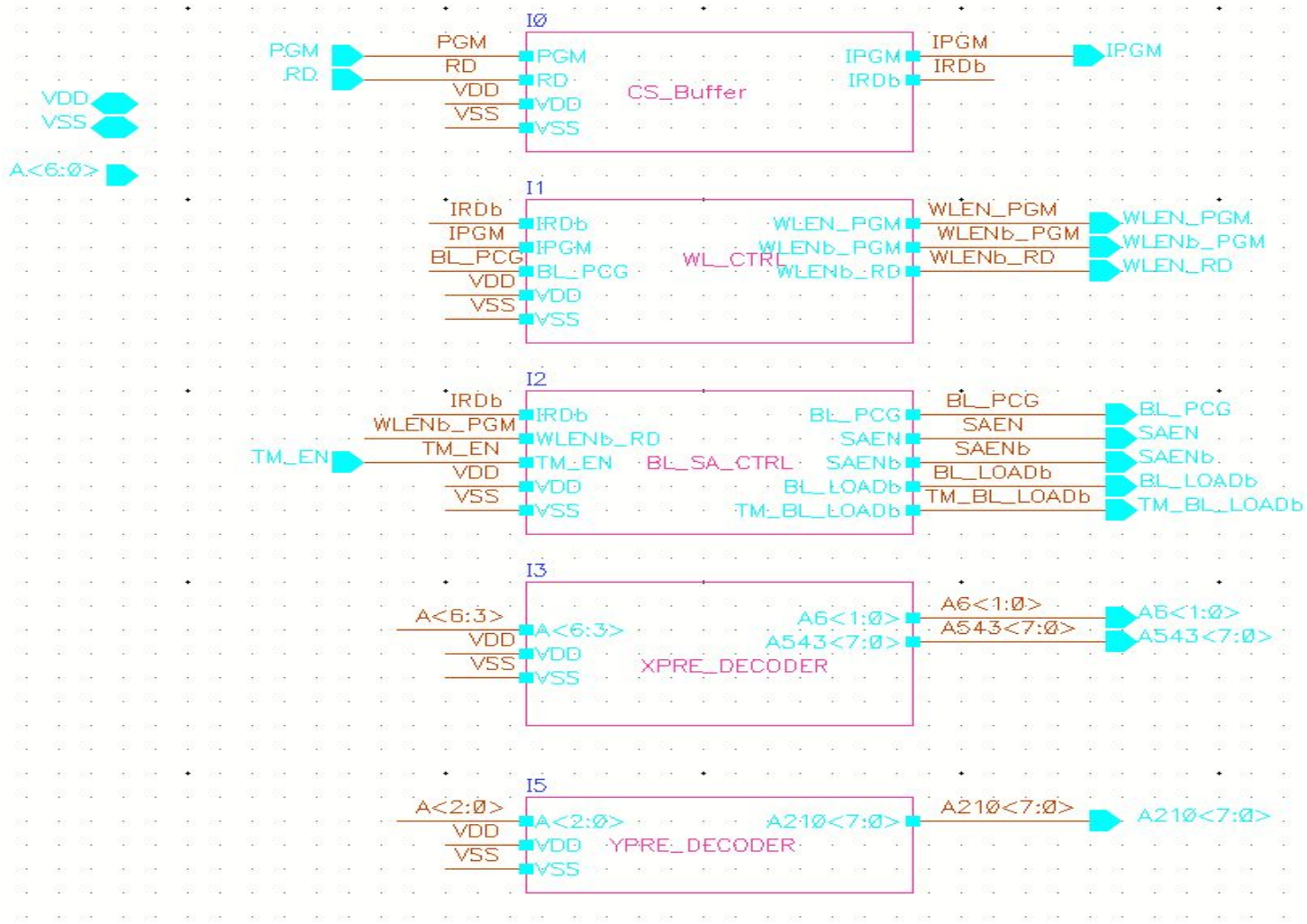
CS_Buffer_Schemati
c

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic



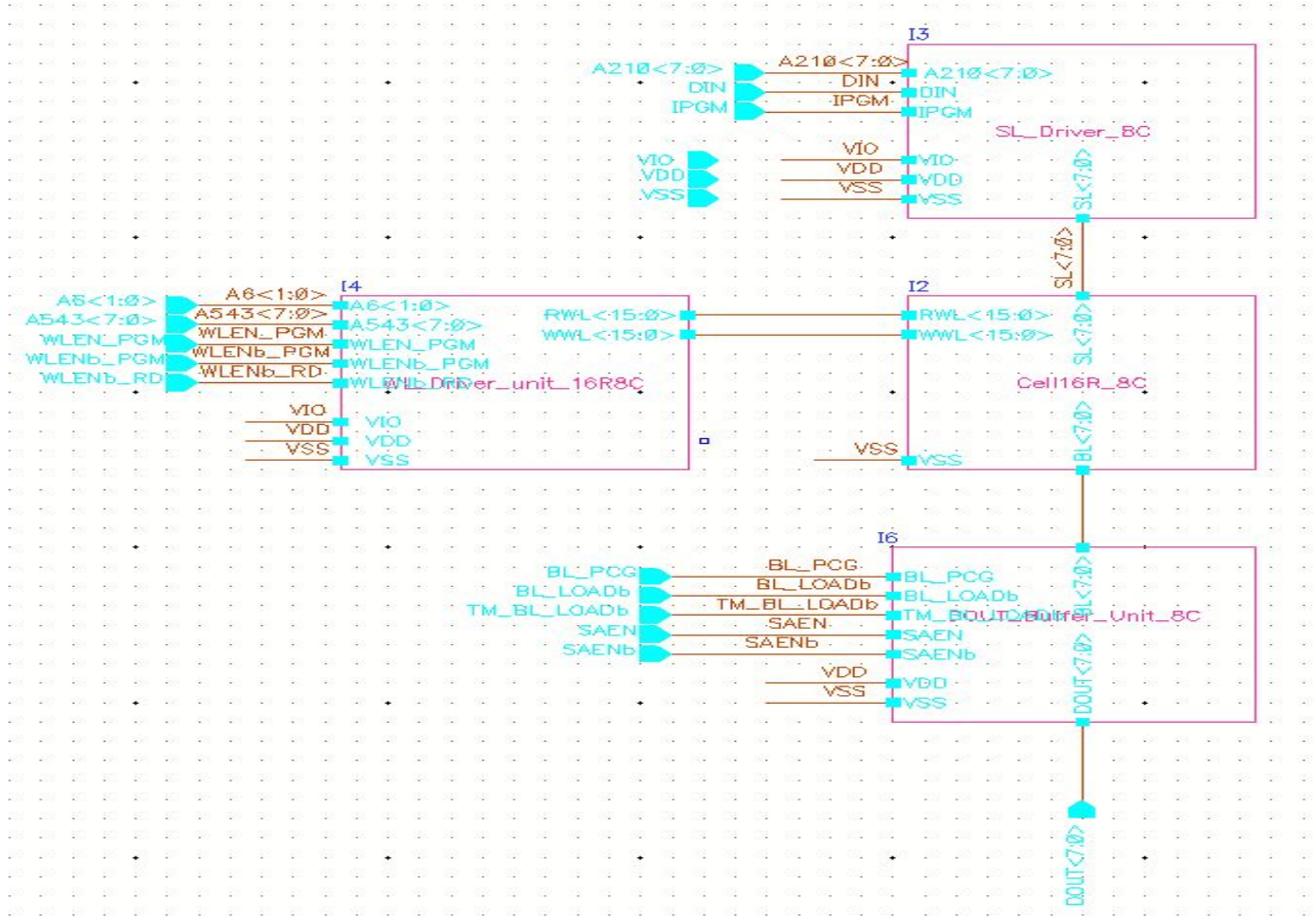
BL_SA_CTRL_Schematic

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic



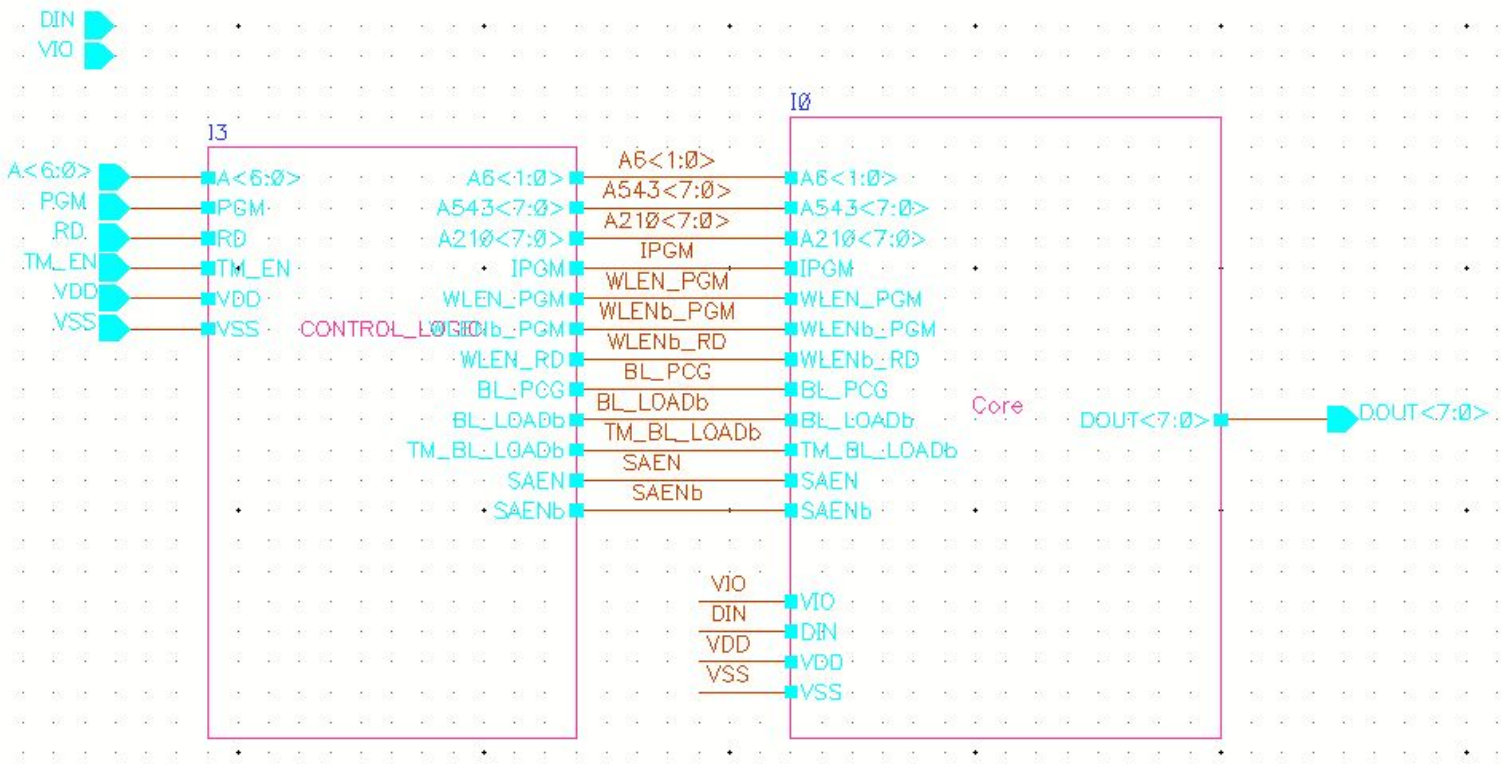
Control_Logic_Schematic

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic



Core_Schematic

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic



Top_Schematic

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic

Subject:128bit eFuse OTP IP design

- Problem statement :creating a convenable circuit that satisfied these specifications

– Supply voltage: VDD=2.2V – VIO=5.5VTemperature:–40C 25 C to 125C

- Operating Mode : Program/Program Verify–Read/ReadProgram.

  – ReadProgram Verify:10k
  – Read Mode :5k {Read_Programmed Cell& Read_Uprogrammed Cell
  – Current :<100uA. (Decreasing current from 168.4uA to 100uA

- Expected result: Suitable block diagram have to be find out by modifying the above simulation circuits based on the requirements.

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic

Simulation software :CX-HSPUI -Xftp5 -Crimson Editor

Design & Layout software :VLSI7(VLSI7:177) -Xmanager5[:0.0]

DBHitek 180nm BCD Process
eFuse Cell Array _Simulation_Schematic