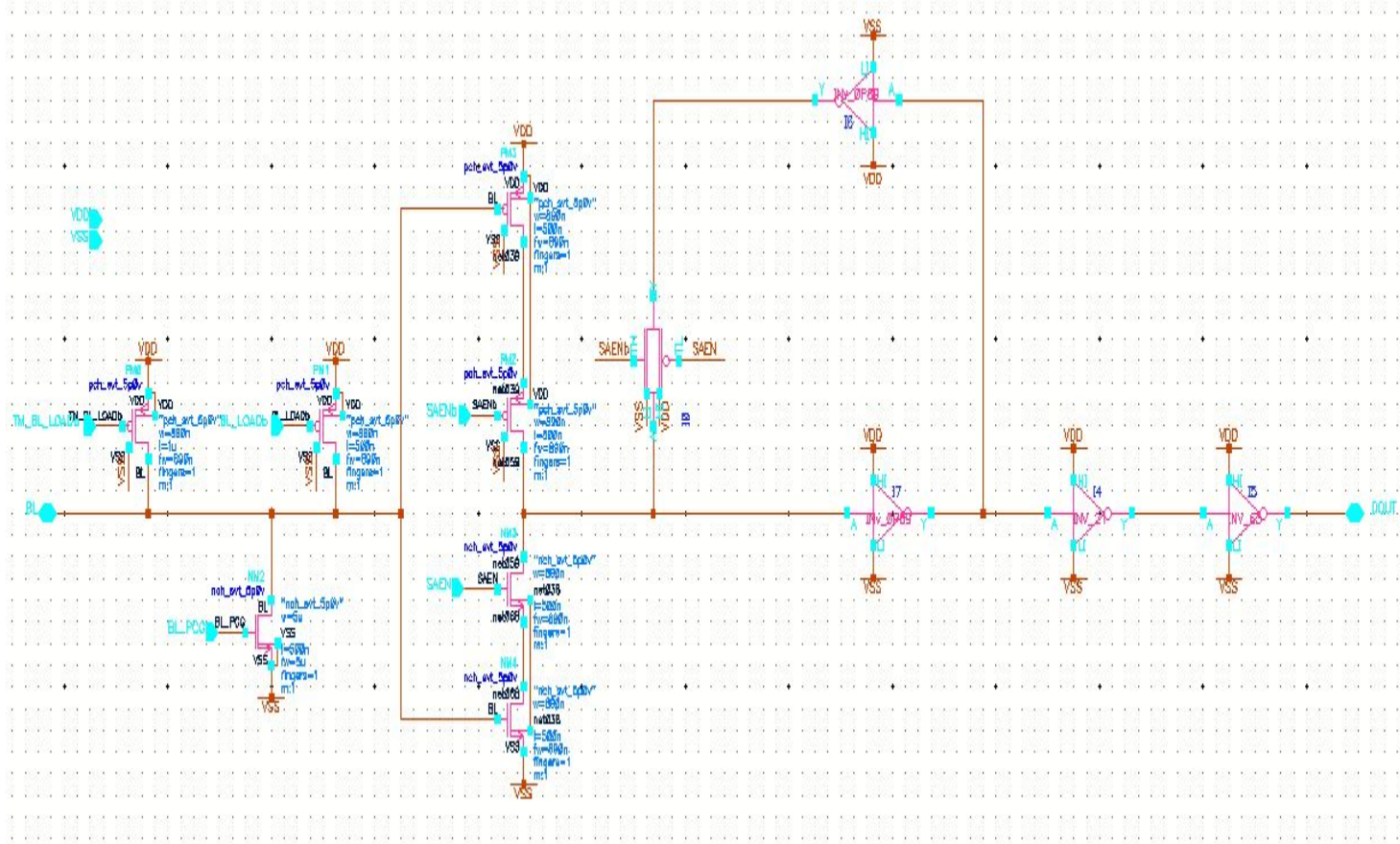
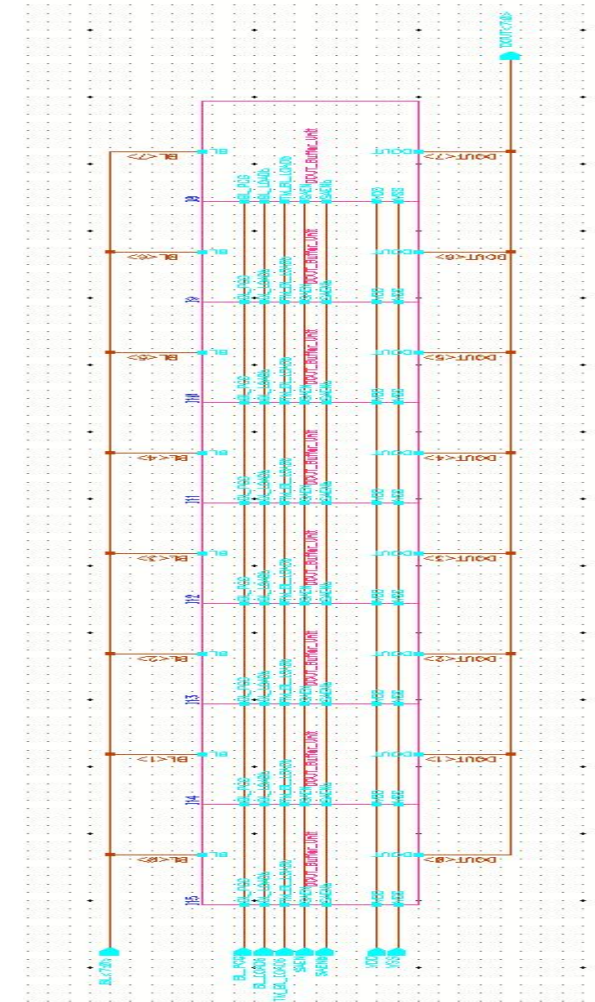


# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic

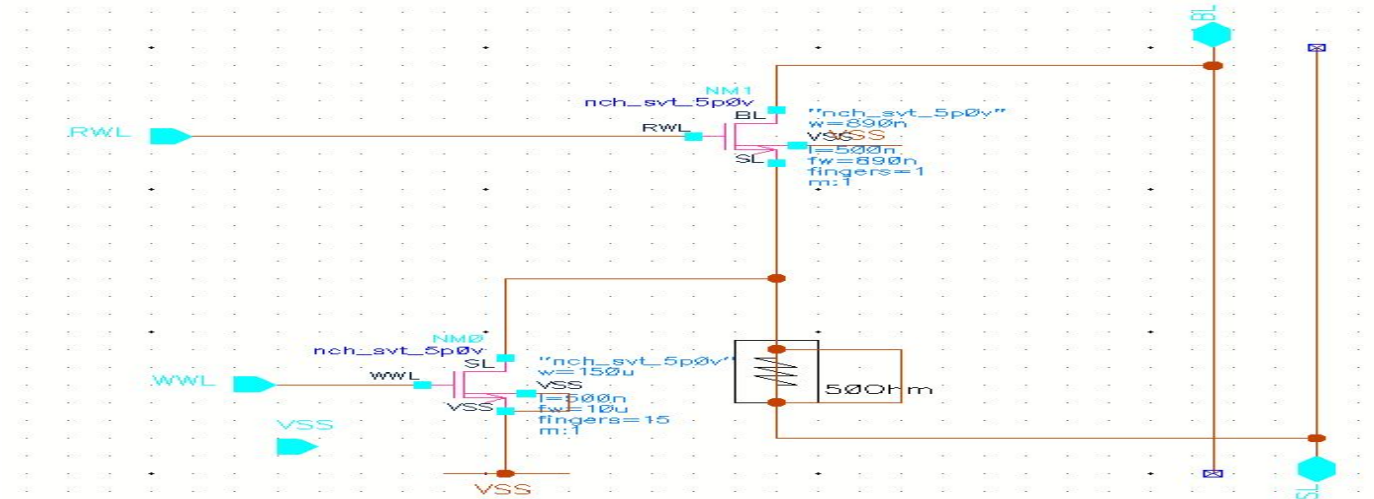


DOUT\_Buffer\_Unit  
\_Schematic

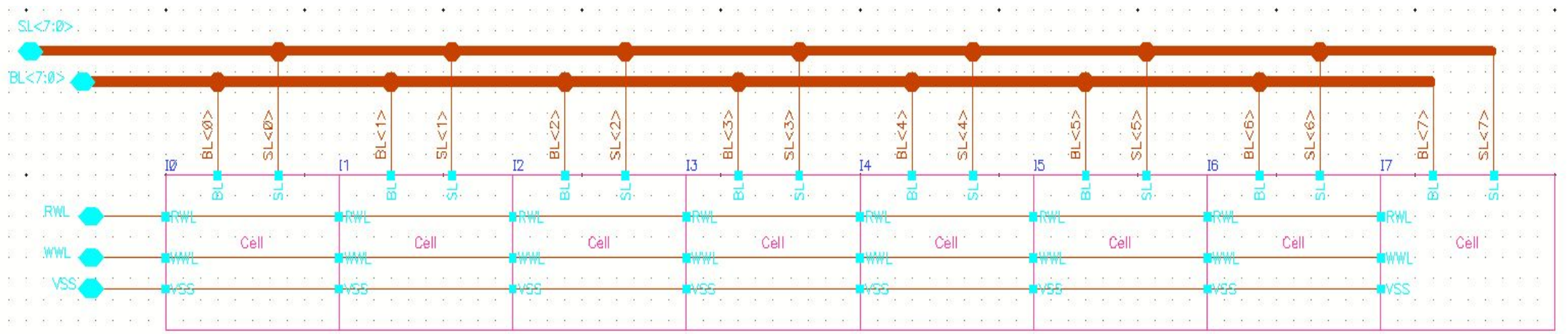


DOUT\_Buffer\_Unit\_8C\_Schematic

# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic

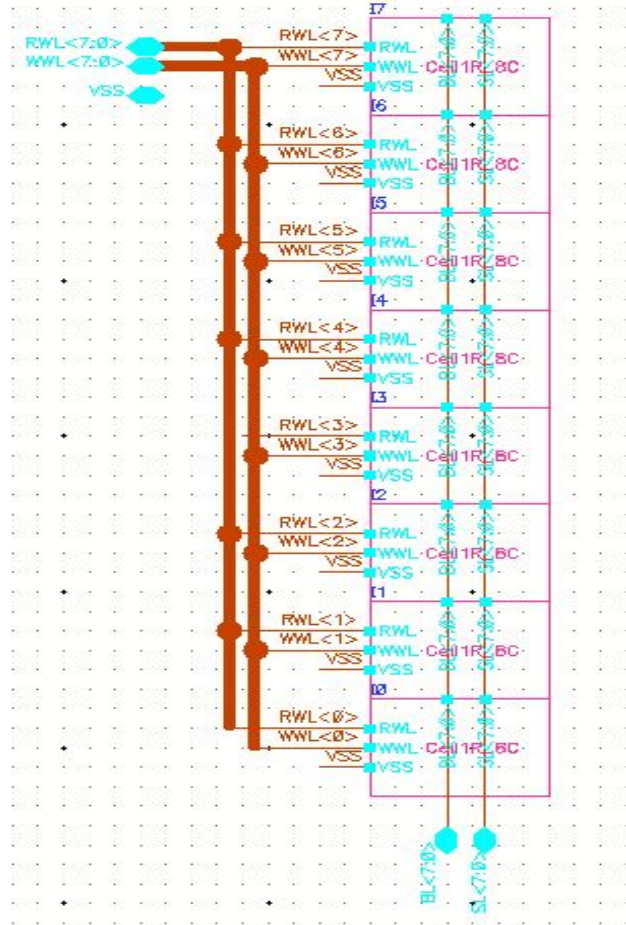


Cell\_Schematic

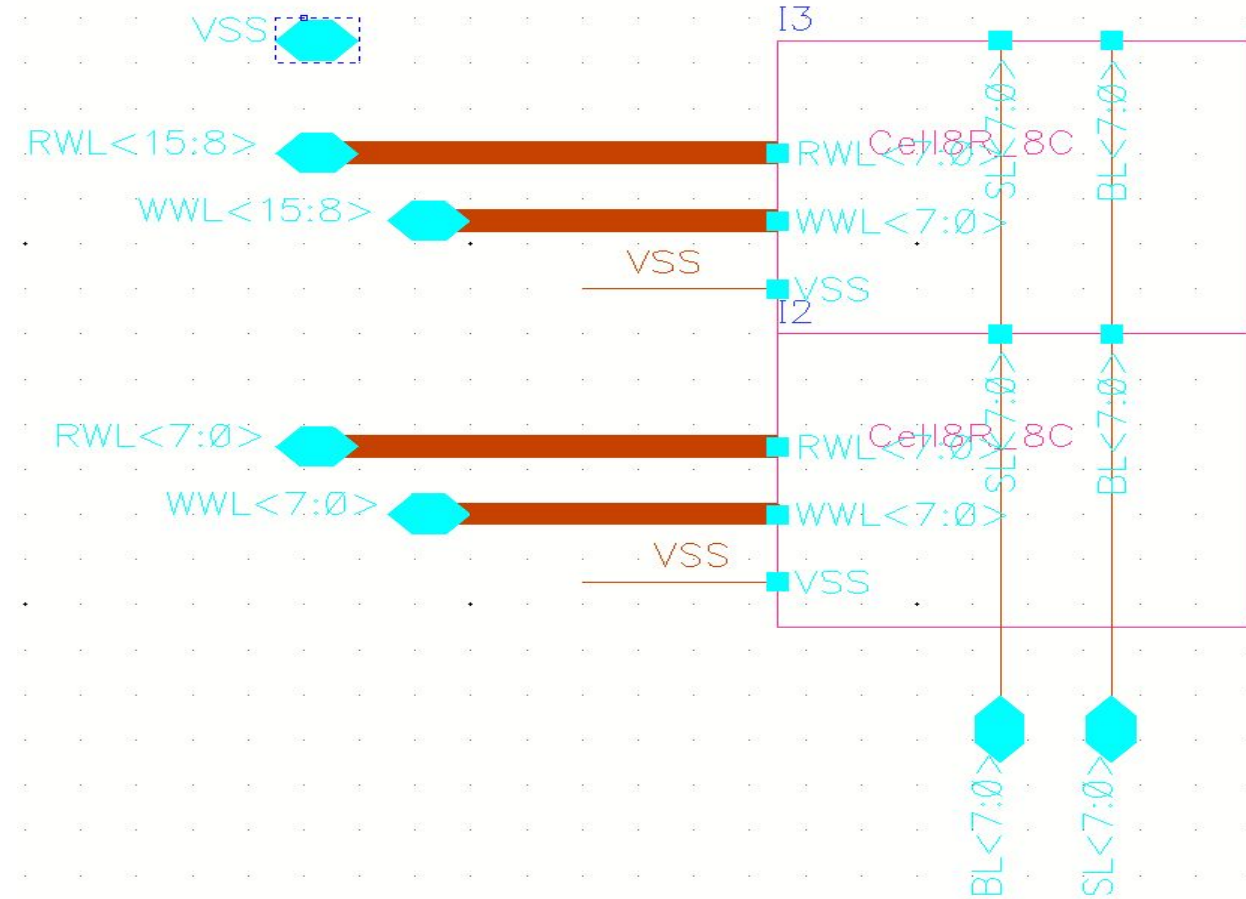


Cell1R\_8C\_Schematic

# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic



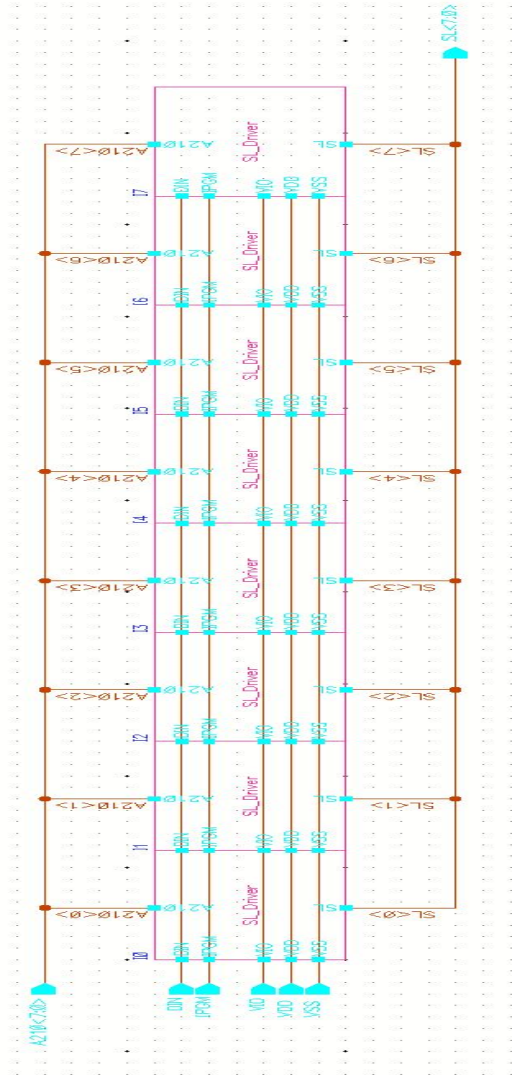
Cell8R\_8C\_Schematic



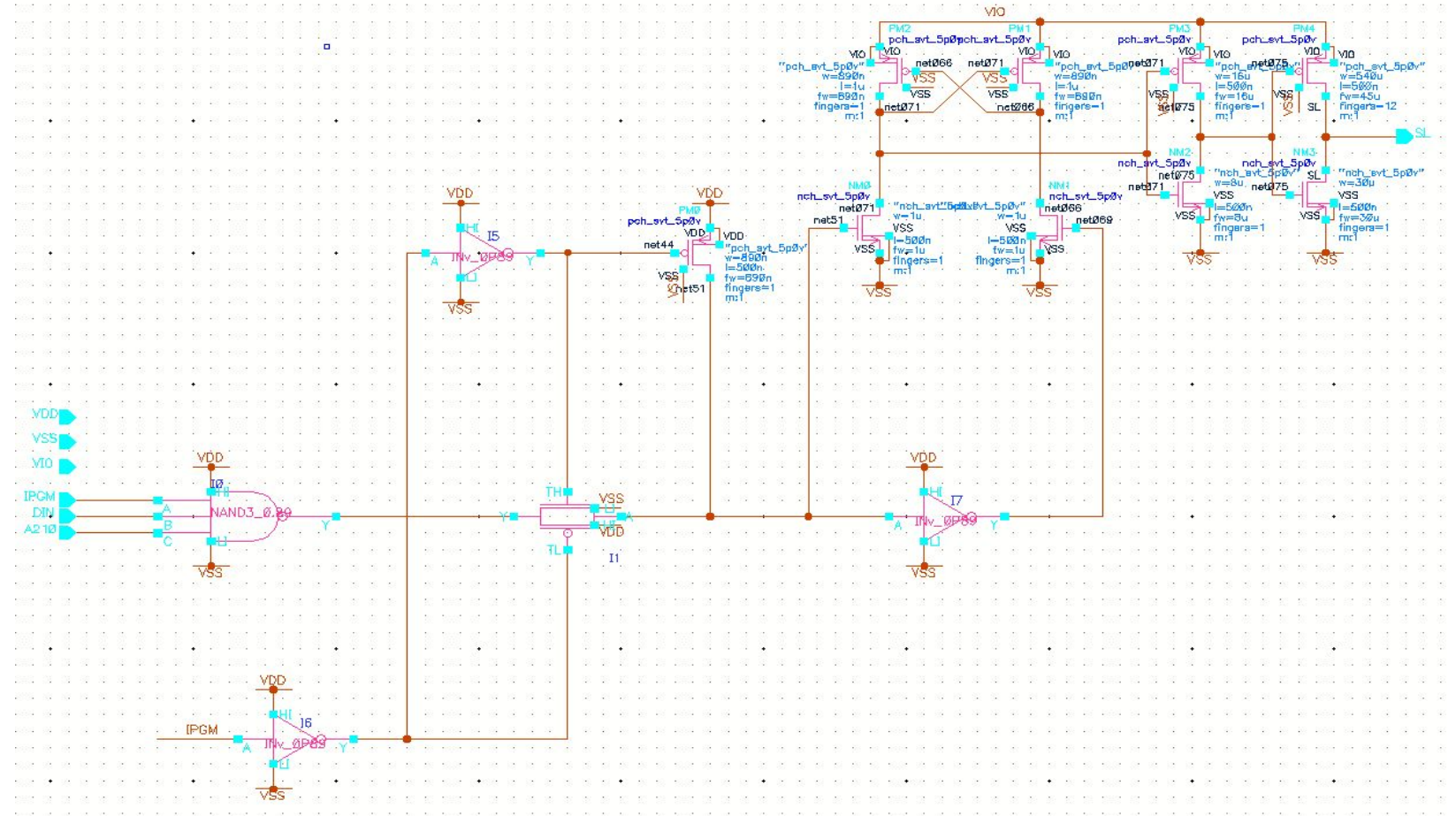
Cell16R\_8C\_Schematic



# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic



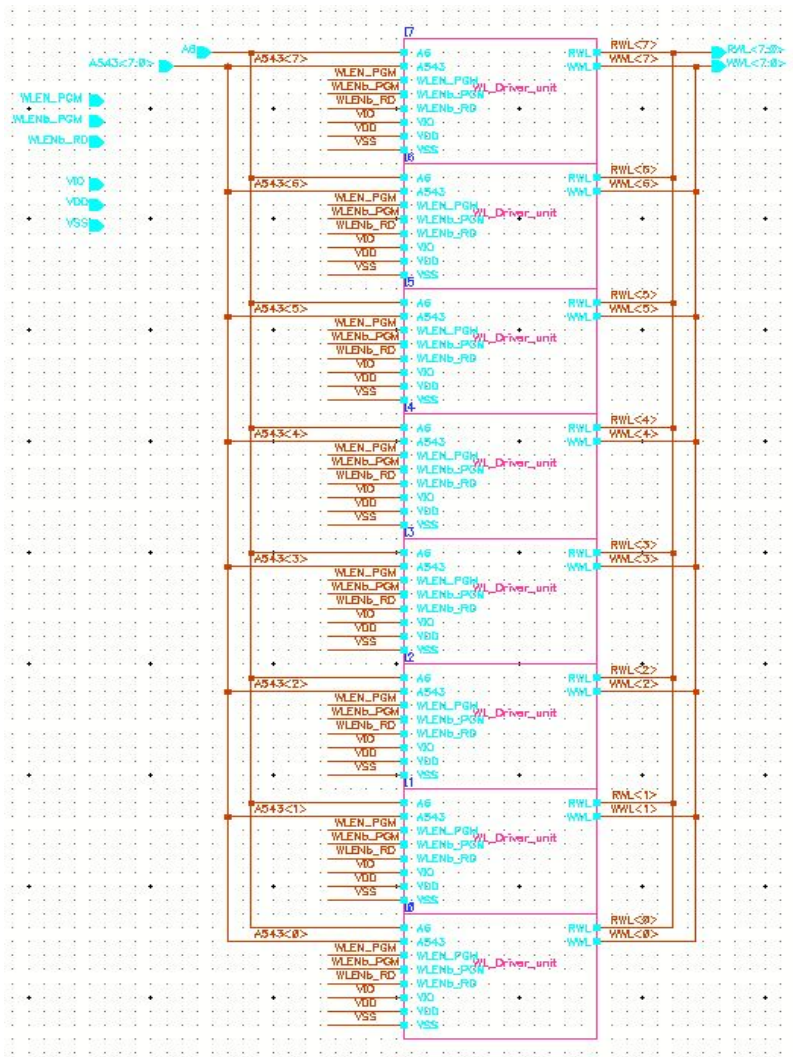
SL\_Driver\_8C\_Schematic



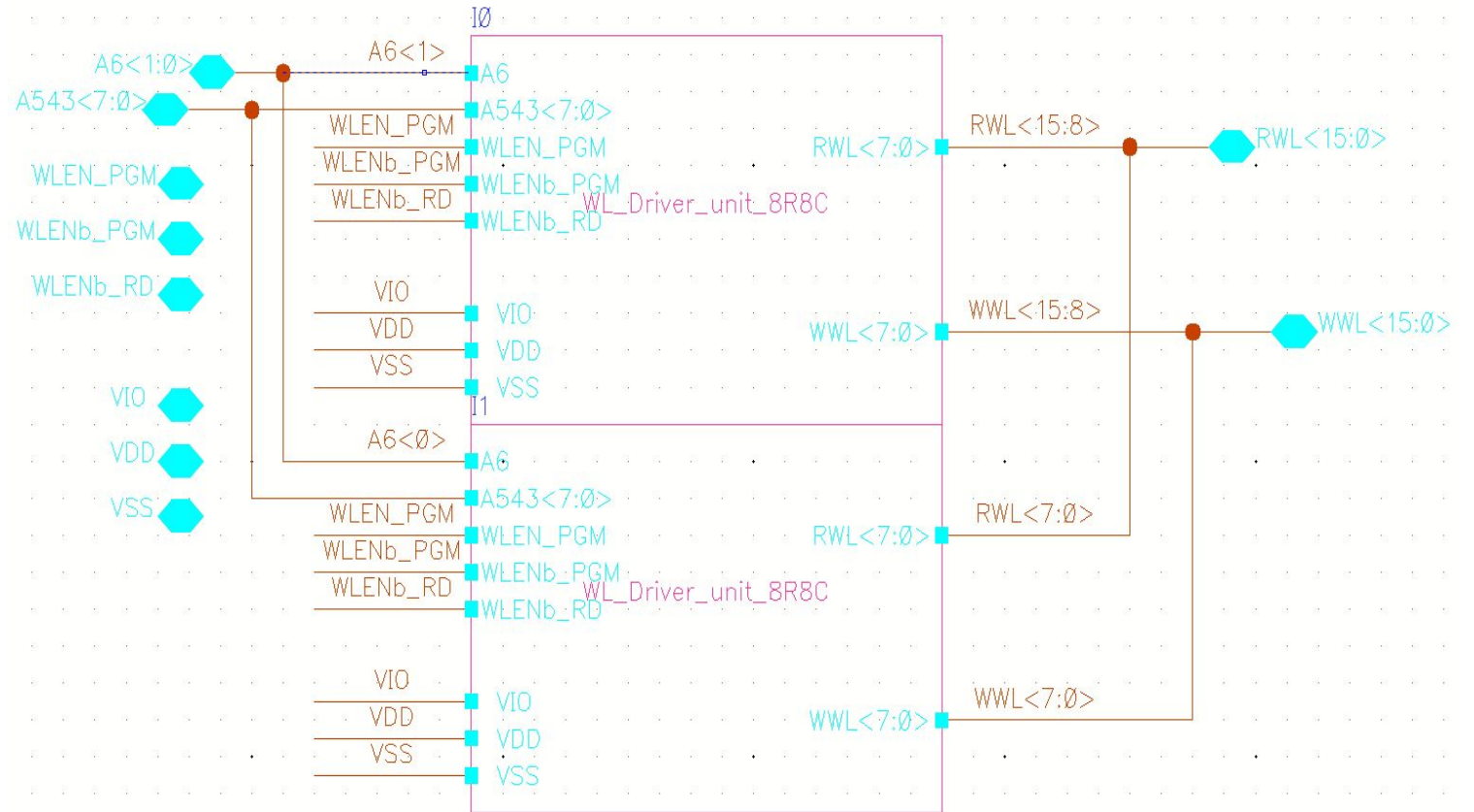
SL\_Driver\_Schematic



# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_ Schematic



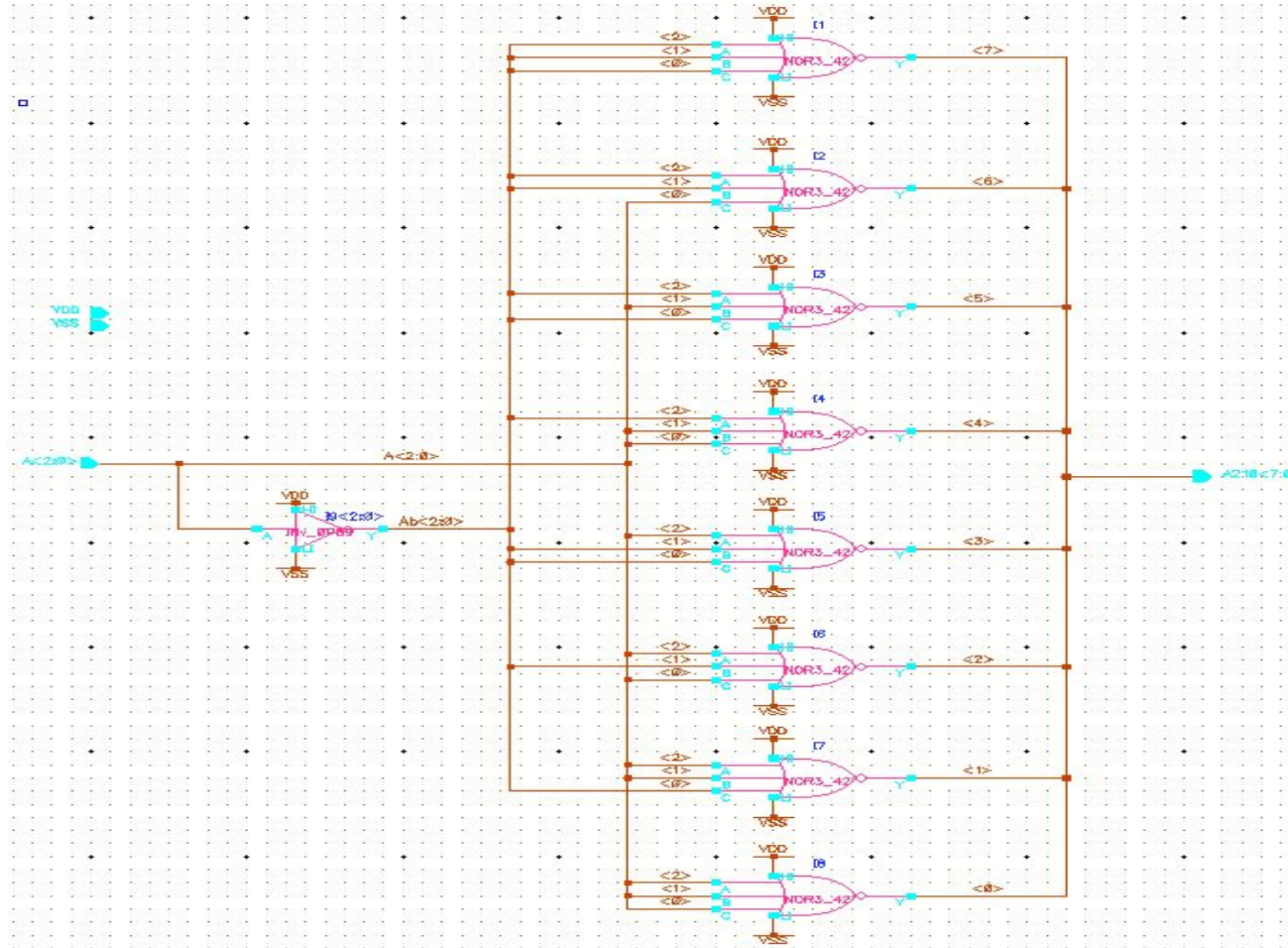
WL\_Driver\_Unit\_1R8C



WL\_Driver\_Unit\_8R8C

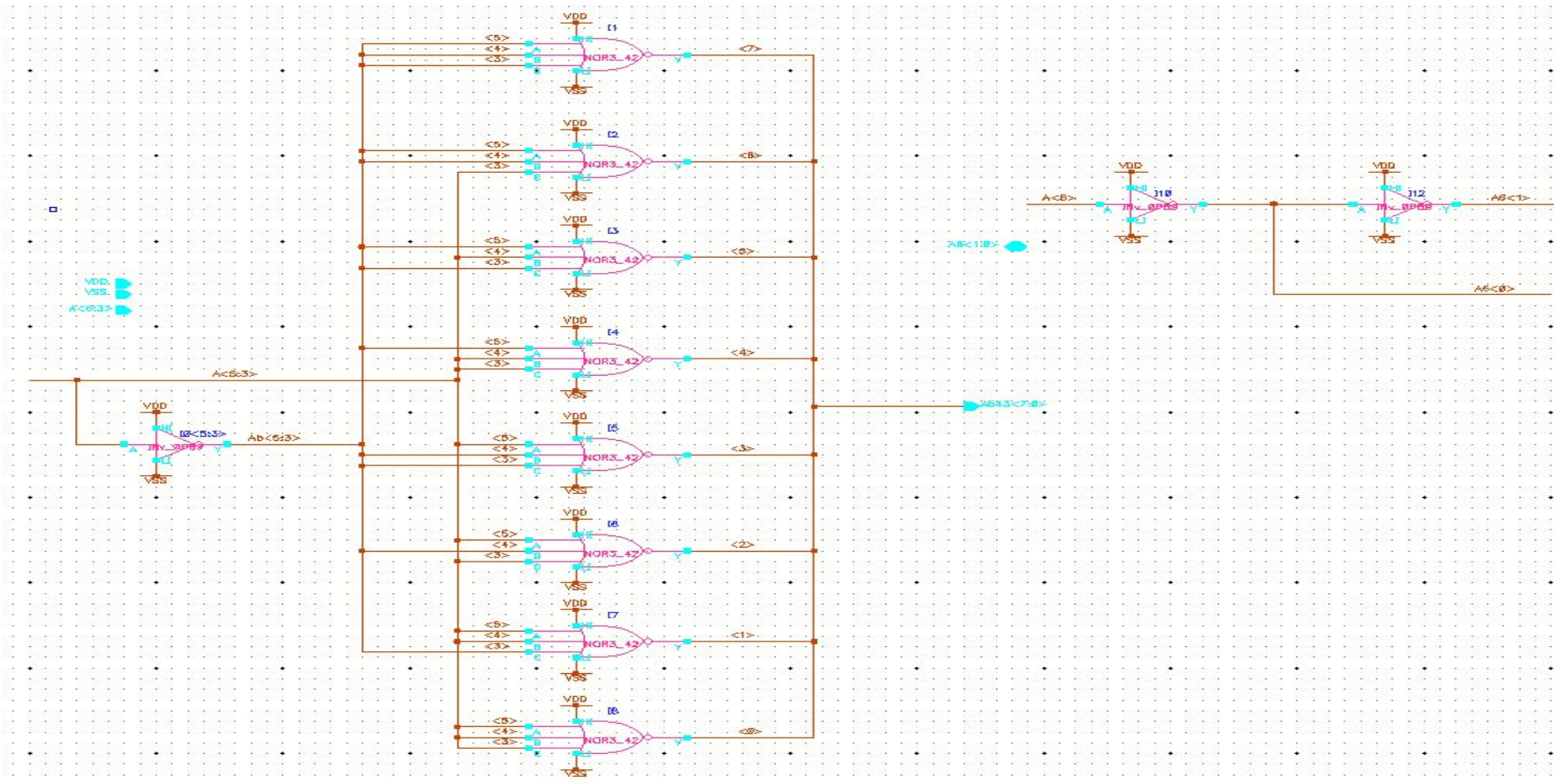


# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic



Ypre\_Decoder\_Schematic  
c

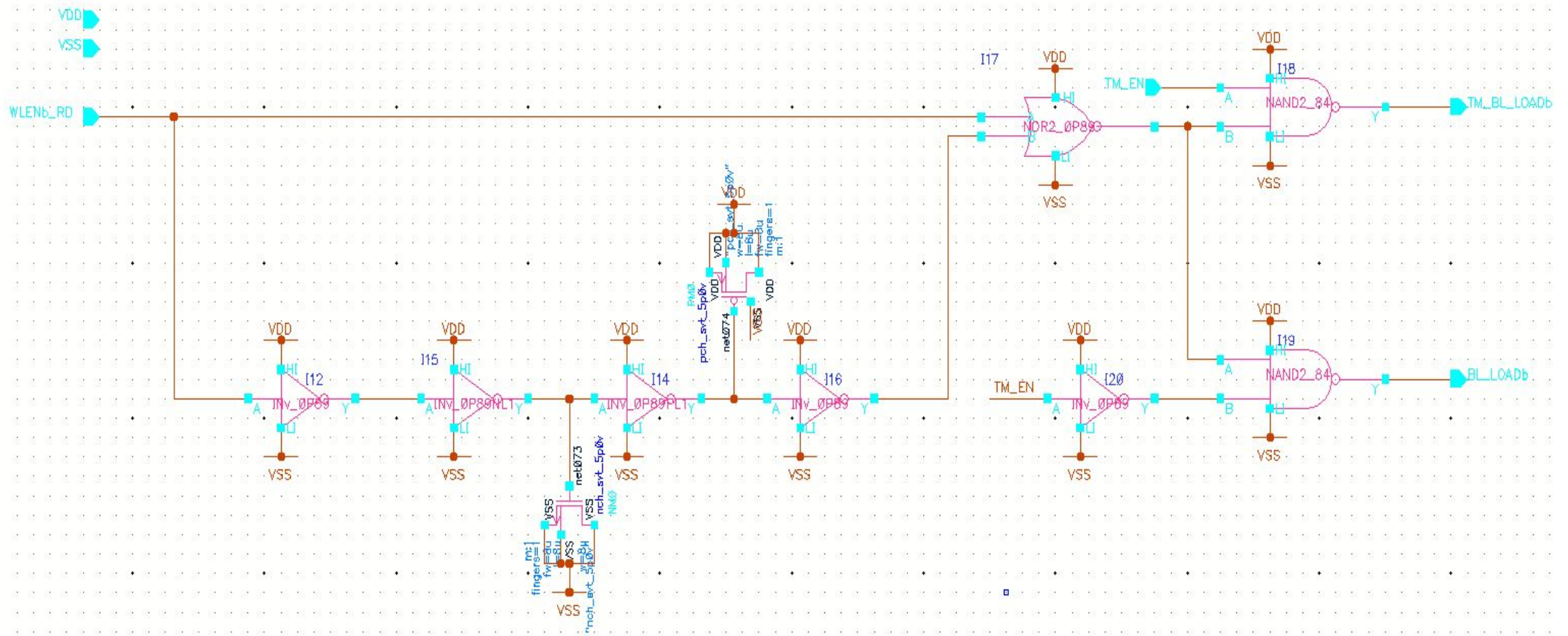
# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic



Xpre\_Decoder\_Schemati  
c

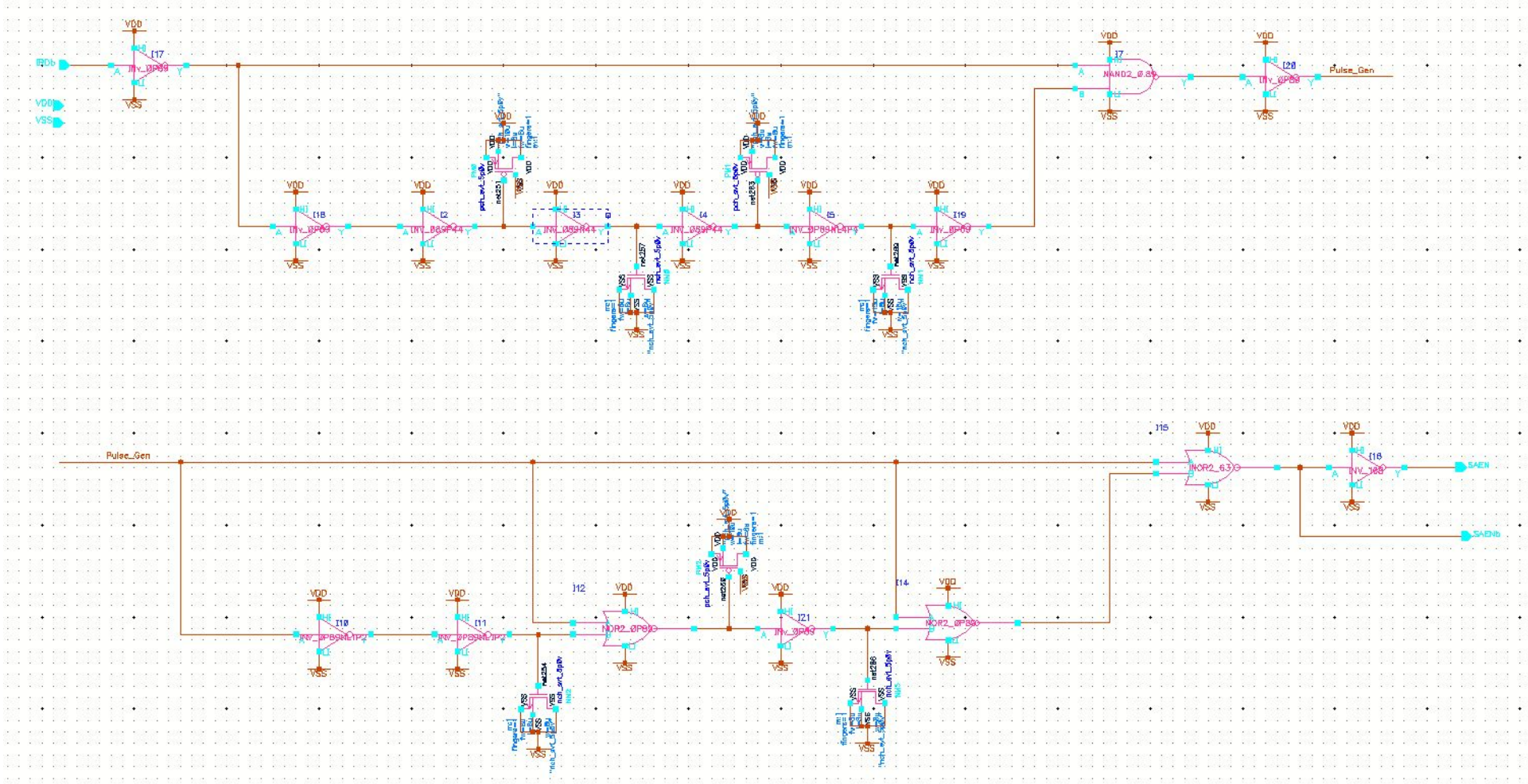


# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic



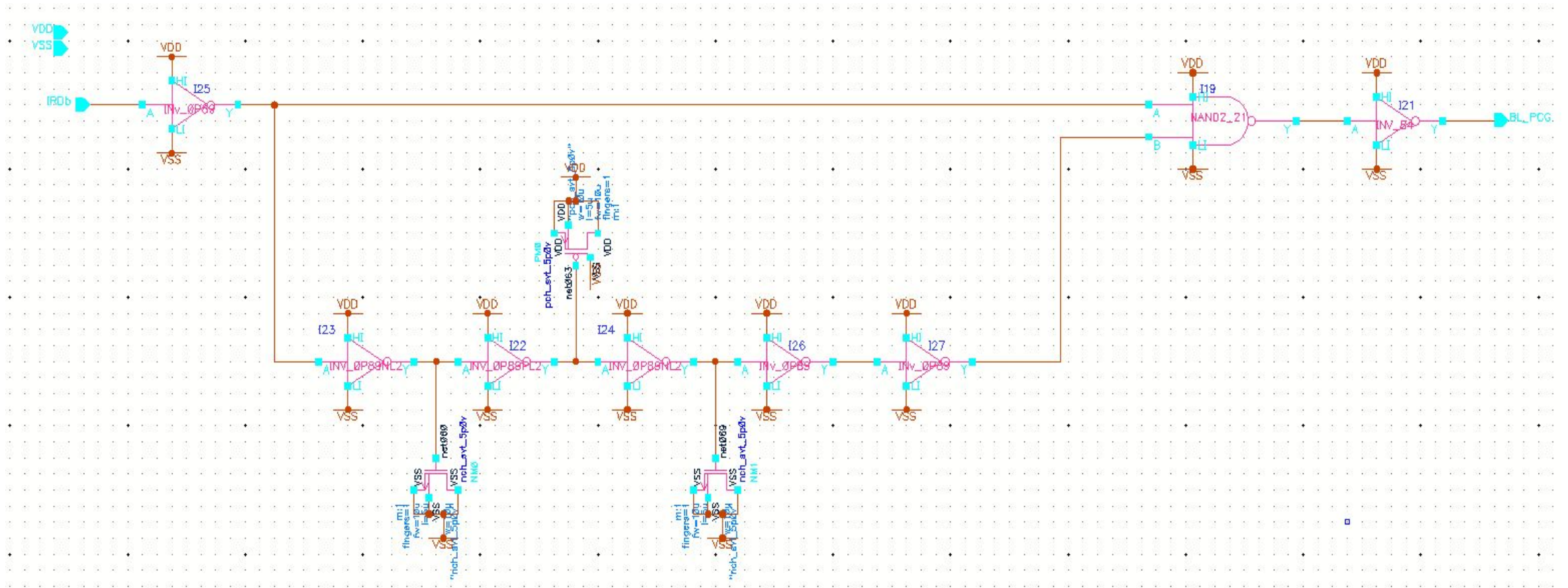
BL\_LoADb\_Schemati  
C

# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic



SAENb\_Schematic

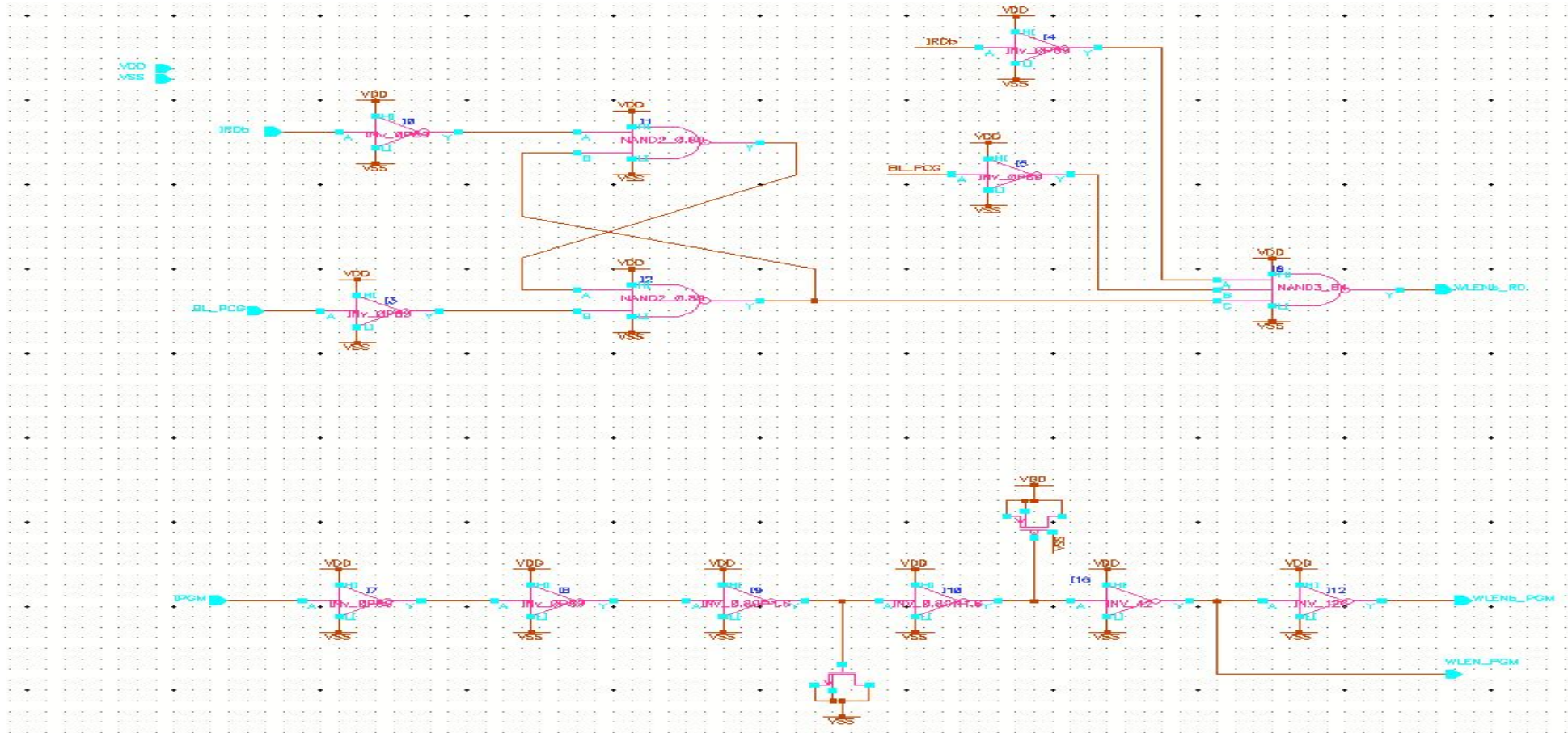
# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic



BL\_PCG\_Schematic

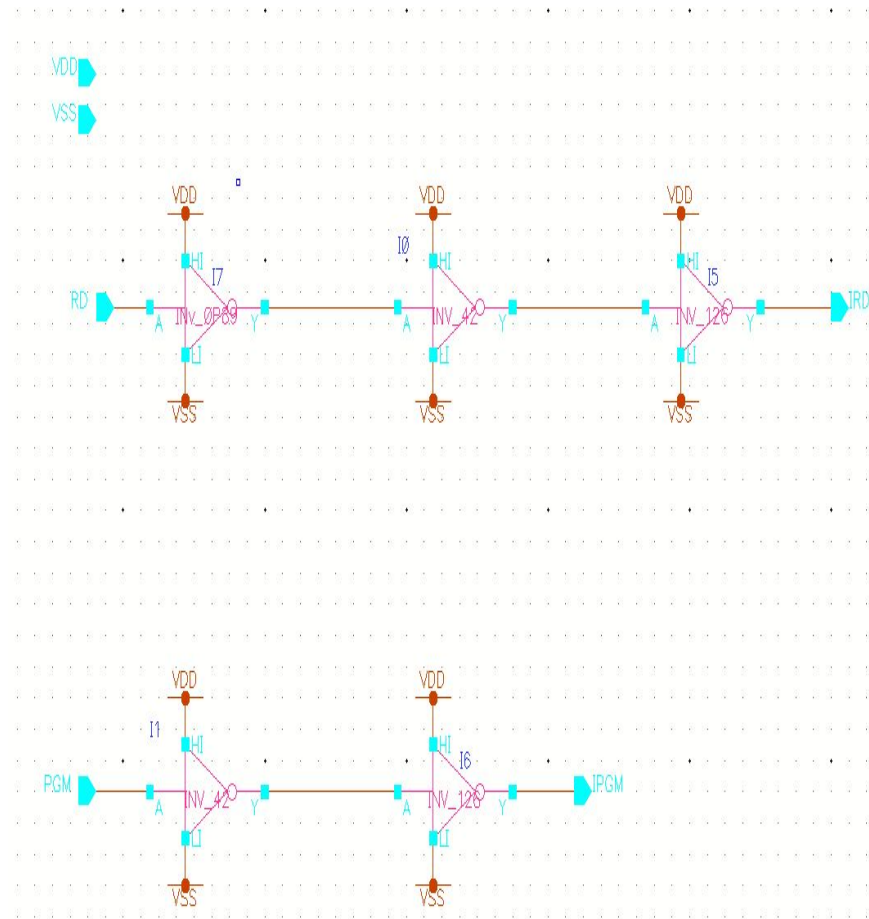


# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic



WL\_CTRL\_Schematic

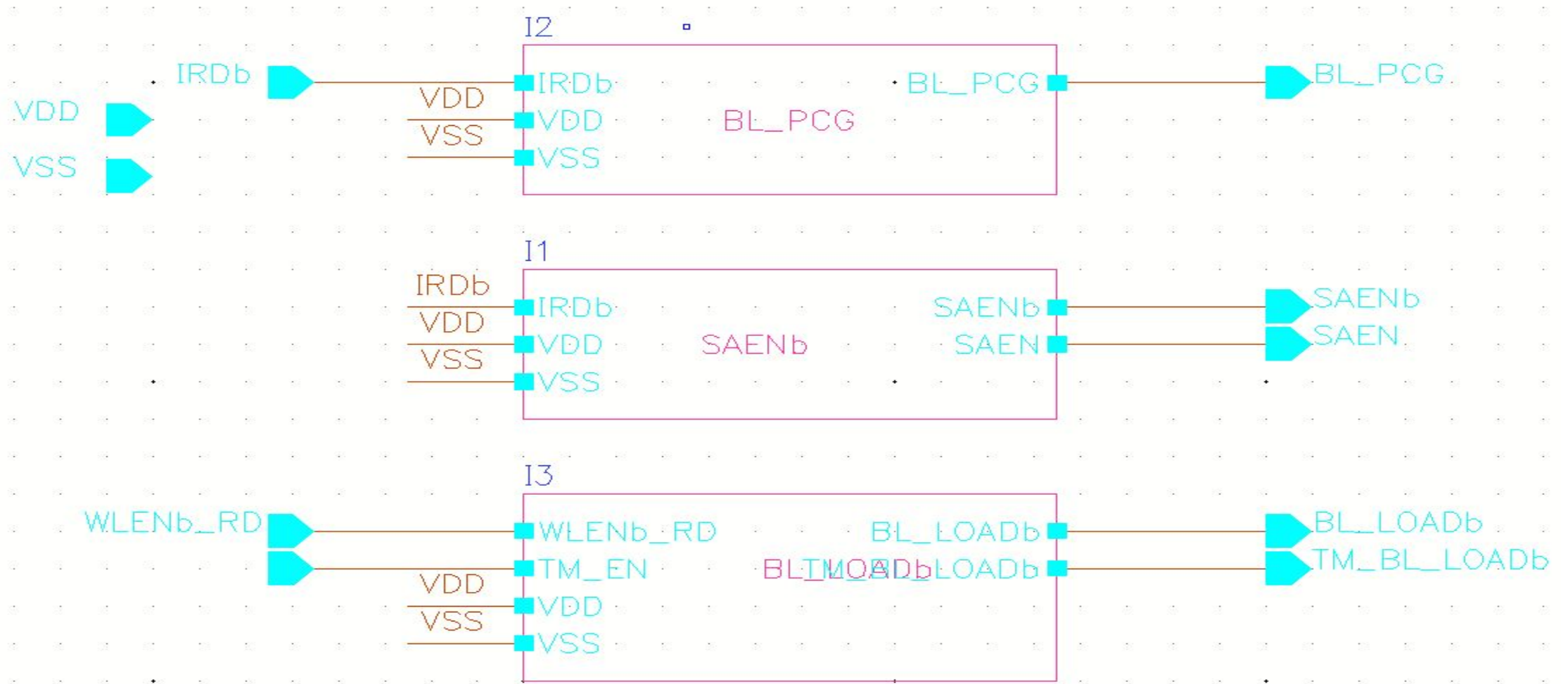
# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic



CS\_Buffer\_Schemati

c

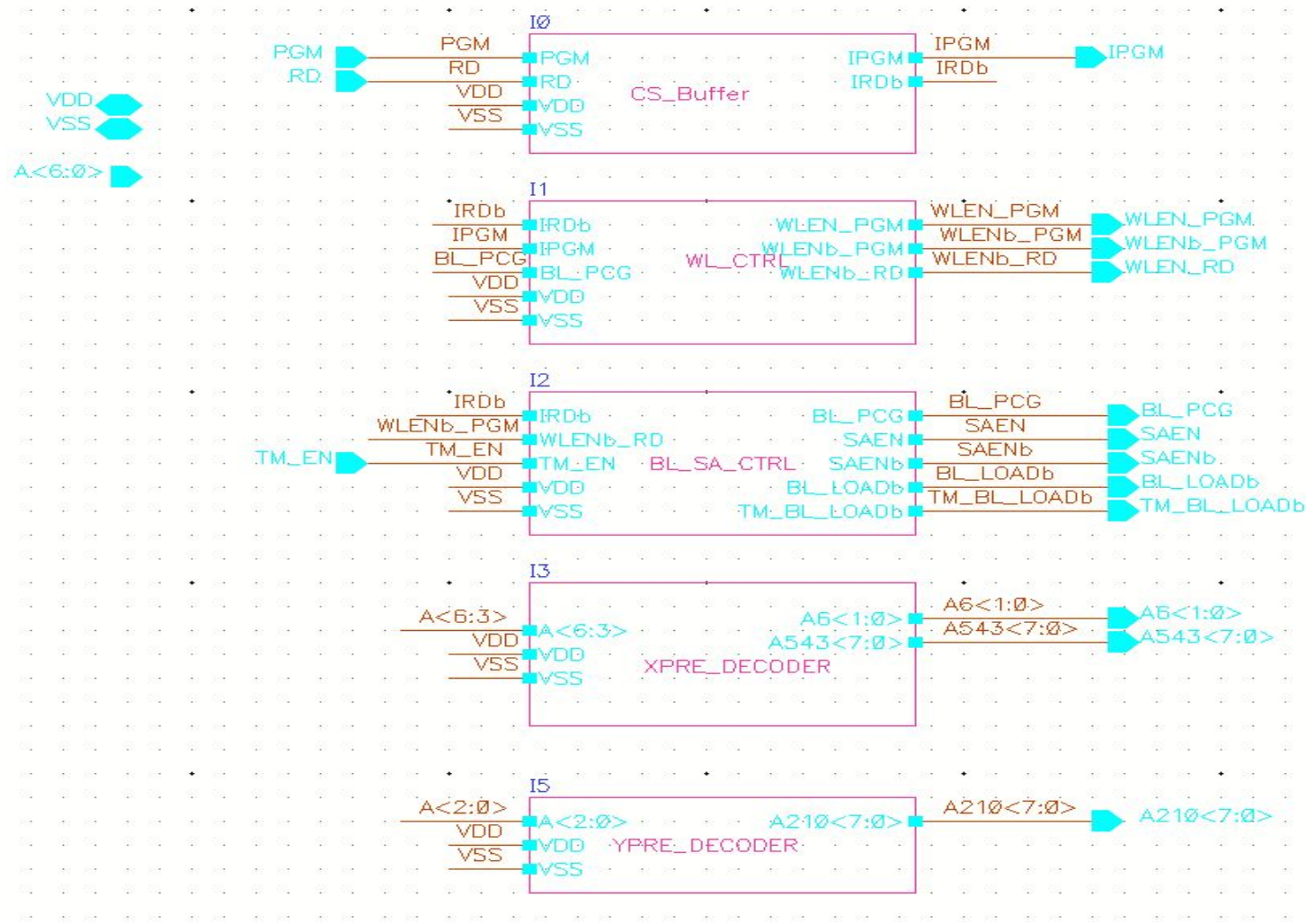
# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic



BL\_SA\_CTRL\_Schematic

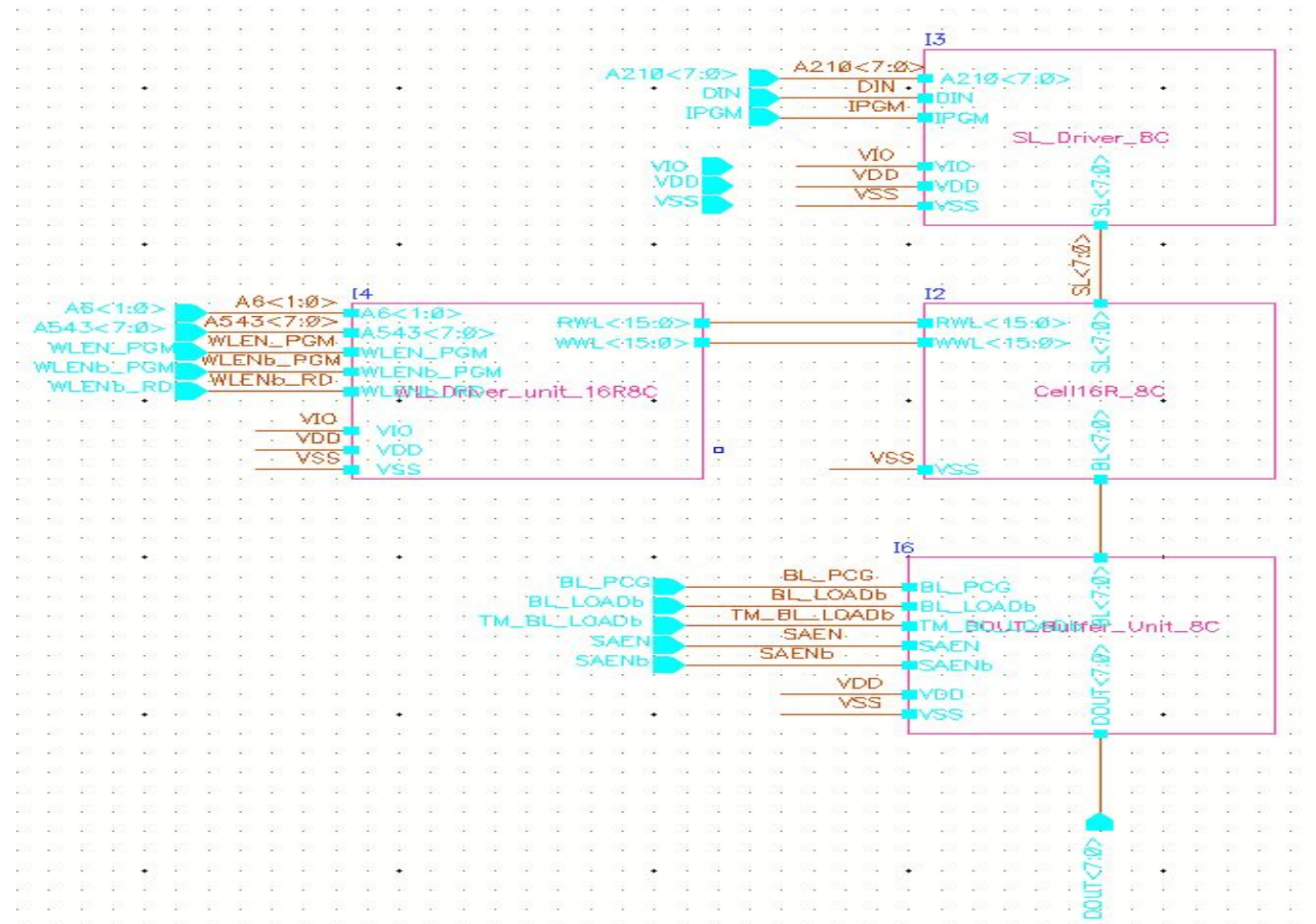


# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic



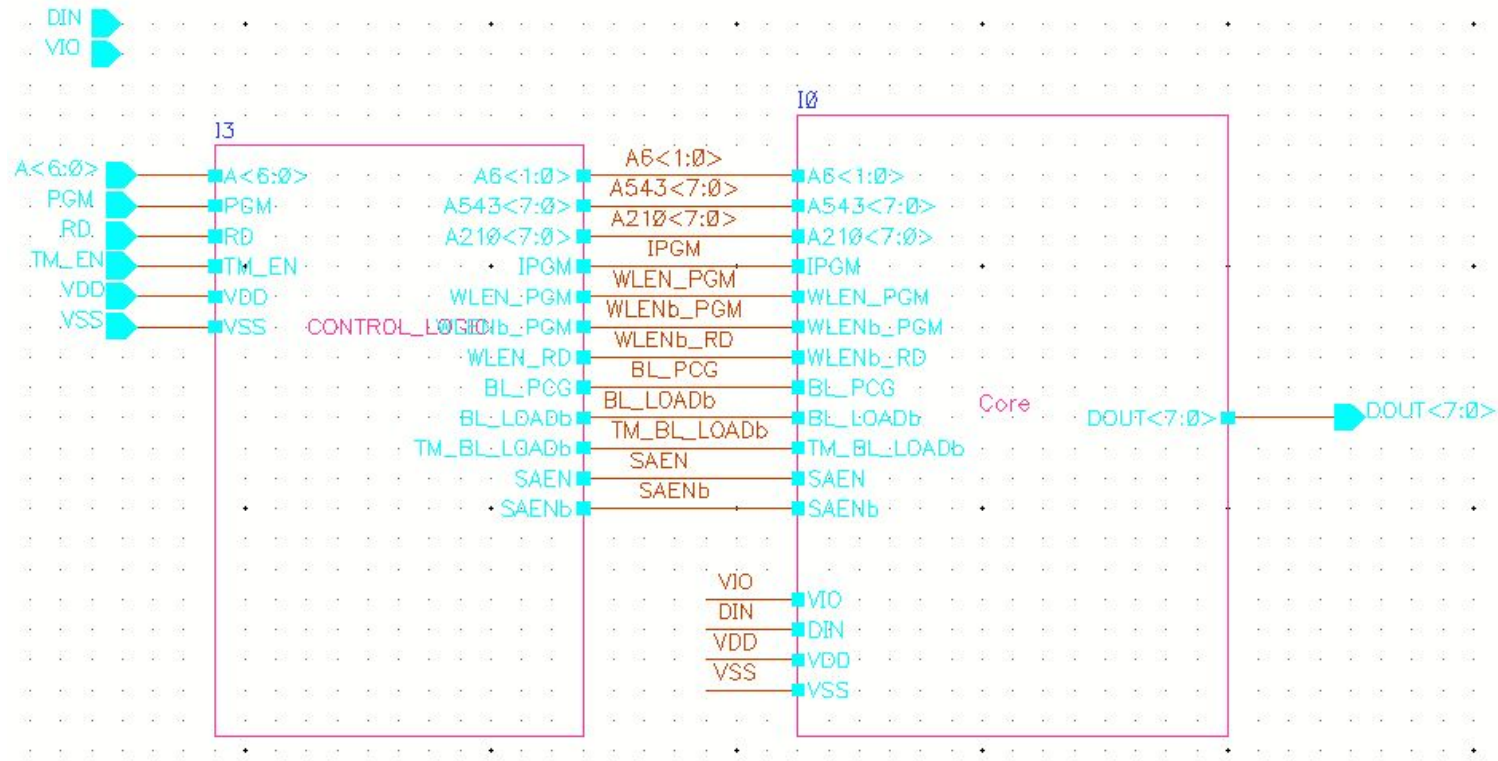
Control\_Logic\_Schematic

# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic



Core\_Schematic

# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic



Top\_Schematic



# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic

Subject: 128bit eFuse OTP IP design

□ **Problem statement**: creating a convenient circuit that satisfied these specifications

– Supply voltage: VDD=2.2V – VIO=5.5V Temperature: -40C 25 C to 125C

□ **Operating Mode** : Program/Program Verify–Read/ReadProgram.

– ReadProgram Verify: 10k

– Read Mode : 5k {Read\_Programmed Cell & Read\_Uprogrammed Cell

– Current : <100uA. (Decreasing current from 168.4uA to 100uA)

□ **Expected result**: Suitable block diagram have to be find out by modifying the above simulation circuits based on the requirements.

# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic

Simulation software : [CX-HSPUI](#) -Xftp5 -Crimson Editor

Design & Layout software : [VLSI7\(VLSI7:177\)](#) -Xmanager5[:0.0]



# DBHitek 180nm BCD Process eFuse Cell Array \_Simulation\_Schematic

**eFuse OTP**

VDD	Temp	Program-Verify-Read Mode					Read Mode				
		SS model	SF model	TT model	FS model	FF model	SS model	SF model	TT model	FS model	FF model
4.5V	-40°C	7.2K	6.8K	7.3K	7.6K	6.9K	3.1K	3.3K	3.7K	4.1K	3.8K
	25°C	9.1K	8.6K	8.9K	9.2K	9.4K	4.3K	4.4K	4.6K	4.8K	4.8K
	125°C	10K	9.3K	9.7K	9.9K	9K	3.9K	4.3K	4.8K	5K	4.8K
5V	-40°C	5.5K	5.6K	6K	6.2K	5.9K	1.9K	2.4K	2.8K	3K	3.1K
	25°C	7.1K	7.2K	7.5K	7.7K	7K	2.9K	3.4K	3.7K	3.9K	3.9K
	125°C	7.6K	7.7K	7.9K	8.1K	7.4K	2.6K	3.2K	3.4K	3.7K	3.7K
3.3V	-40°C	4.4K	4.8K	5K	5.2K	5.1K	0.9K	1.5K	2.1K	2.2K	2.6K
	25°C	5.9K	6.2K	6.3K	6.5K	6.3K	2K	2.7K	3K	3.1K	3.3K
	125°C	6.1K	6.5K	6.6K	6.7K	6.5K	1.4K	2.4K	2.6K	2.7K	2.8K