

# 2012 Component Training Ivy Platform Series

**GRMA Brain\_HUNG**

# Ivy 7 Series – Agenda

- **Platform Structure**
  - CPU feature introduce
  - Intel 7 series chipset architecture
- **Critical Power Flow**
- **Clock Distribution**
- **Power Sequence**
- **Problem Debug**
  - Can't power on
  - Power auto shutdown
  - All dots, zero, and no display
  - Power part

# CPU Feature introduce

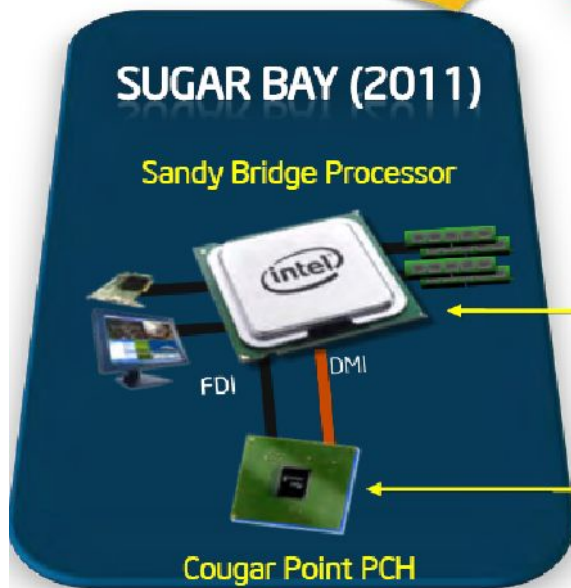
## Platform Overview

*Sugar Bay to Maho Bay Platform Transition*

PCIe Architecture	Raw Bit Rate	Max Total Bandwidth for x16 Link
PCIe 2.0	5.0 GT/s	16 GB/s
PCIe 3.0	8.0 GT/s	32 GB/s

**2X Faster**

**Key Platform Differences:**



**22nm Processor Si Tech**

**USB 3.0**

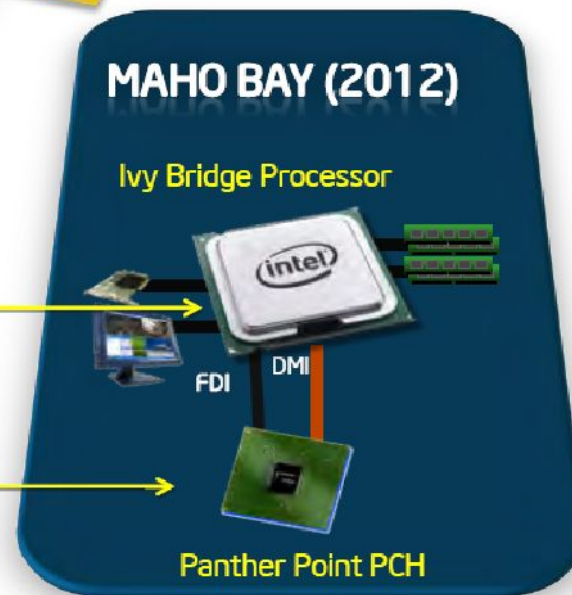
**PCIe\* Gen 3**

**DX11**

**3 Display Support**

**LGA 1155 Socket compatible with Sandy Bridge**

**Pin compatible with Cougar Point**

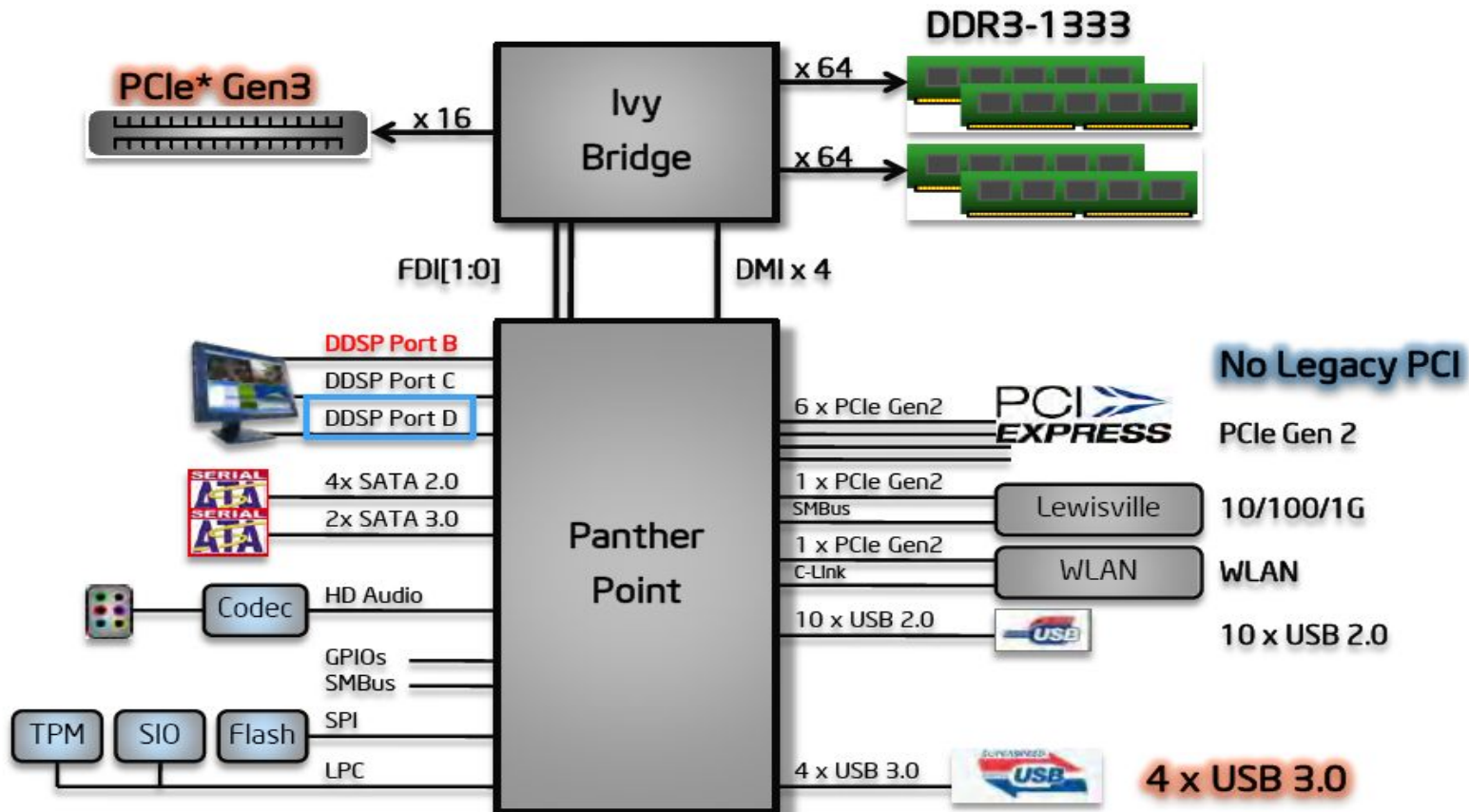


**Easy Migration to Next Generation Performance and Features**

# Intel 7 Series Chipset Architecture

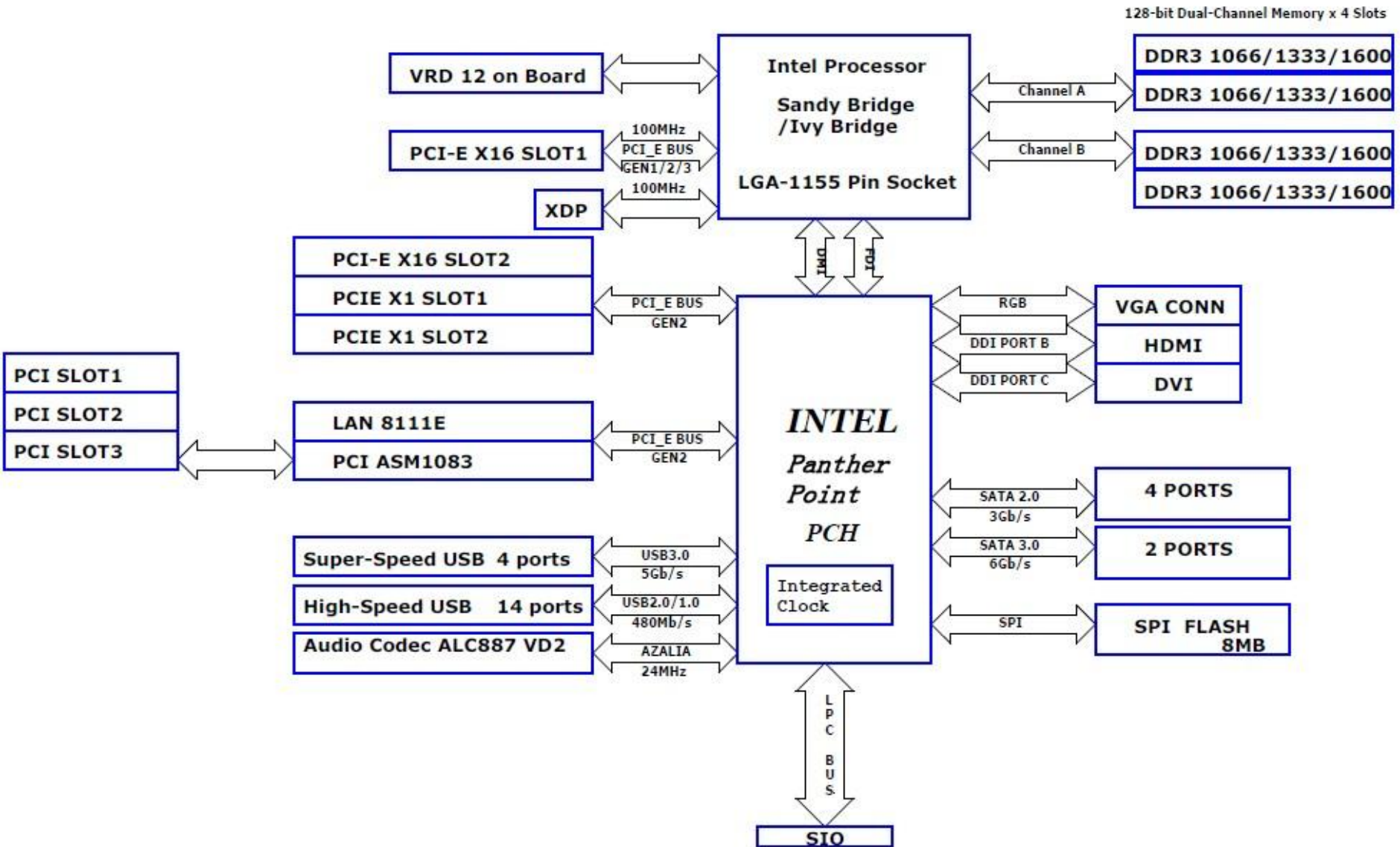
## Platform Enabling Overview Maho Bay Block Diagram

CDI/IBP1

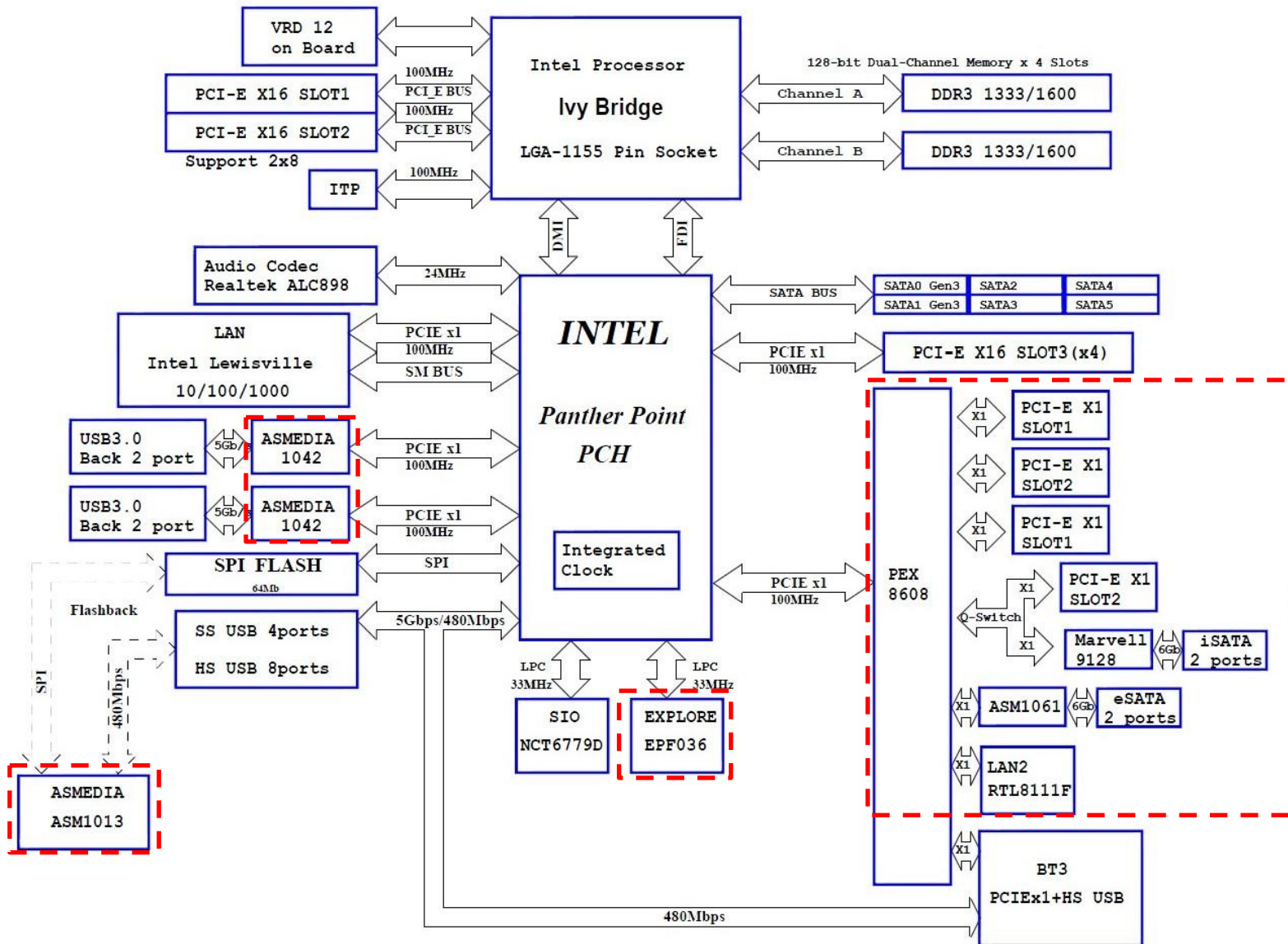


**Leadership with Feature and Technology Rich Platforms**

# P8Z77-V LX Architecture



# P8Z77-V DELUXE Architecture



# PCH Feature introduce

**Table 1-2. Desktop Panther Point Chipset SKUs**

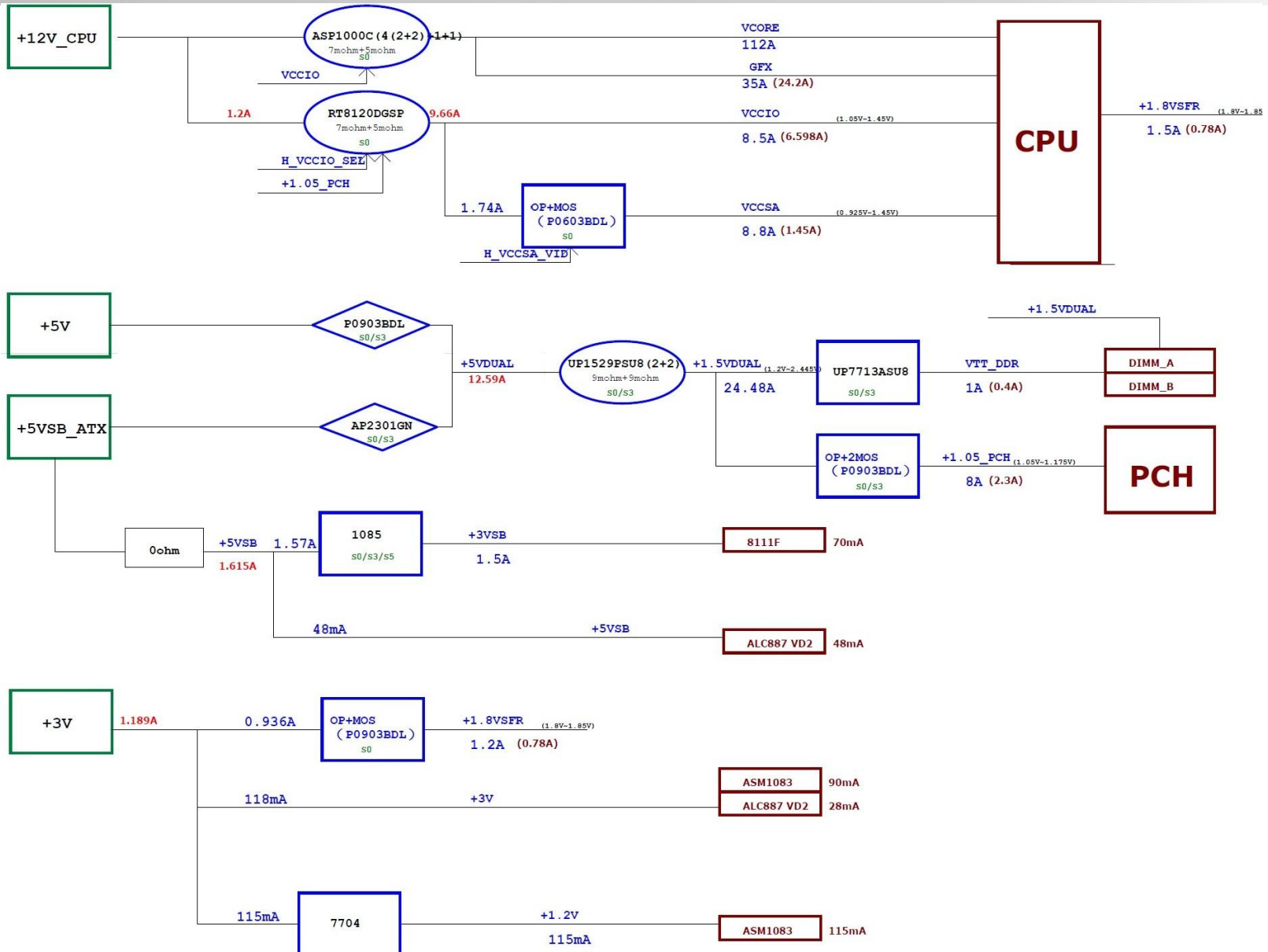
Feature Set		SKU Name					
		Q77	Q75	B75	Z77	Z75	H77
PCI Express* 2.0 Ports		8	8	8	8	8	8
PCI Interface		Yes	Yes	Yes	No <sup>3</sup>	No <sup>3</sup>	No <sup>3</sup>
Total number of USB ports		14	14	12 <sup>4</sup>	14	14	14
<ul style="list-style-type: none"> <li>• USB 3.0 Capable Ports (SuperSpeed and all USB 2.0 speeds)</li> <li>• USB 2.0 Only Ports</li> </ul>		4	4	4	4	4	4
<ul style="list-style-type: none"> <li>• USB 2.0 Only Ports</li> </ul>		10	10	8	10	10	10
Total number of SATA ports		6	6	6	6	6	6
<ul style="list-style-type: none"> <li>• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)</li> <li>• SATA Ports (3 Gb/s and 1.5 Gb/s only)</li> </ul>		2 <sup>5</sup>	1 <sup>6</sup>	1 <sup>6</sup>	2 <sup>5</sup>	2 <sup>5</sup>	2 <sup>5</sup>
<ul style="list-style-type: none"> <li>• SATA Ports (3 Gb/s and 1.5 Gb/s only)</li> </ul>		4	5	5	4	4	4
HDMI/DVI/VGA/DisplayPort*/eDP*		Yes	Yes	Yes	Yes	Yes	Yes
Integrated Graphics Support		Yes	Yes	Yes	Yes	Yes	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes	Yes
	RAID 0/1/5/10 Support	Yes	Yes <sup>7</sup>	No	Yes	Yes	Yes
	Intel® Smart Response Technology	Yes	No	No	Yes	No	Yes
Intel® Anti-Theft Technology		Yes	Yes	Yes	Yes	Yes	Yes
Intel® Active Management Technology 8.0		Yes	No	No	No	No	No
Intel Fast Flash Standby <sup>8</sup>		Yes	No	No	No	No	No

# Ivy 7 Series – Agenda

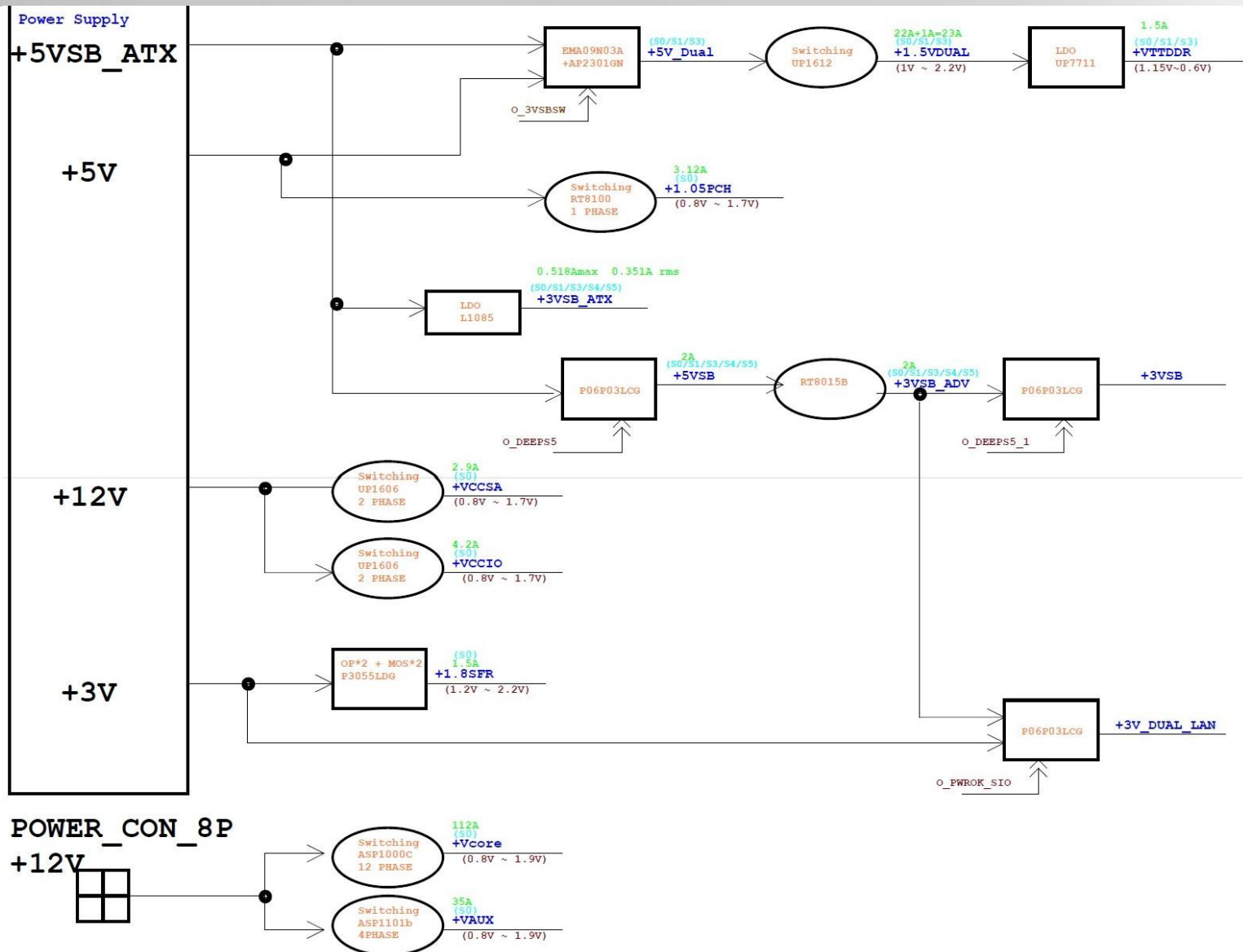
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# P8Z77-V LX Power Flow



# P8Z77-V DELUXE Power Flow



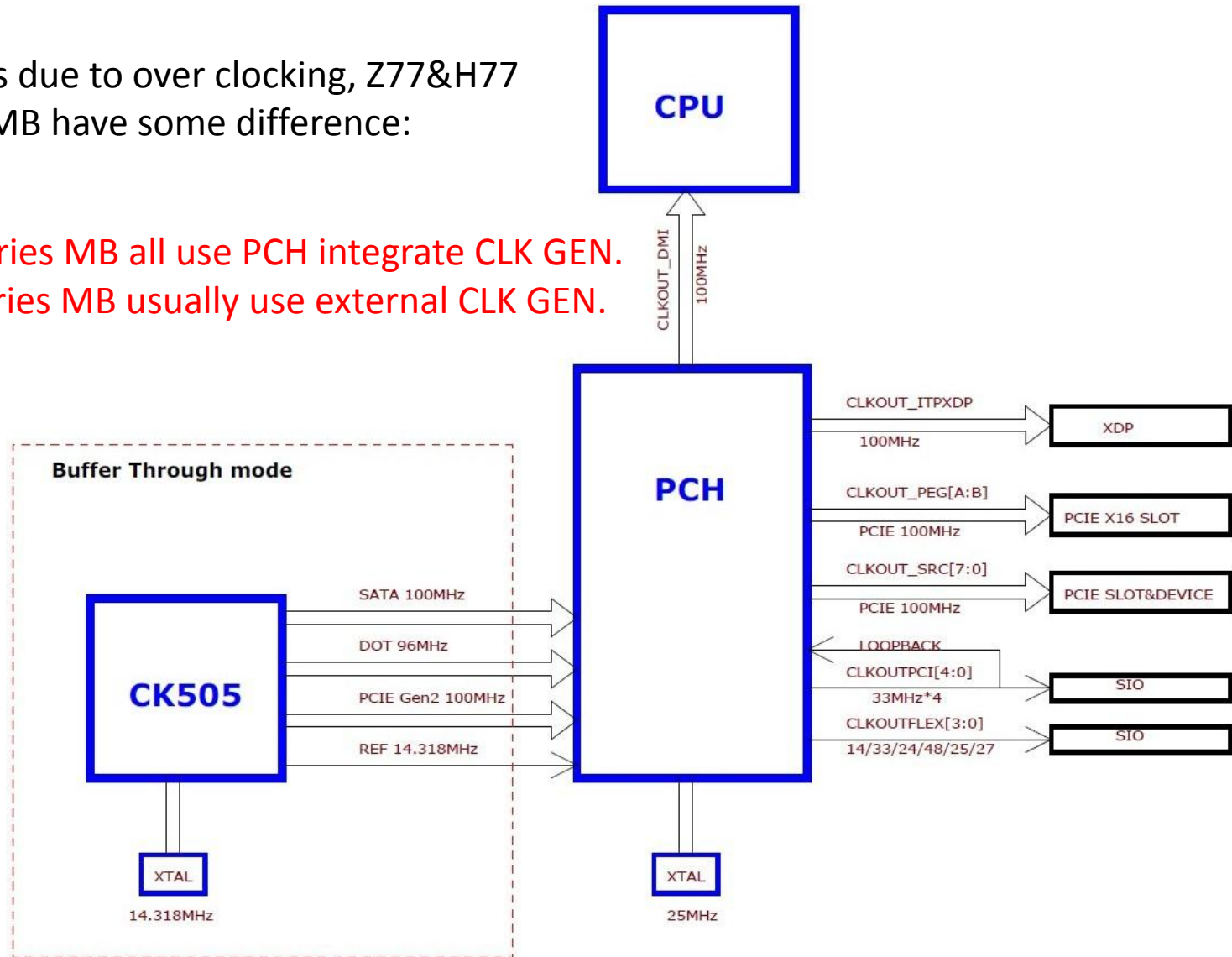
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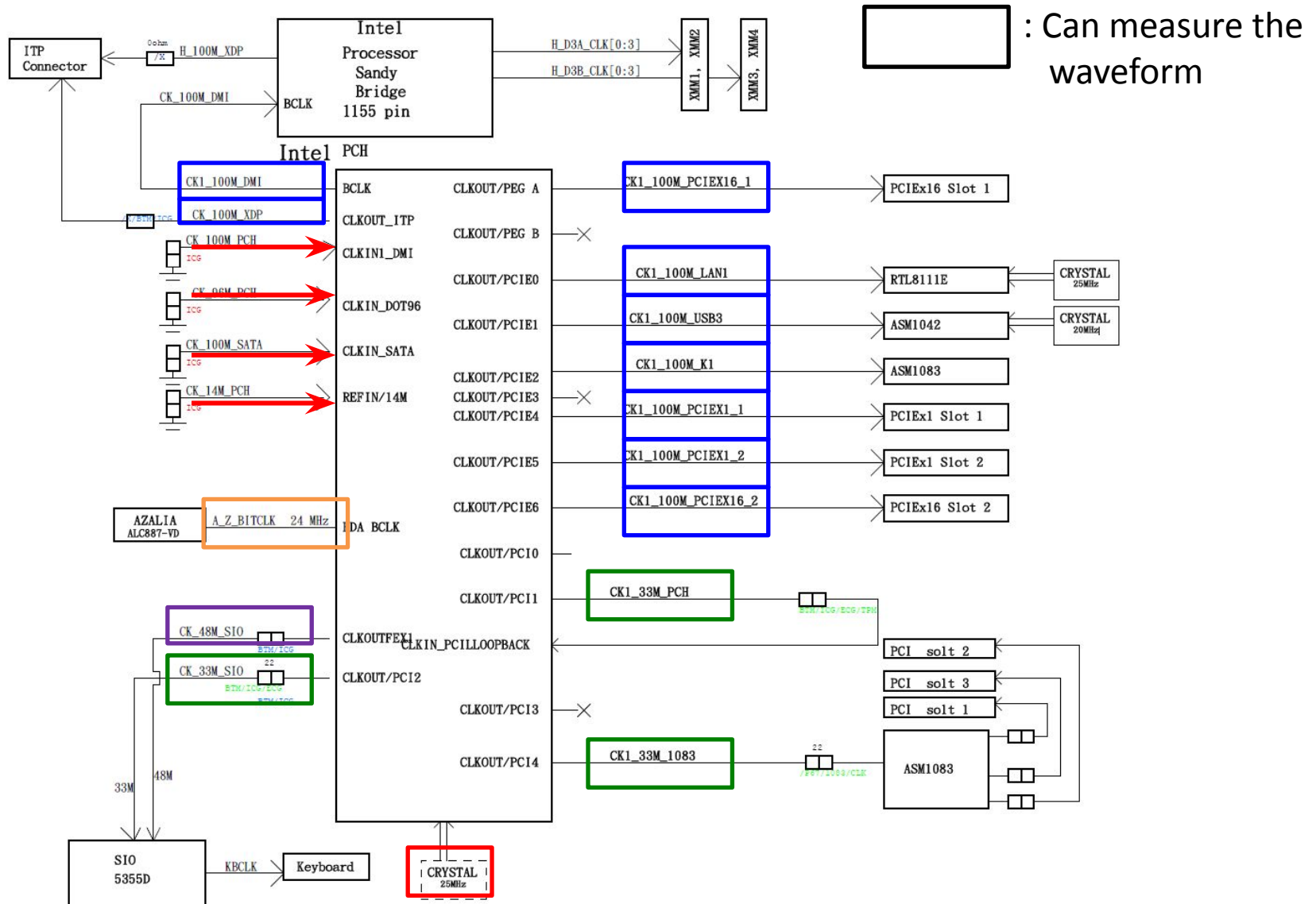
# 7 Series Clock Distribution

7 Series due to over clocking, Z77&H77 series MB have some difference:

Z77 series MB all use PCH integrate CLK GEN.  
H77 series MB usually use external CLK GEN.

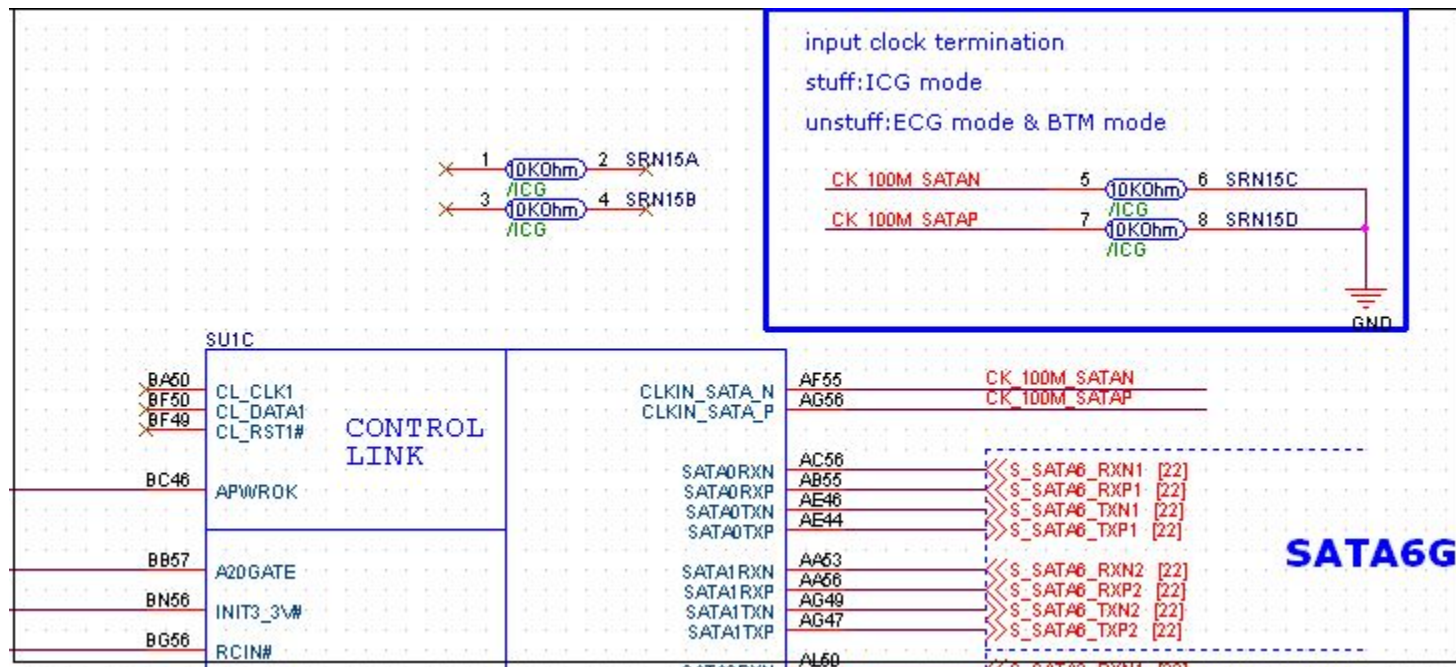


# P8Z77-V LE Clock Distribution



# SATA clock

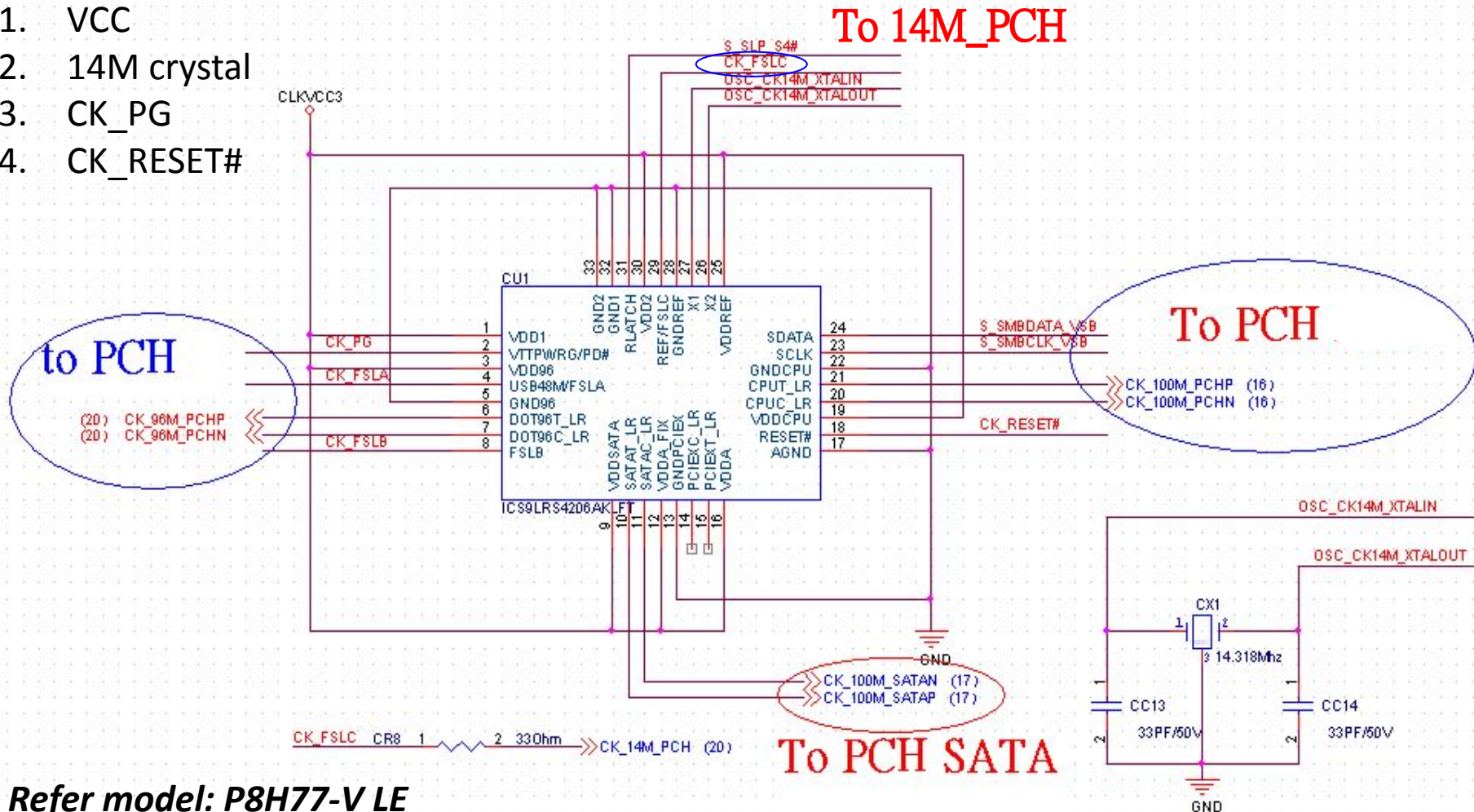
1. If PCH internal provide CLK, it will use two 10K ohm resistors to connect to ground.
2. If not, external CLK generator will provide 100M Hz frequency for PCH



# External CLK GEN (ICS9LRS4206)

Check point:

1. VCC
2. 14M crystal
3. CK\_PG
4. CK\_RESET#



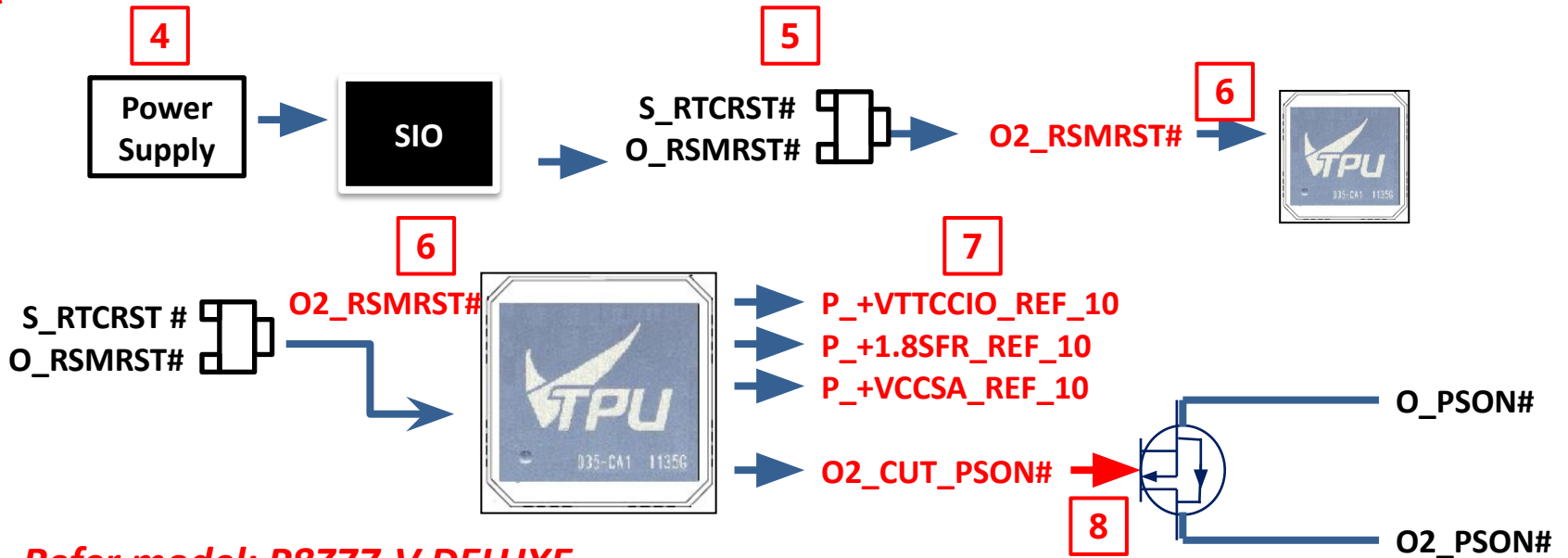
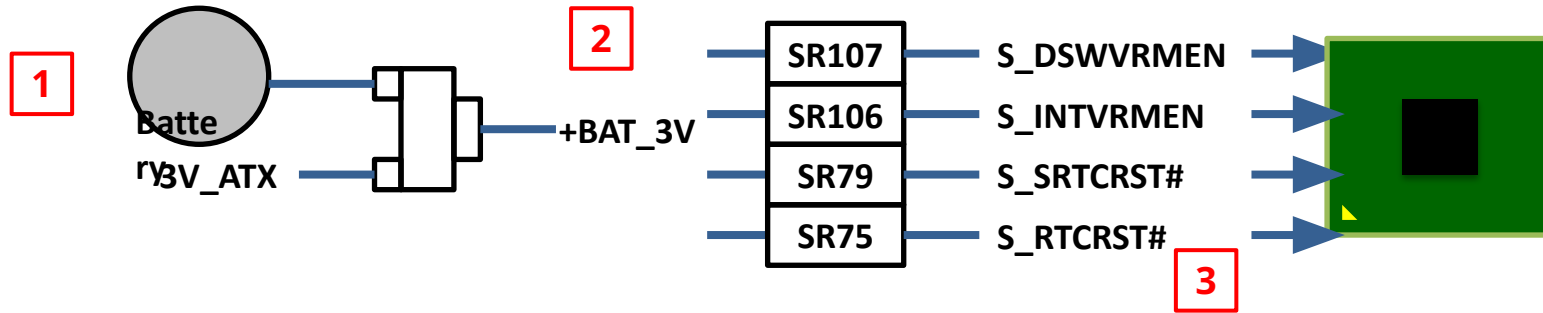
**Refer model: P8H77-V LE**

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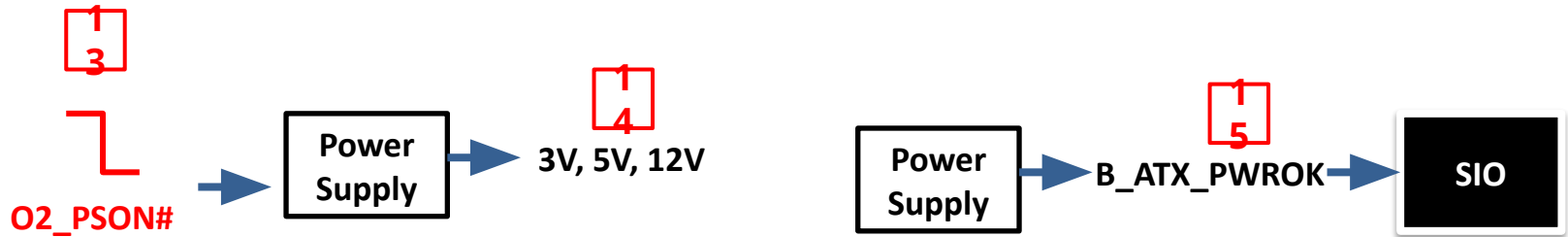
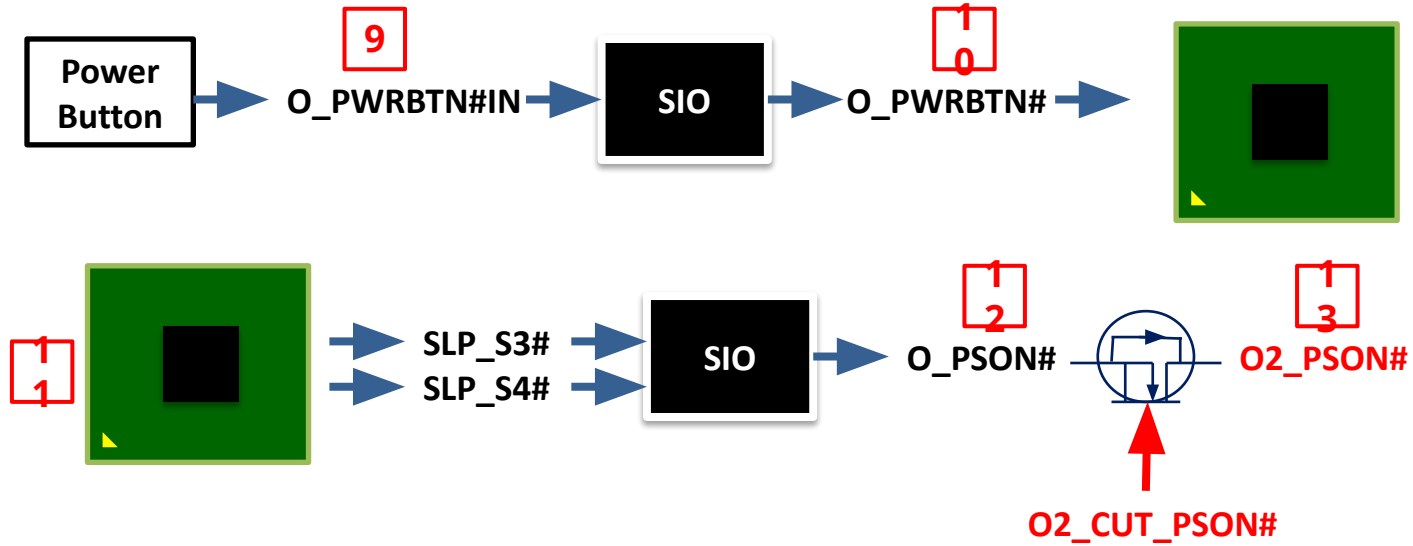


# Power on sequence

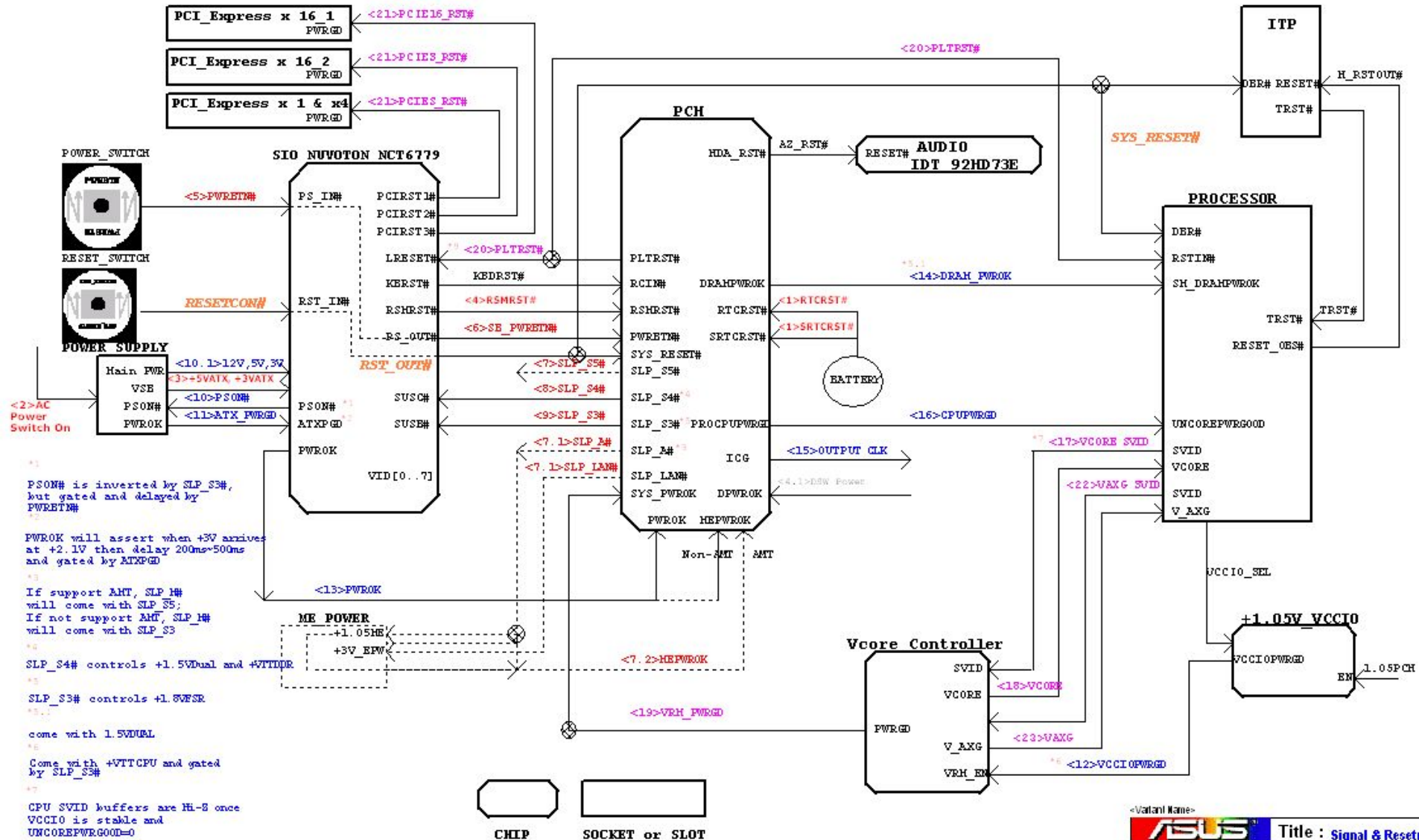


**Refer model: P8Z77-V DELUXE**

# Power on sequence



# Power on sequence

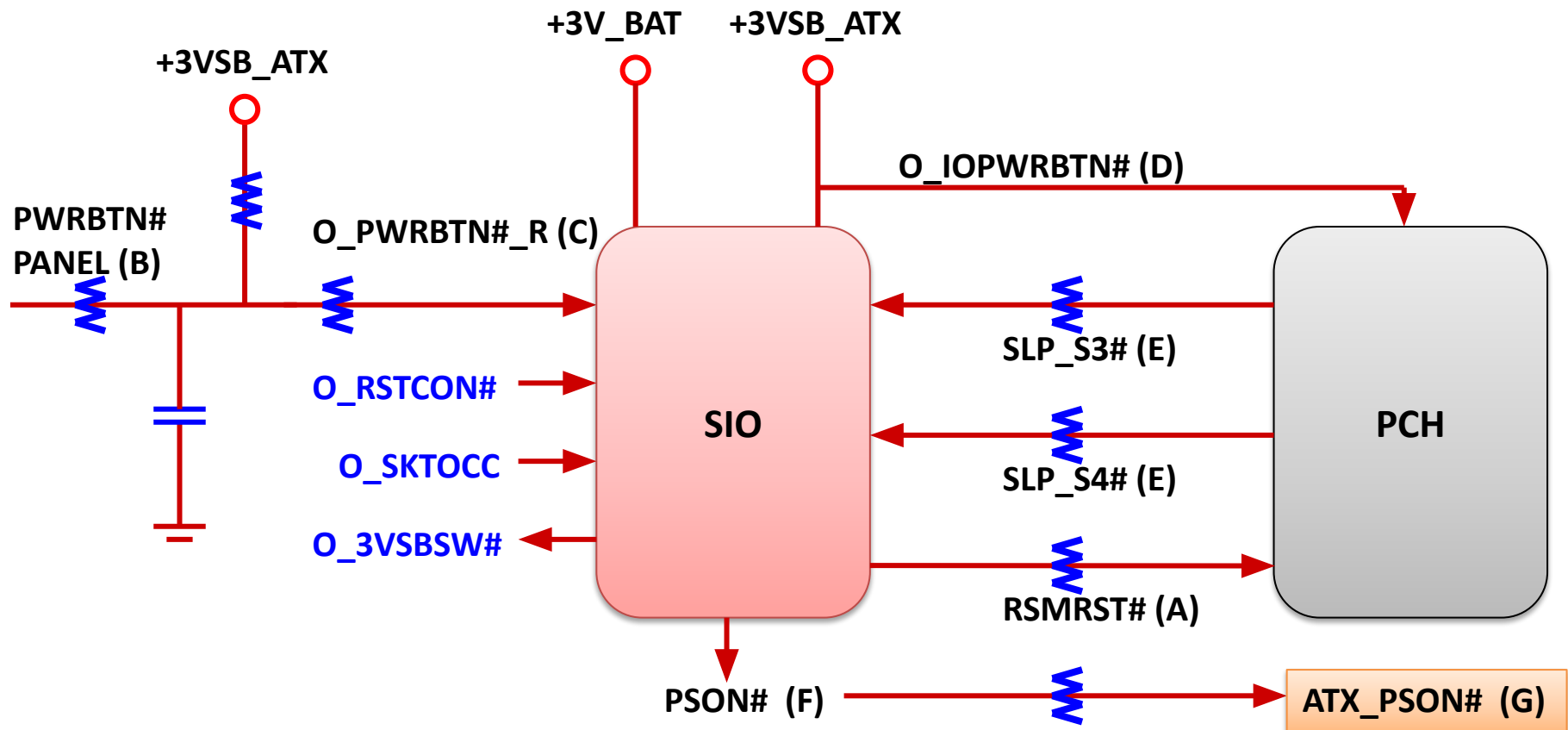


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# Debug - Can't power on (1)

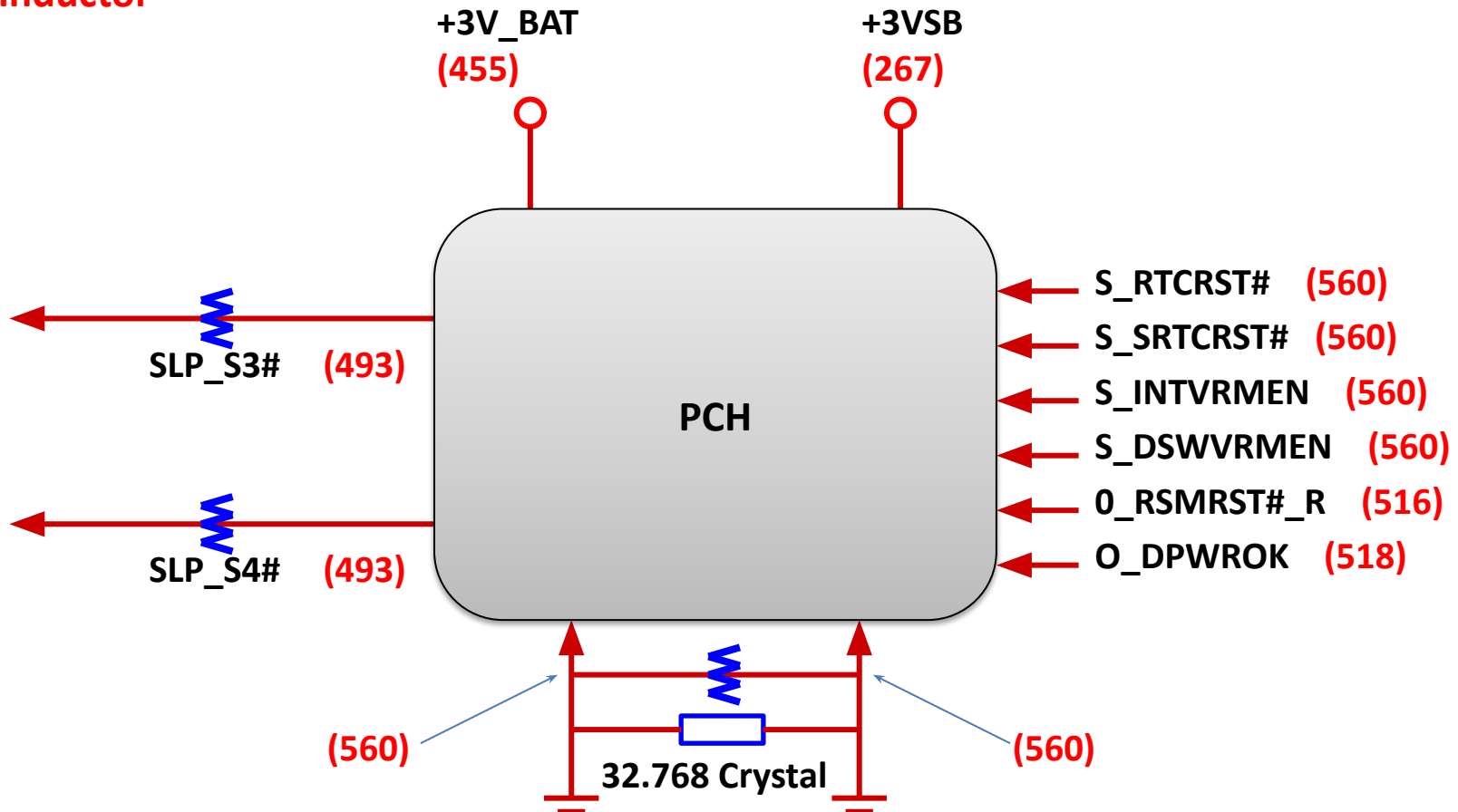
## 1. Check SIO power sequence and working condition:



# Debug - Can't power on (2)

2. Check PCH power sequence and working condition

3. Other condition: make sure 5V\_DUAL & 1.5VDUAL is low; 1.5V\_DUAL phase inductor

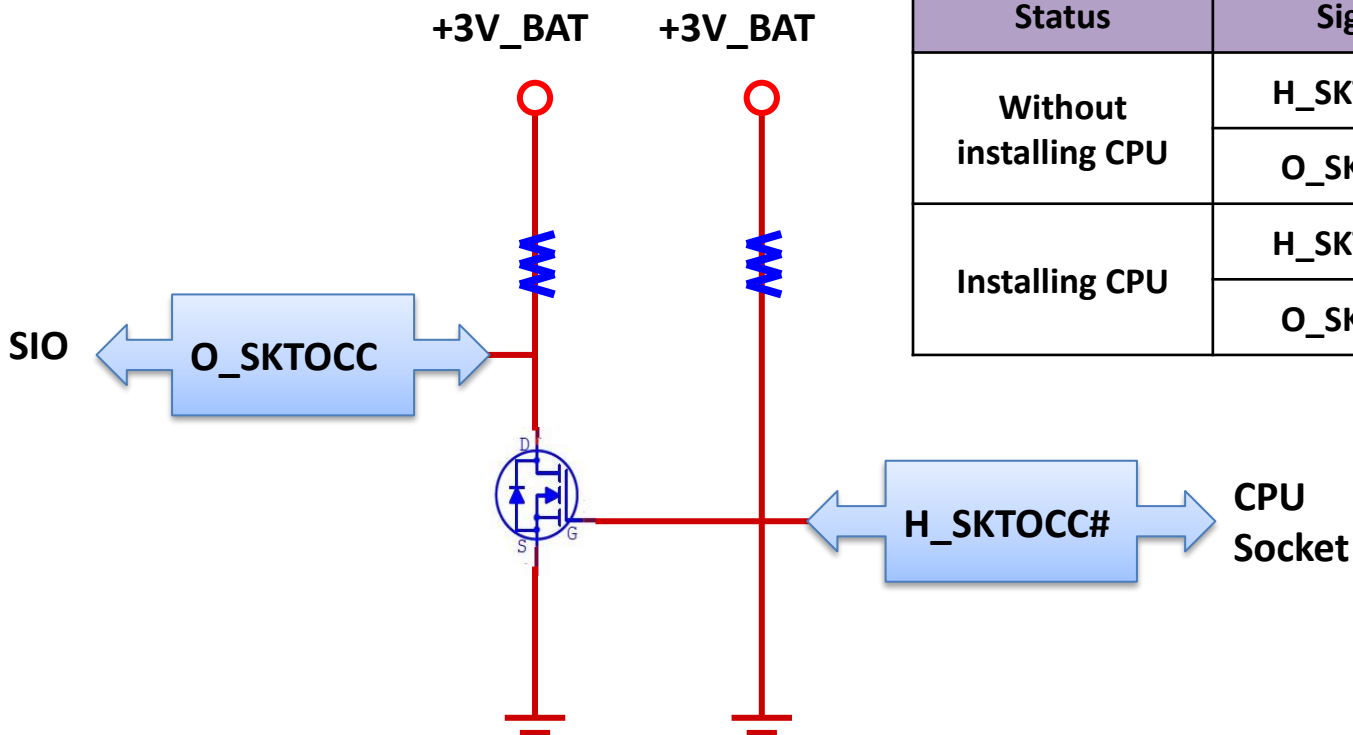


\*(red part): using multi meter with diode status, red(VΩmA ) to ground & black to test via

# Debug - Can't power on (3)

## 4. O\_SKTOCC: SIO uses this pin to detect MB with CPU or not.

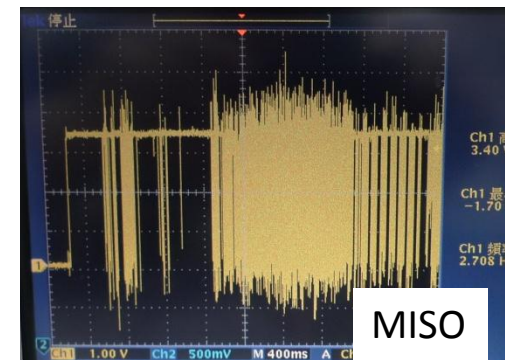
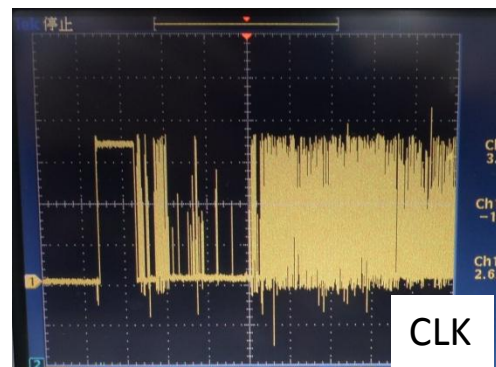
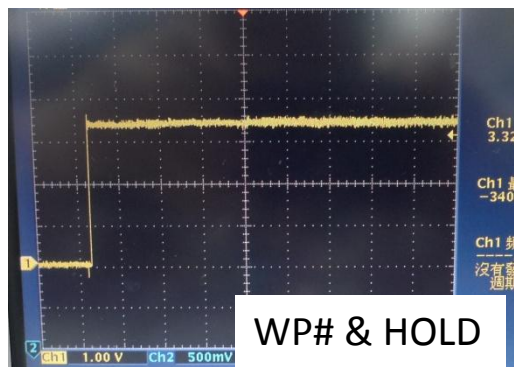
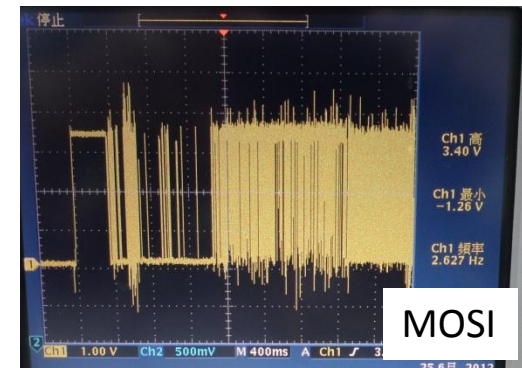
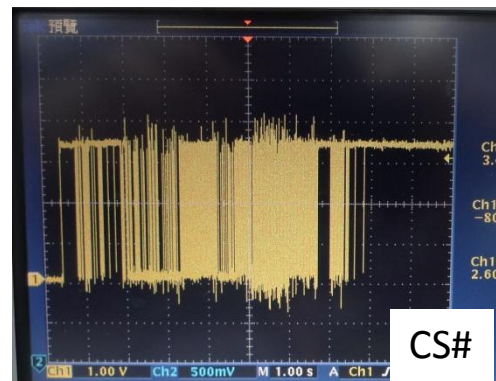
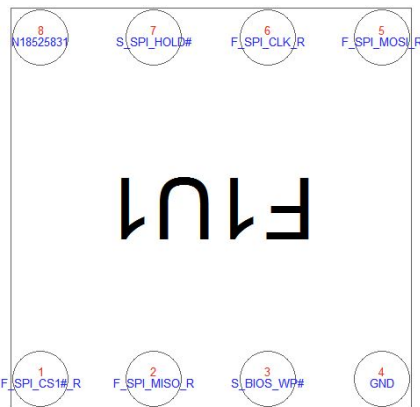
At G3, before installing CPU, H\_SKTOCC# voltage level is high; after installing CPU, H\_SKTOCC# signal will get low.



Status	Signal	Power level
Without installing CPU	H_SKTOCC#	High
	O_SKTOCC	Low
Installing CPU	H_SKTOCC#	Low
	O_SKTOCC	High

# Debug – Power auto shutdown (1)

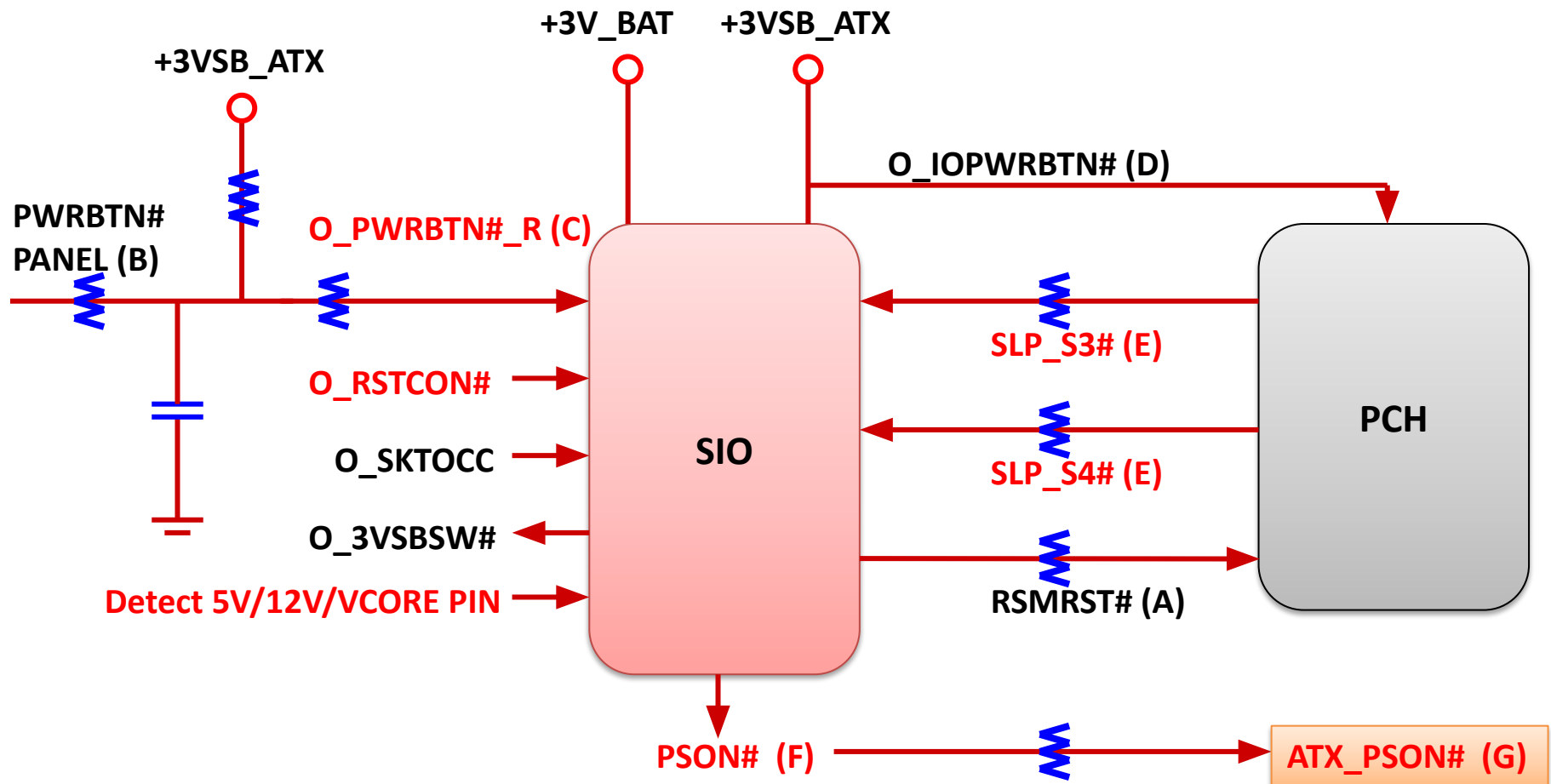
1. Update BIOS or exchange another BIOS chipset
2. Make sure that MB has no crack, trace open and components missing or damage
3. Check DMI (or FDI) LED bus signals are ok.
4. Check main voltage impedance. If ok, short with PSON to check main voltage.
5. 12V/5V/3V/5VDUAL/1.5VDUAL/ VTTDDR/1.05PCH/1.8SFR/VCCSA/ VCCIO/VCORE
6. When power on, BIOS signals will start to receive command & send data.





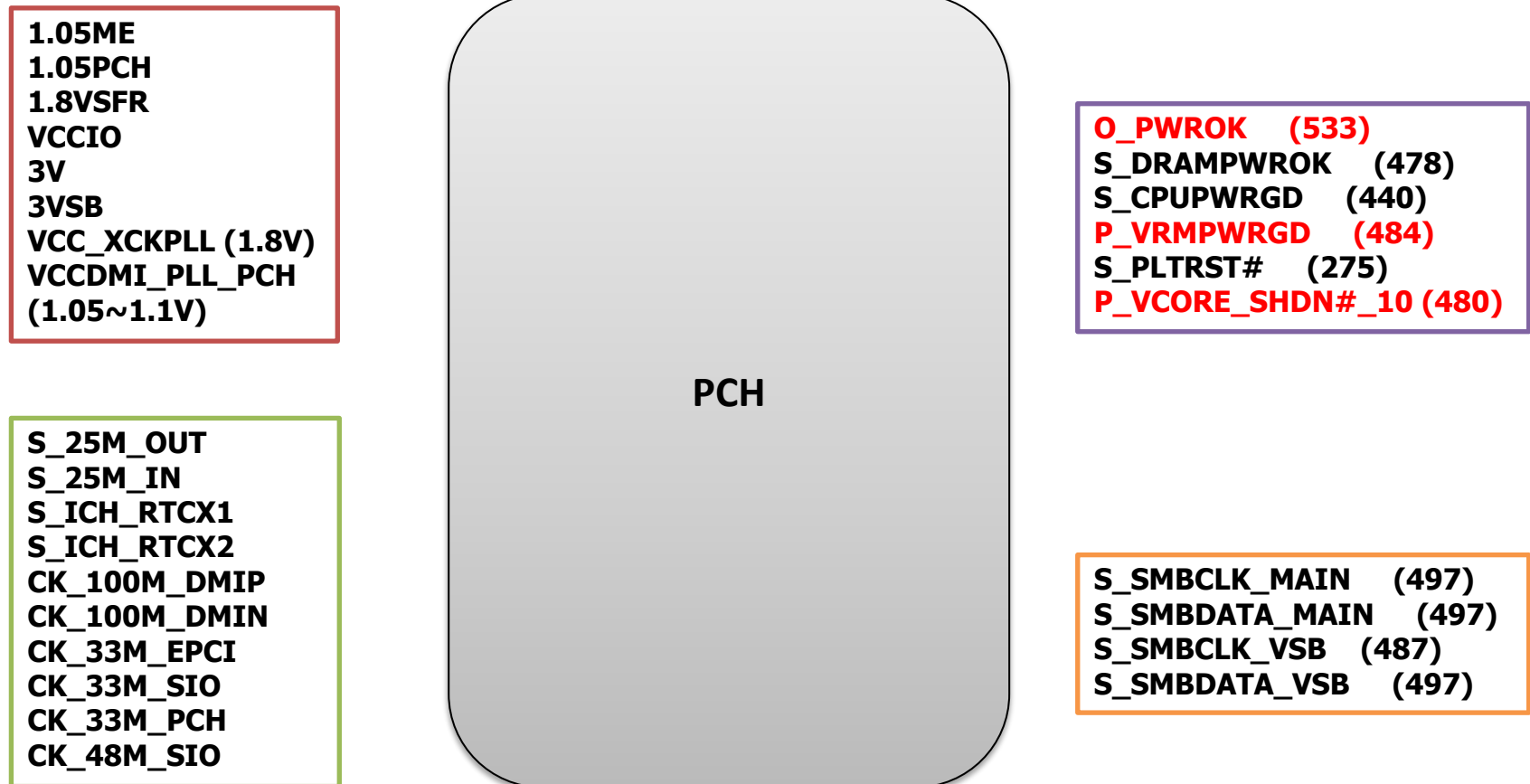
# Debug – Power auto shutdown (2)

7. Follow the sequence, measure that PSON#, SLP\_S3, SLP\_S4, PWRBTN# and RSTCON# are normal or not.



# Debug – Power auto shutdown (2)

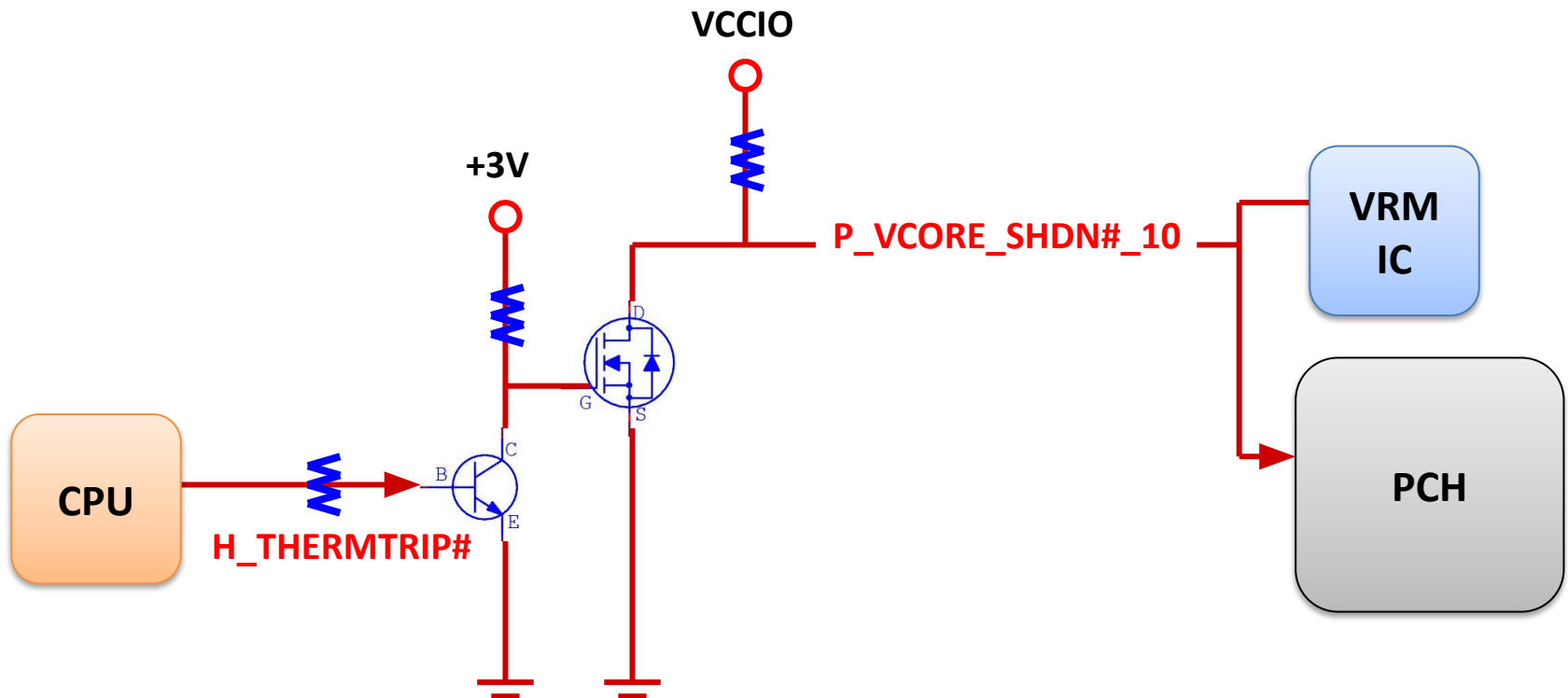
10. If PCH working condition is abnormal, MB also will shutdown.



# Debug – Power auto shutdown (3)

Problem with power shutdown: THERMAL signals, voltage, PCH working condition and the power sequence (power ok signals)

8. If H\_THERMTRIP# is low, P\_VCORE\_SHDN#\_10 will pull low to PCH.
9. If VCORE is abnormal, VRM IC will also use P\_VCORE\_SHDN#\_10 to pull low.



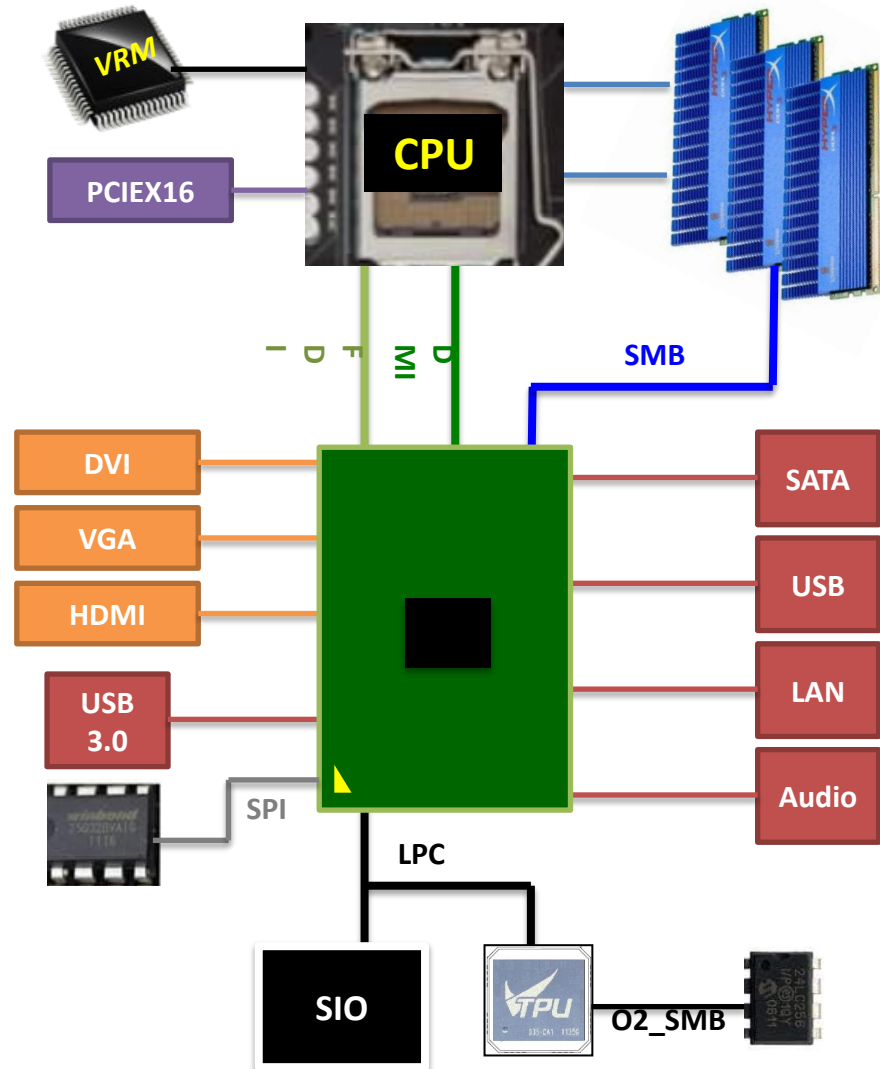
# Debug – All dots, zero, and no display

## Before 00:

1. Power on
2. Power/CLK/RST
3. CPURST#

## After 00 and CPURST#:

1. CPU to PCH (DMI)
2. PCH to BIOS (SPI)
3. SPI to PCH (SPI)
4. PCH to CPU (DMI)  
PCH to MEMORY (SMB)
5. CPU to MEMORY
6. PCH to SIO (LPC)  
PCH to EC
7. PCH to DEVICE
8. CPU to PCH (FDI)
9. PCH to DVI/VGA/HDMI  
CPU to PCIEX16



# Debug – All dots, zero, and no display

## Measure BUS:

### 1. DMI:

H\_DMI\_RXN/P[0:3]  
H\_DMI\_TXN/P[0:3]  
S\_DMICOMP  
S\_DMIRBIAS  
VCCDMI\_PLL\_PCH

### 2. FDI:

H\_FDI\_INT  
H\_FDI\_COMP  
H\_FDI\_FSYNC[0:1]  
H\_FDI\_LSYNC[0:1]  
H\_FDI\_TXN/P[0:7]

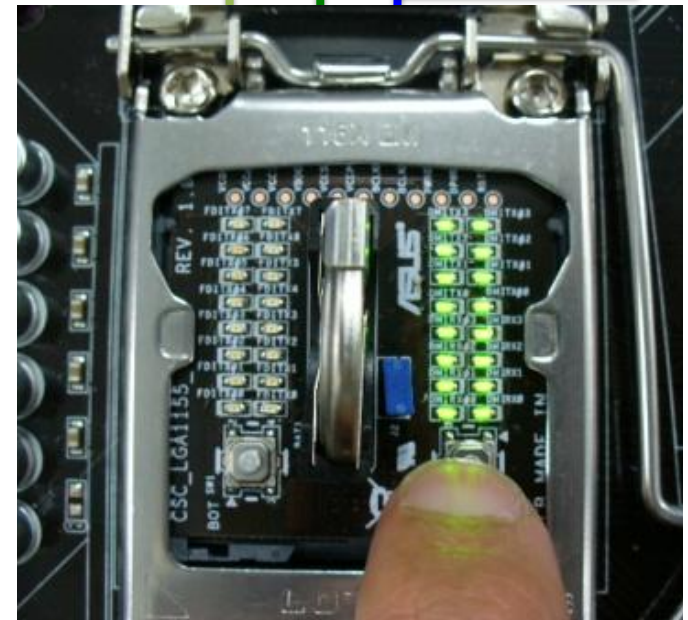
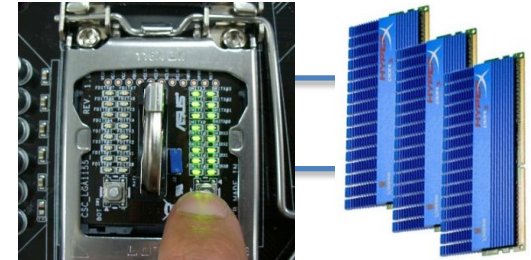
### 3. SMB:

S\_SMBCLK\_MAIN  
S\_SMBDATA\_MAIN  
S\_SMBCLK\_PCI  
S\_SMBDATA\_PCI

### 4. Memory to CPU

D3A\_DQ[0:63]  
D3A\_MA[0:15]  
D3A\_DQSN/P[0:7]  
D3A\_BA[0:2]  
D3A\_RESET#

D3A\_CLKP/N[0:1]  
D3A\_CS#[0:1]  
D3A\_ODT[0:1]  
D3A\_CKE[0:1]  
D3A\_WE#  
D3A\_RAS#  
D3A\_CAS#



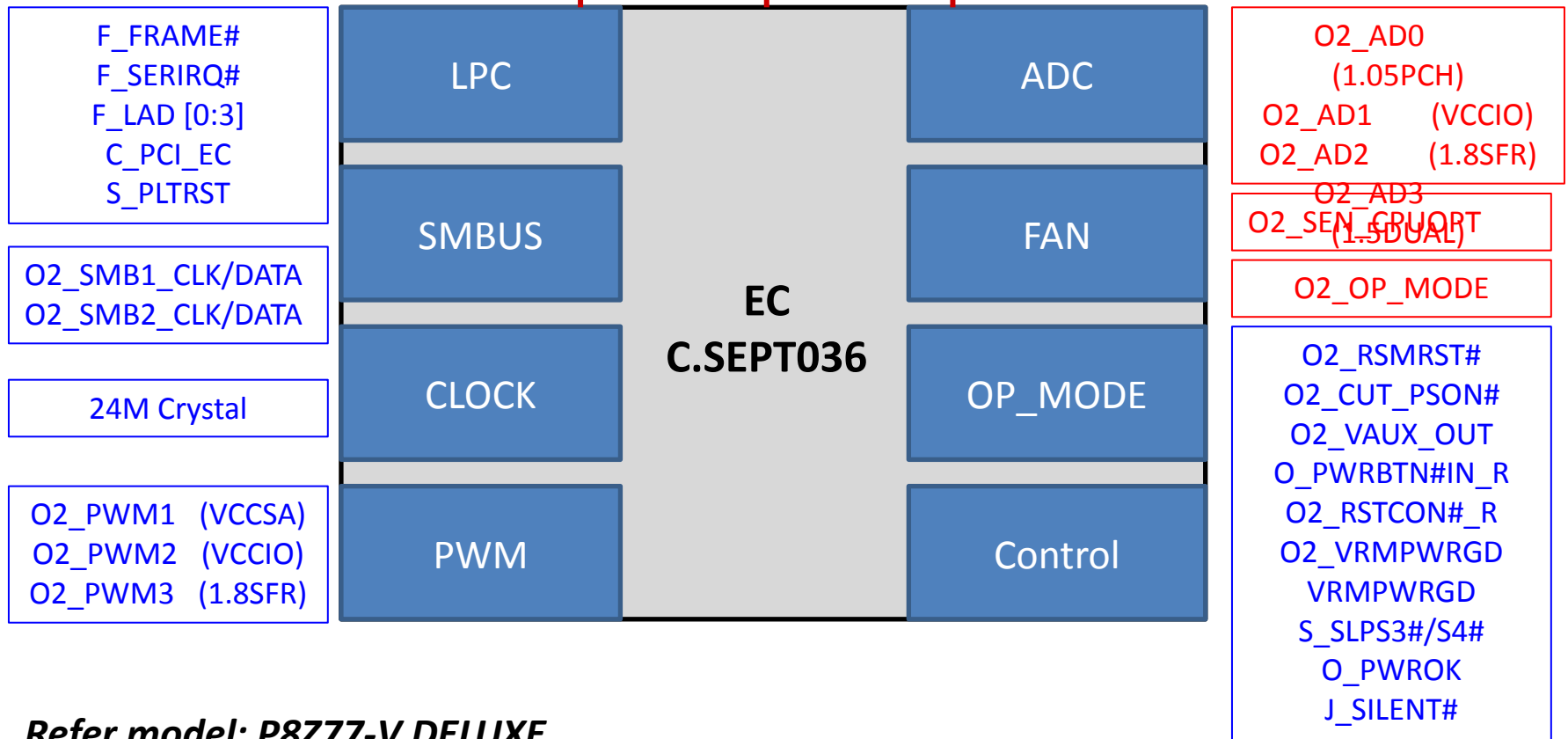
# Debug – All dots, zero, and no display

Chipset (EC C.SEPT036)

O2\_VREF

3VSB

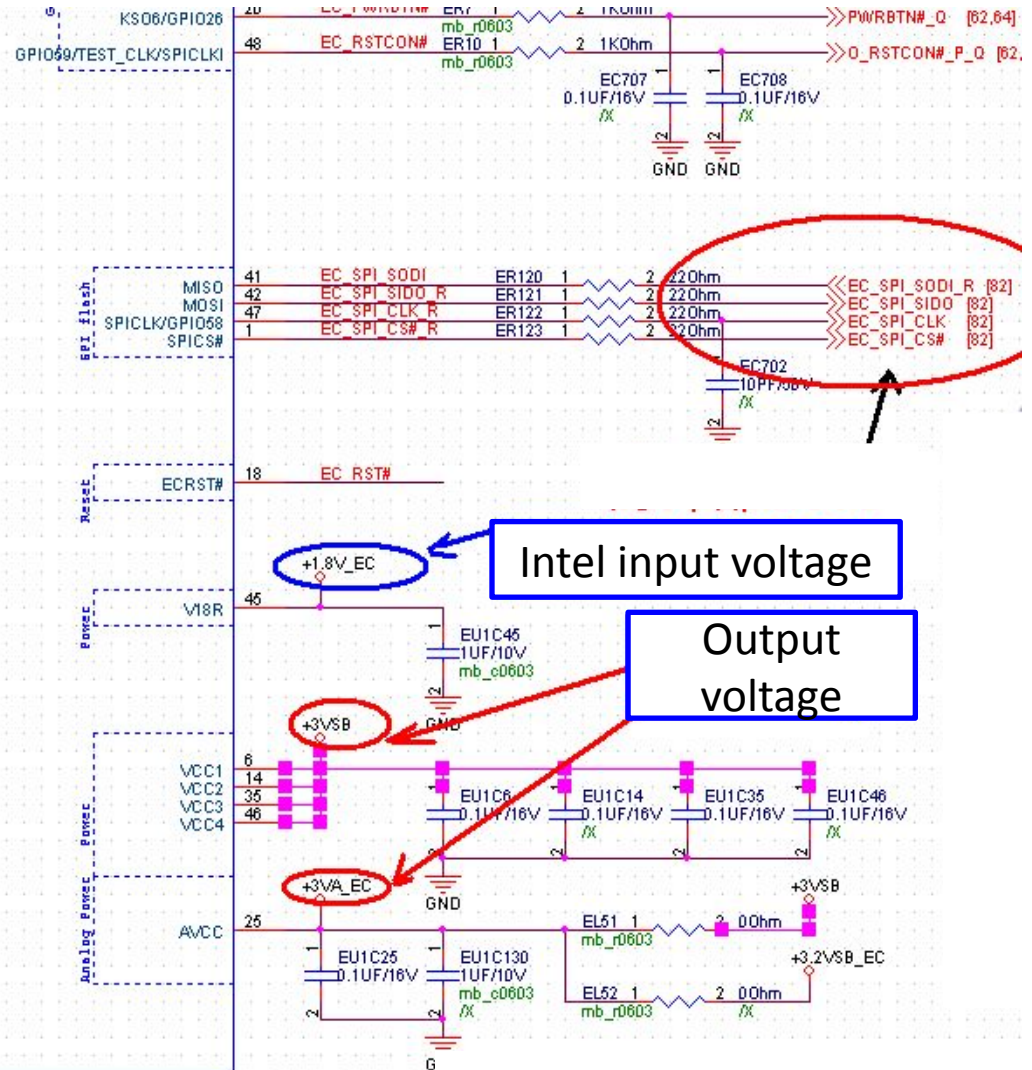
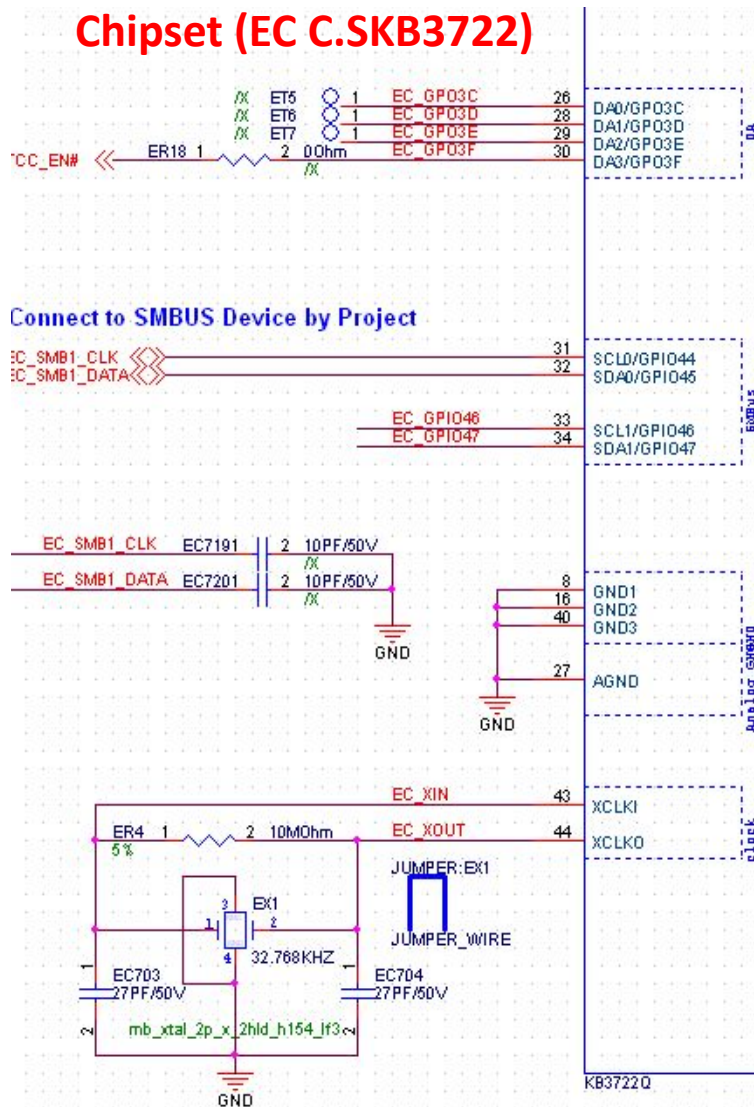
O2\_VDDA (O2\_3.2V)



**Refer model: P8Z77-V DELUXE**

# Debug – All dots, zero, and no display

## Chipset (EC C.SK3722)

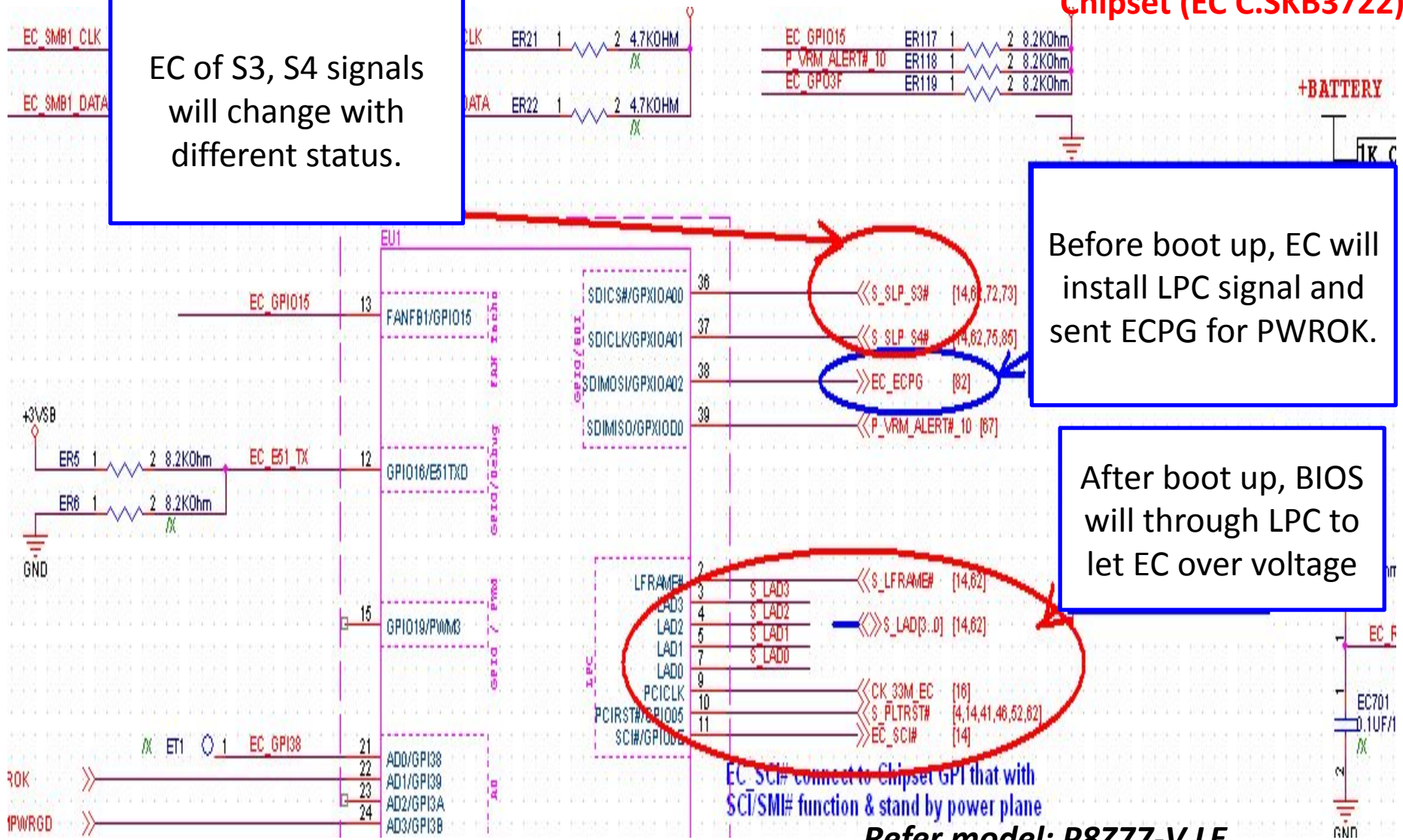


**Refer model: P8Z77-V LE**

# Debug – All dots, zero, and no display

EC of S3, S4 signals will change with different status.

Chipset (EC C.SK3722)



Before boot up, EC will install LPC signal and sent ECPG for PWROK.

After boot up, BIOS will through LPC to let EC over voltage

EC SCI# connect to Chipset GPI that with SCI/SMI# function & stand by power plane

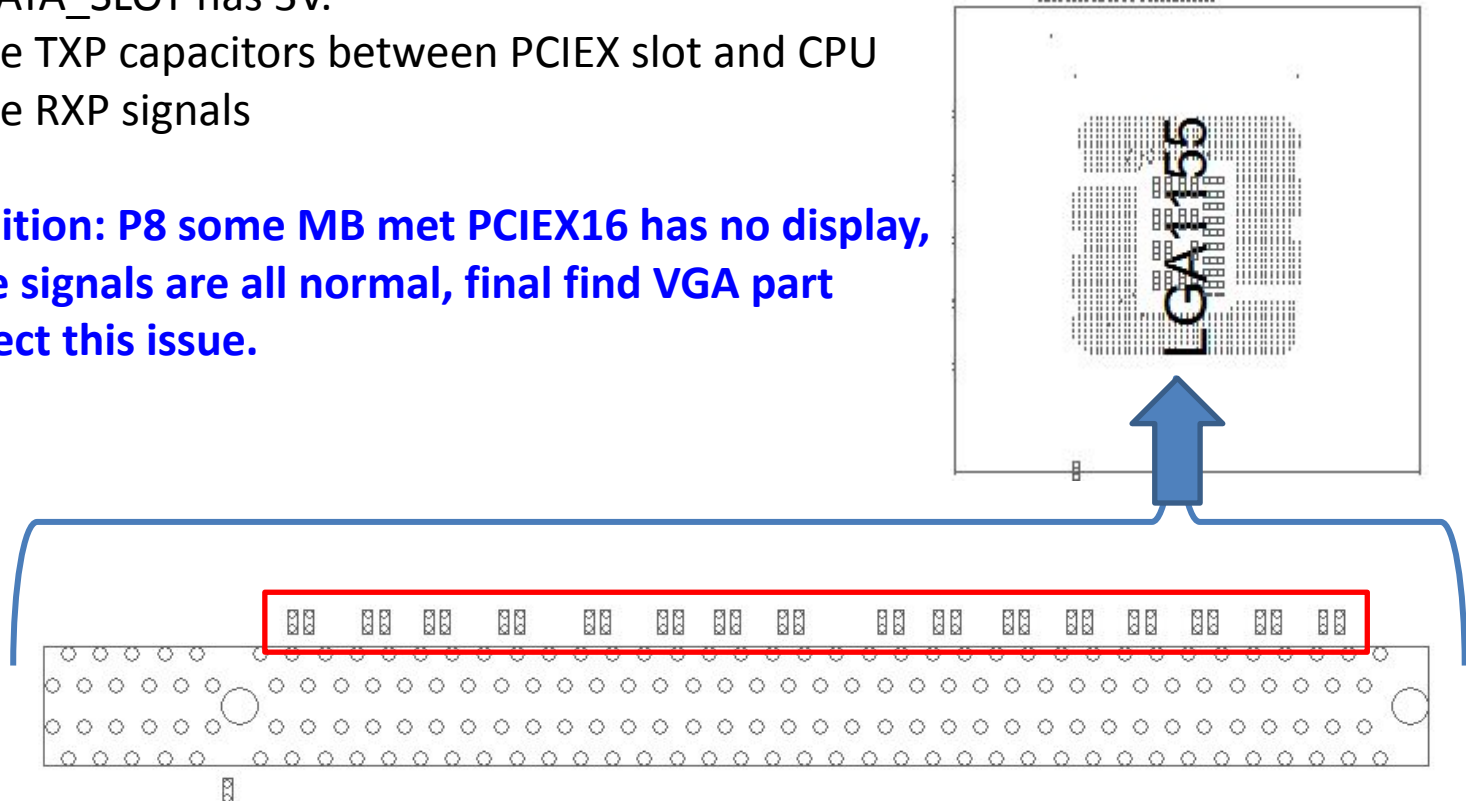
Refer model: P8Z77-V LE



# Debug – No display (PCIEX16)

1. Measure CPU voltage: V<sub>CORE</sub>, G<sub>FX</sub>, V<sub>CCIO</sub>, V<sub>CCSA</sub>, 1.8S<sub>FR</sub>, 1.5V<sub>DUAL</sub>
2. Check 12V, 3V, 3V<sub>SB</sub> on PCIEX slot.
3. CK\_100M\_X16SL1N/P, 100M Hz frequency from SB.
4. O\_X16\_RST#, reset signal from SIO.
5. S\_SMBCLK\_SLOT has 3V.
6. S\_SMBDATA\_SLOT has 3V.
7. Check the TXP capacitors between PCIEX slot and CPU
8. Check the RXP signals

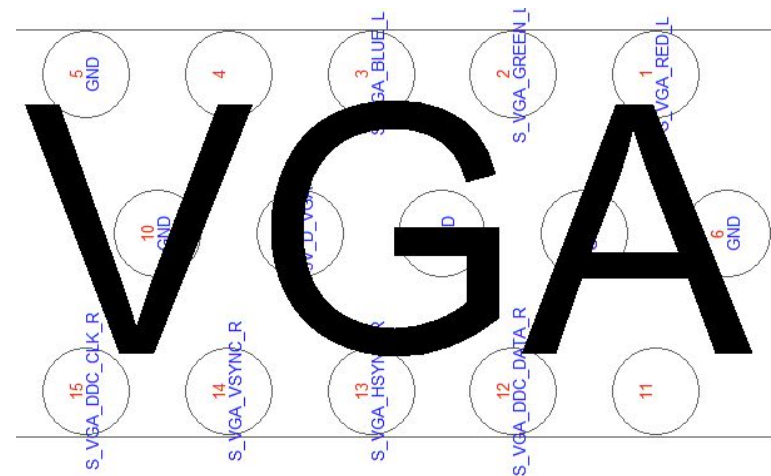
**Others condition: P8 some MB met PCIEX16 has no display, Check above signals are all normal, final find VGA part signal to affect this issue.**



# Debug – No display (VGA)

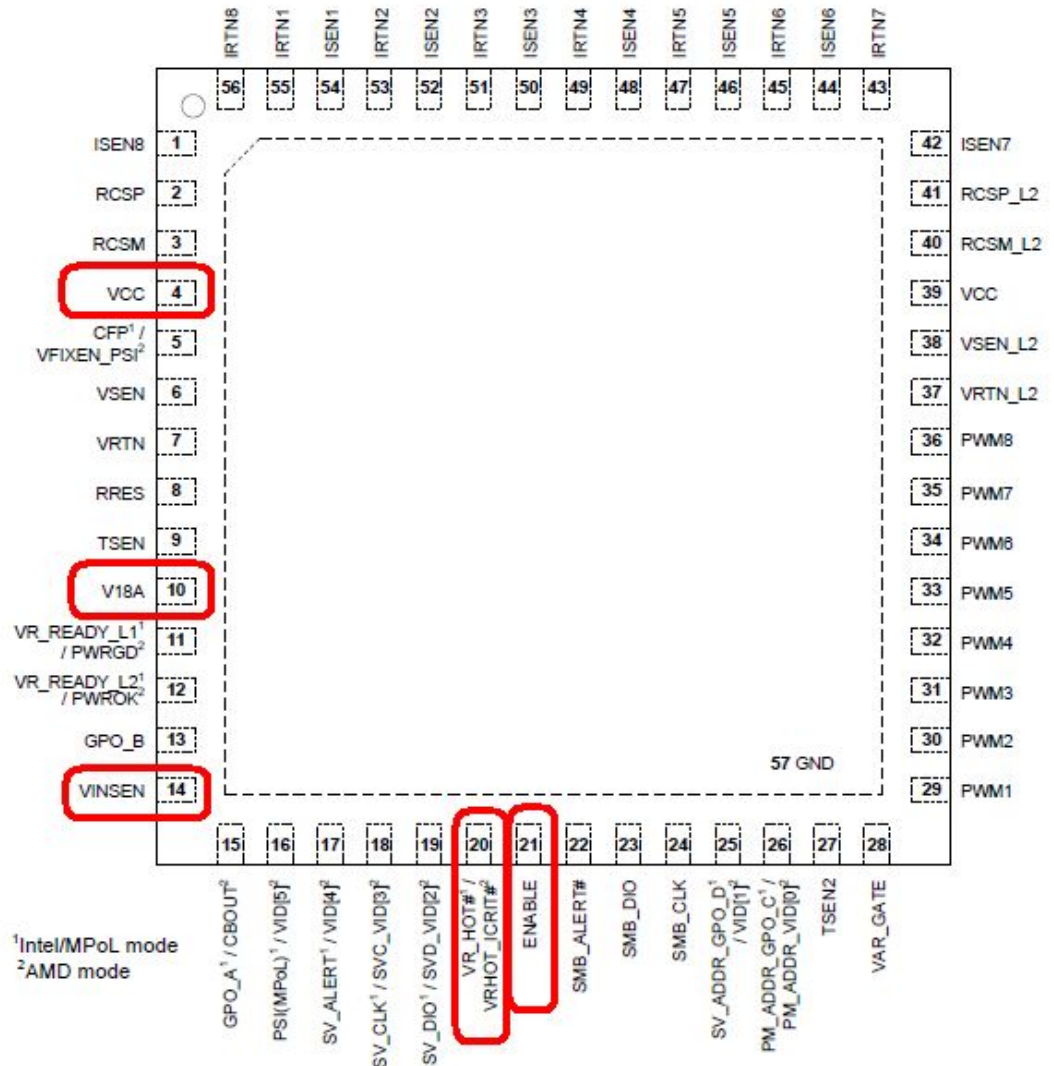
1. FDI and DMI Bus, make sure that all LED lights are normal
2. CPU voltage: VCORE, GFX, VCCIO, VCCSA, 1.8SFR, 1.5VDUAL
3. P\_GFX\_OK\_10, when debug code run to b2, P\_GFX\_OK\_10 will pull high to 3V, at the same time, GFX power will drop from 1V to 0.4~0.5V
4. +5V\_D\_VGA has 5V
5. Check the RGB GND impedance (77 ohm)
6. Check S\_VGA\_VSYNC and S\_VGA\_HYSNC GND impedance (500 ohm)
7. Check VGA\_DDC\_CLK and VGA\_DDC\_DATA impedance (538 ohm)
8. Check PCH V\_3P3\_DAC\_FB (3V)
9. S\_DAC\_IREF(0.6), after b2 code, this signal's power level will raise up
10. 25M Hz crystal
11. Other device also will affect this problem

**EX: P8P67 LE halt at b2**  
**Exchange USB3.0 IC (ASM1042)**  
**To solve this case**



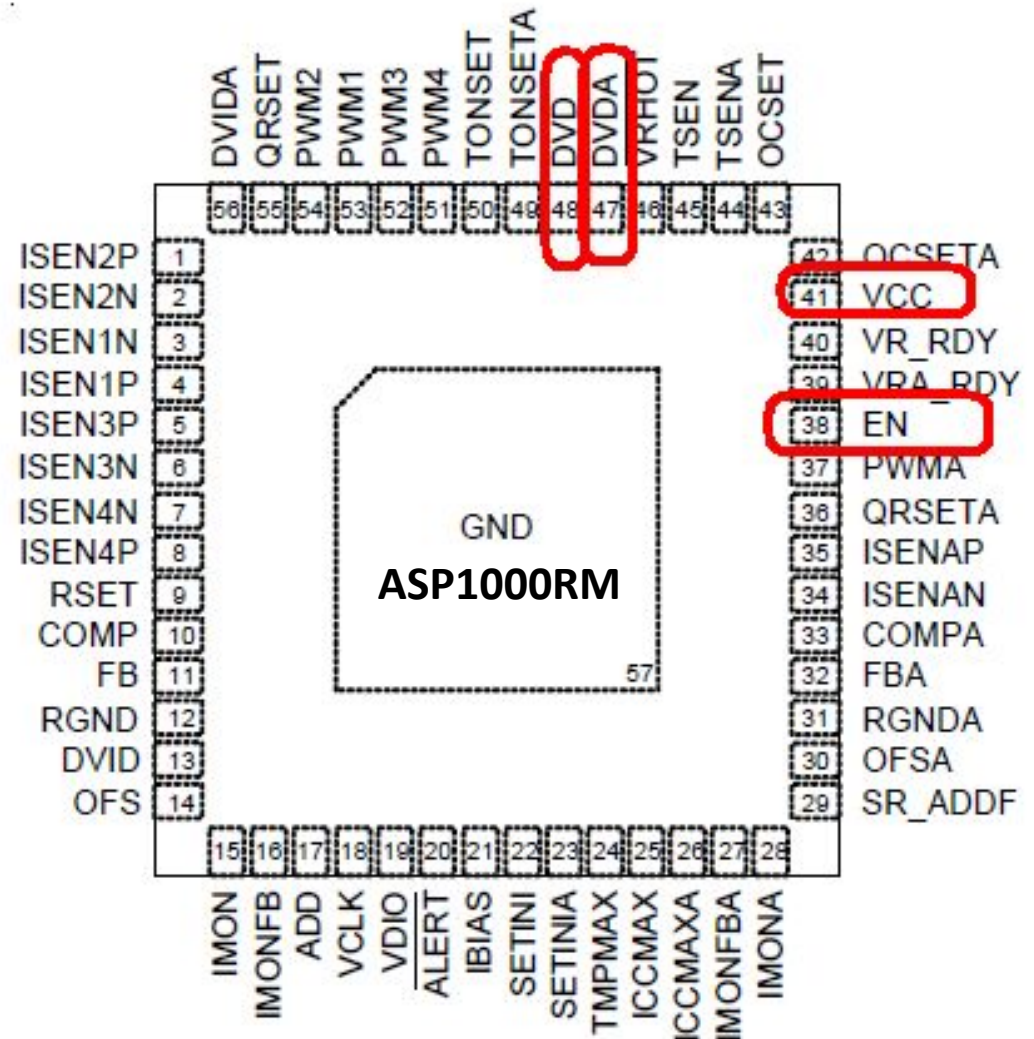
# ASP1000C

- Vcc=3.3V
- Vinsen = 0.86V
- VRHot = Vcc
- EN=3.3V
- Sequence
- 1.2.3 first
- En signal
- V18A= 1.8V



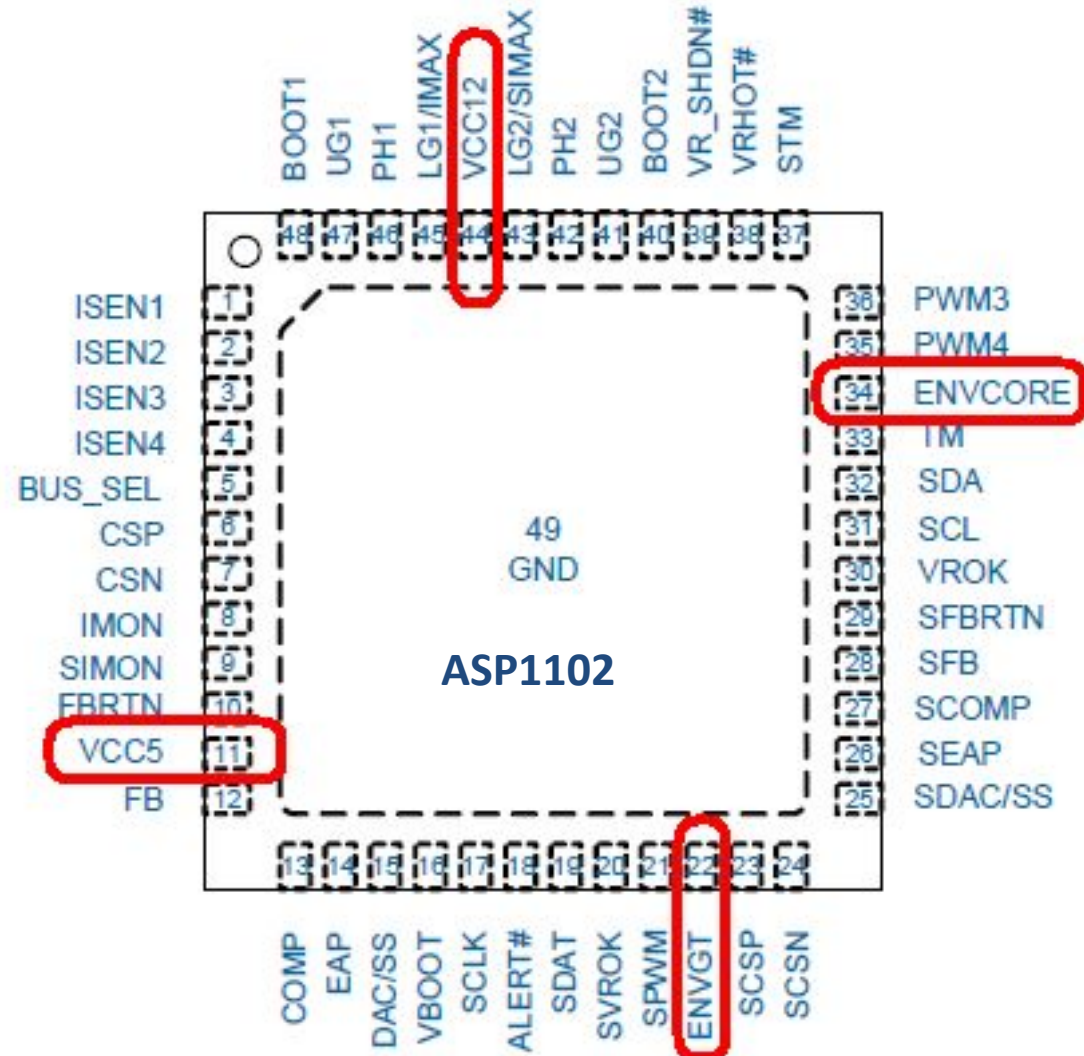
# ASP1000RM

- $V_{CC} = 5V$
- $DVD = 1.5V \geq 1.11$
- $DVDA = 1.33V \geq 1.11$
- $EN = V_{CCIO} \doteq 1.05$
  
- Sequence
- 1.2.3 first
- EN signal

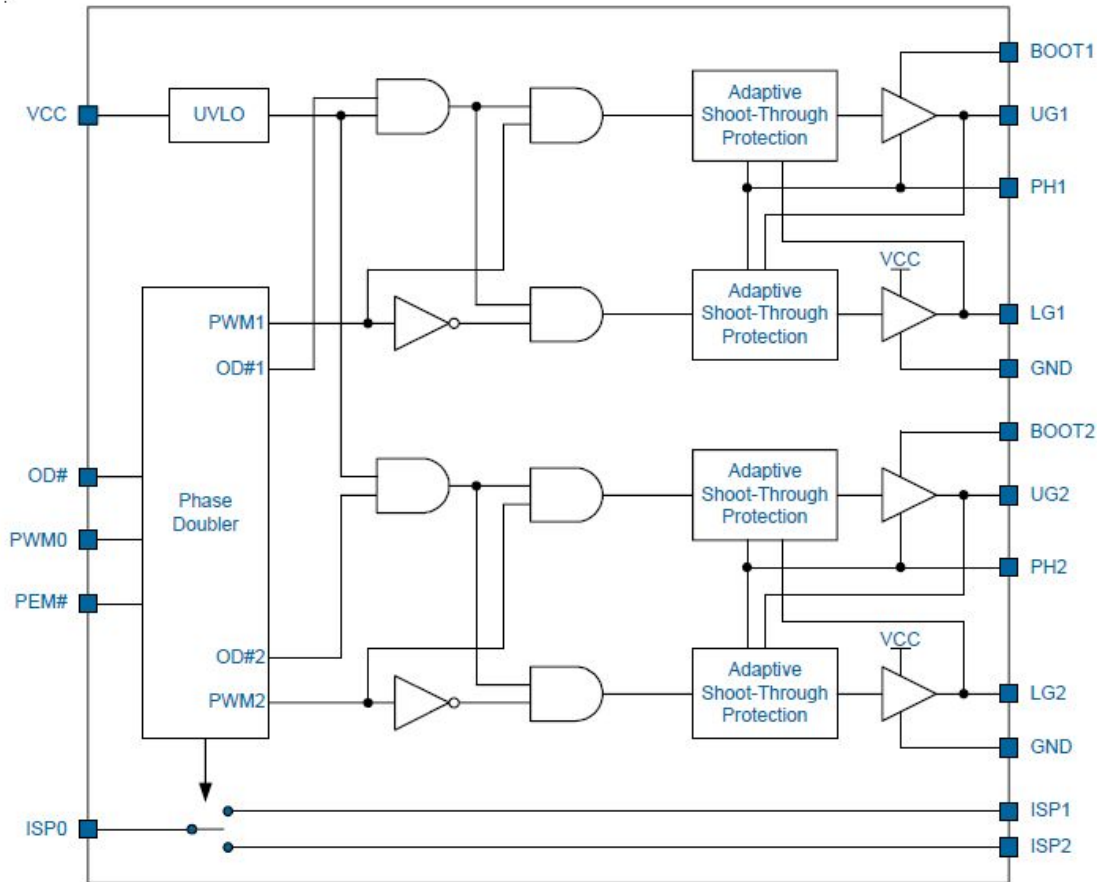


# ASP1102

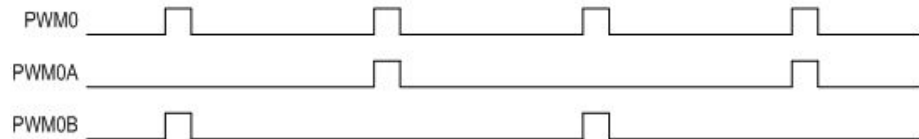
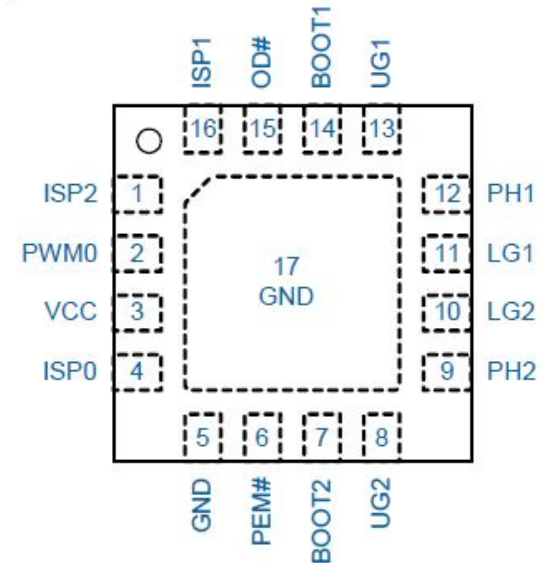
- Vcc5= 5V
- Vcc12= 12V
- EN=VCCIO  $\doteq$  1.05V
- Sequence
- 1.2 first
- EN signal



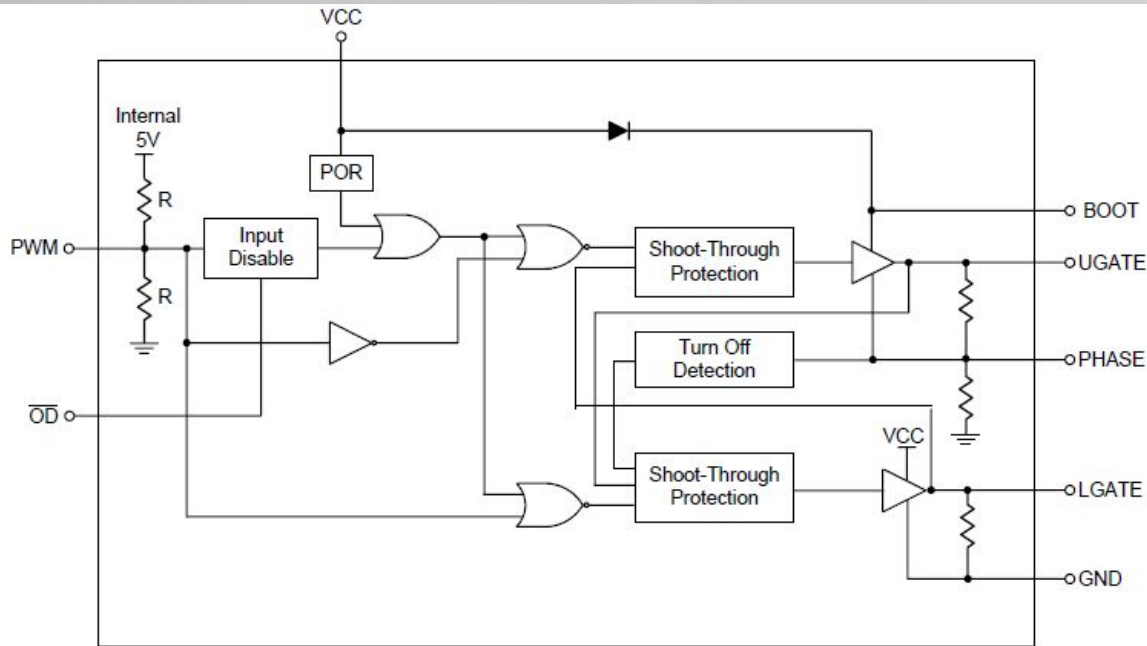
# VCORE Driver (ASP0A13)



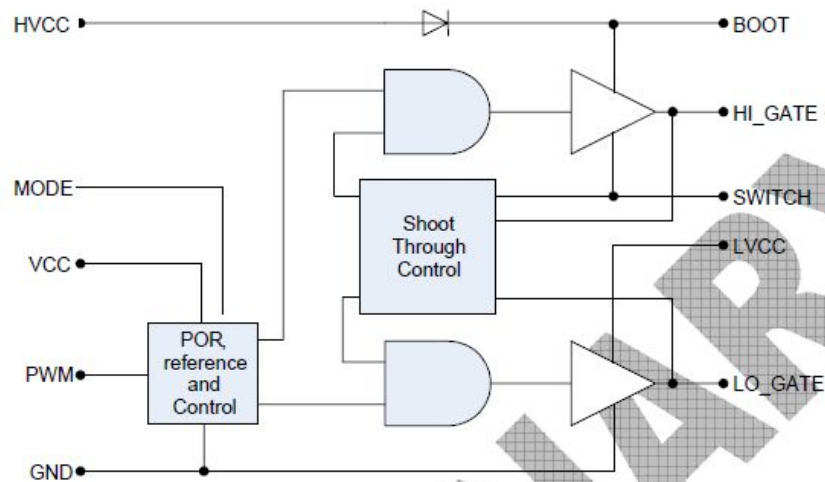
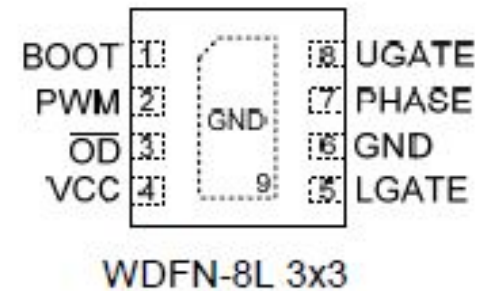
**ASP0A13**



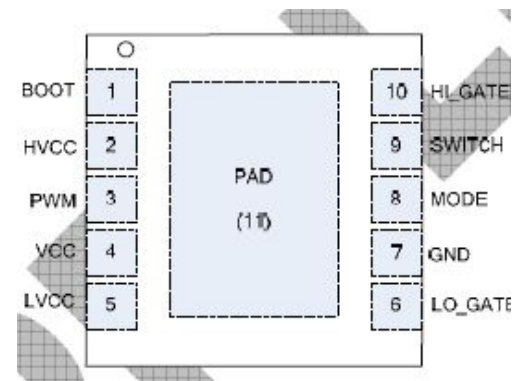
# VCORE Driver (ASP0A13)



**RT9611**

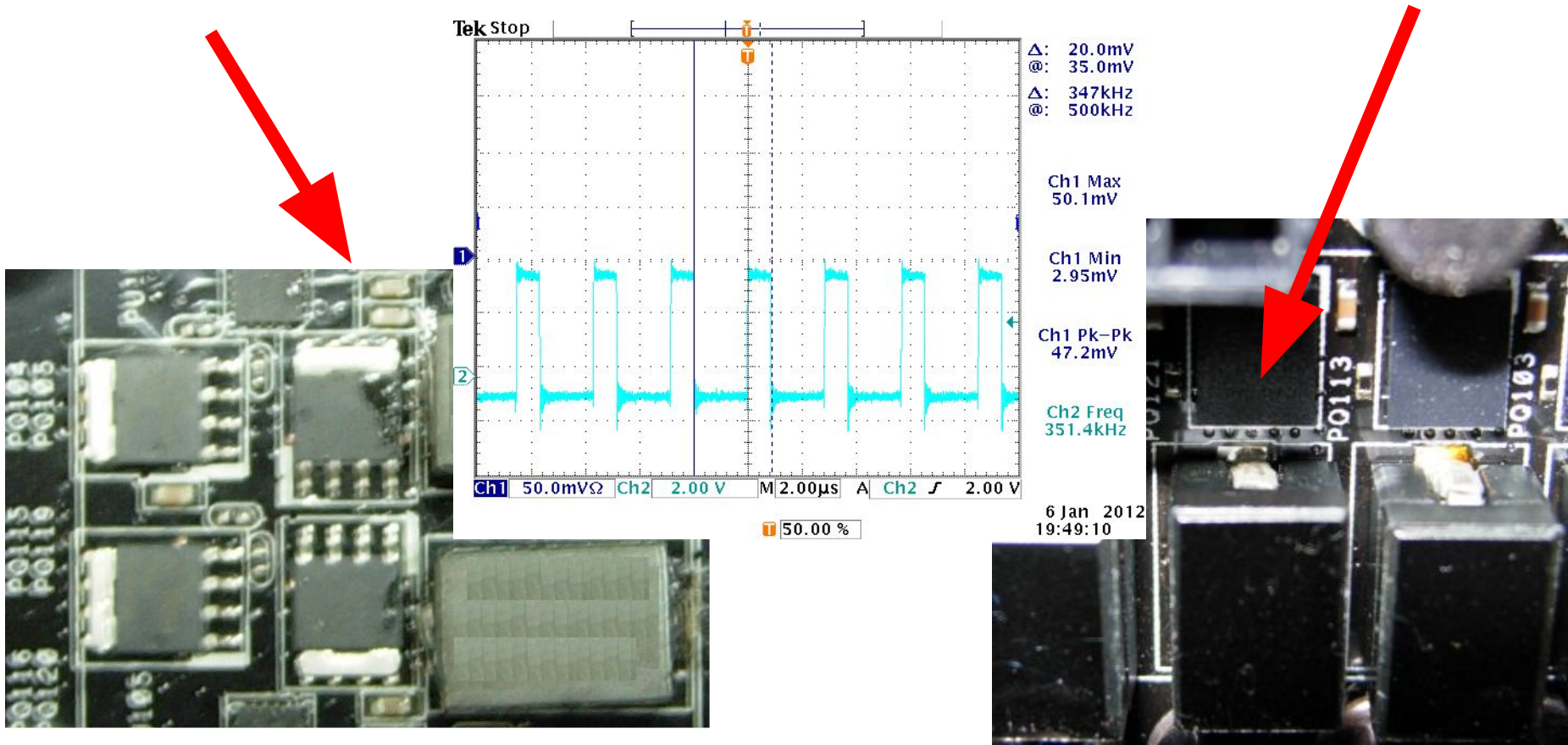


**IR8510**



# Debug - Vcore Repairing

- Vcore voltage output of each phase must have the correct waveform
- Empty board boot to Vcore is about 1V boot voltage .
- After installing CPU, it is set with the SVID voltage, so the value is different.
- Vcore run normally, but still halts at 00=>check PG signals.

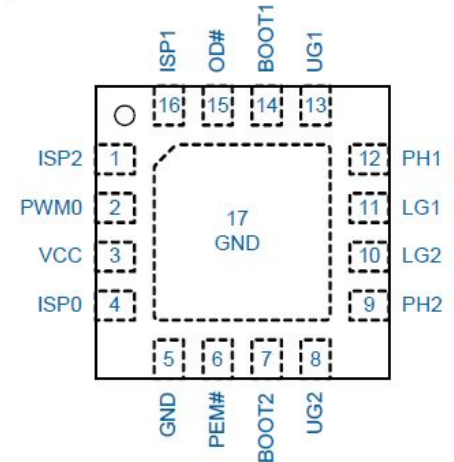




# Debug - Driver and Component

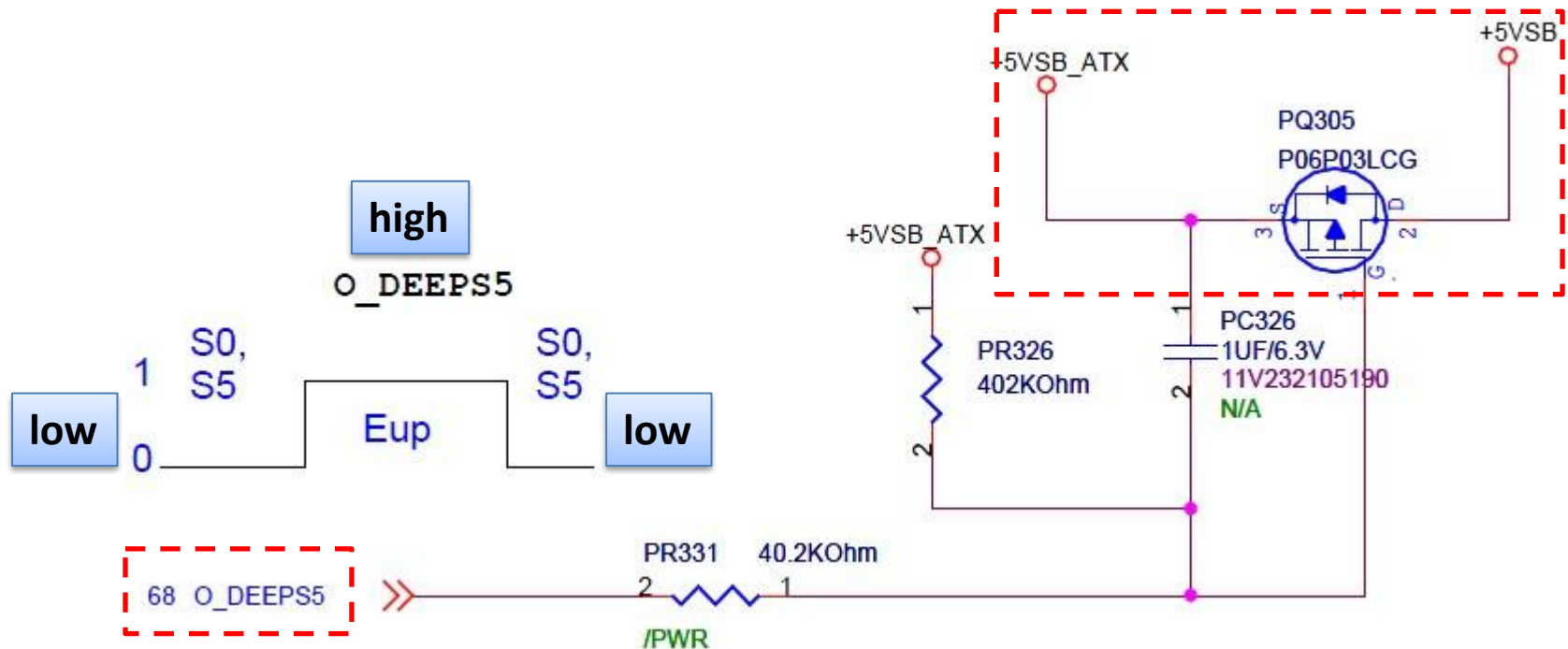
## If you suspect that other components are burned, such as the Driver

- To see whether the appearance of any abnormalities.
- Impedance measure:  
Measuring the ESD diodes, the terminal is connected to GND.
- To remove the component measurement is abnormal compared to the impedance and normal components of each pin to ground.
- If Vcore is short circuit and +3.3 V is short circuit, SIO may have burned.

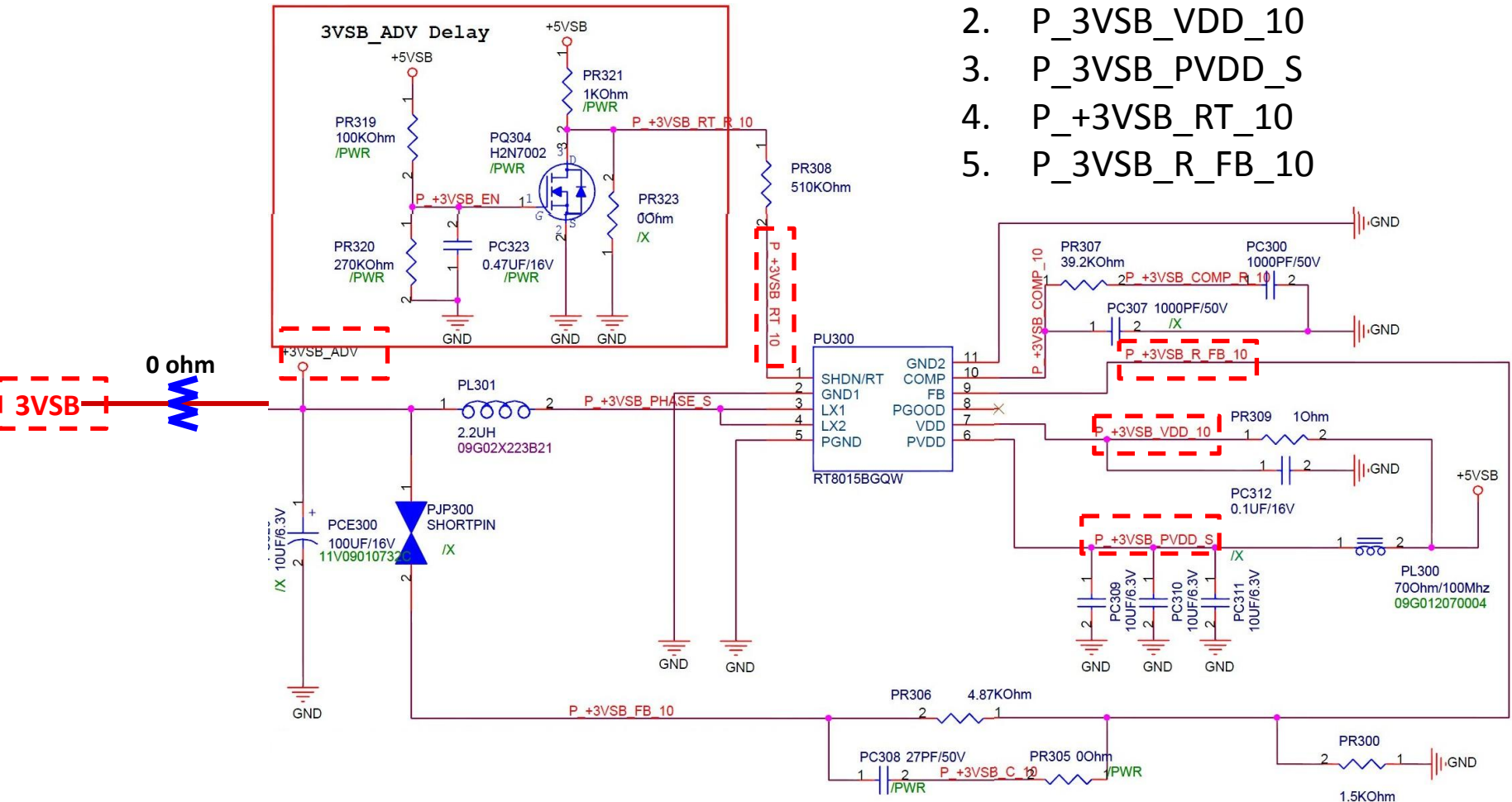


# Debug – 5VSB

1. Clear COMS and let MB at load default status
2. Check +5VSB\_ATX
3. Check O\_DEEPS5 and PQ305



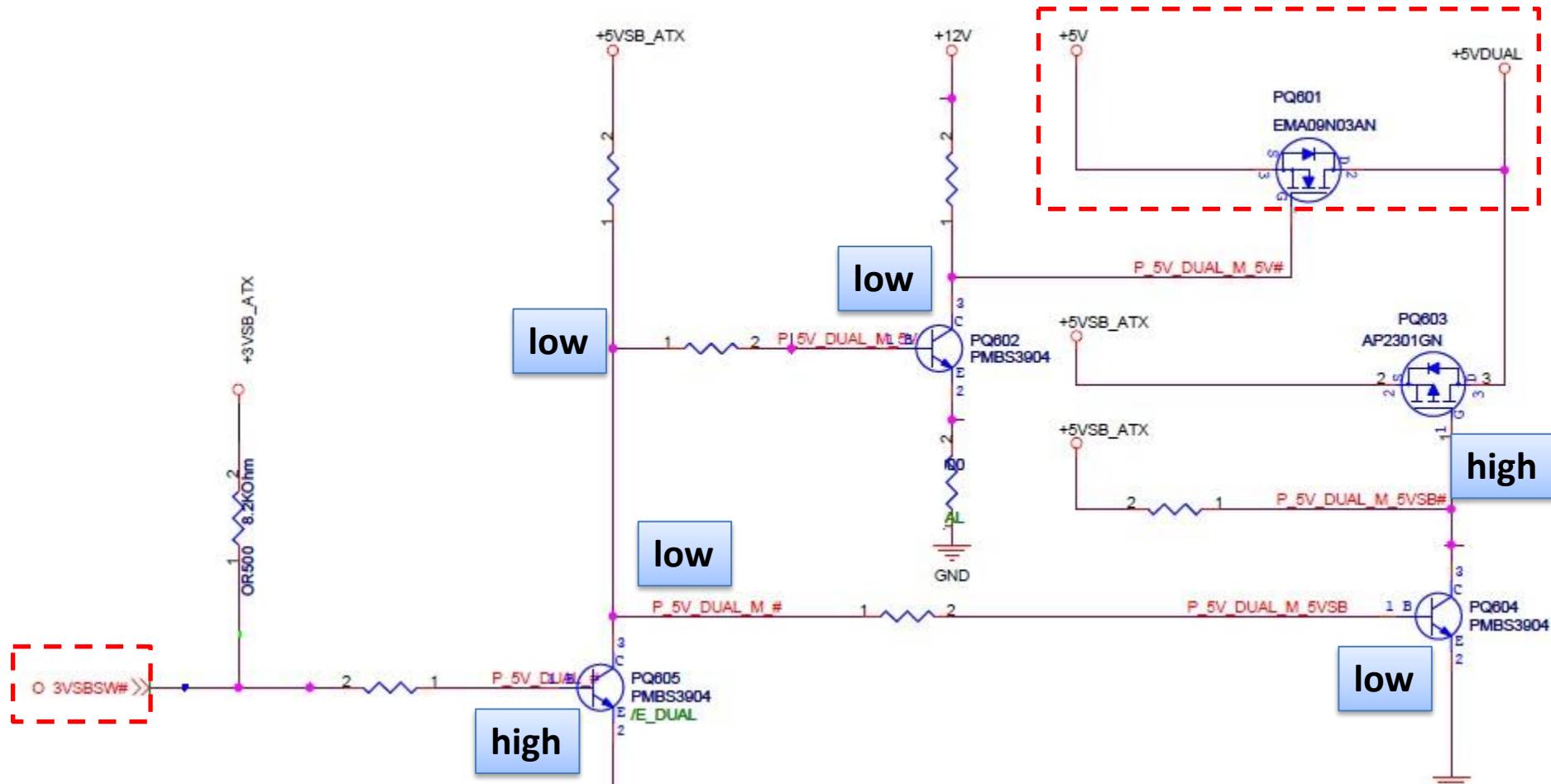
# Debug – 3VSB\_ADV & 3VSB



1. 5VSB
2. P\_3VSB\_VDD\_10
3. P\_3VSB\_PVDD\_S
4. P\_+3VSB\_RT\_10
5. P\_3VSB\_R\_FB\_10

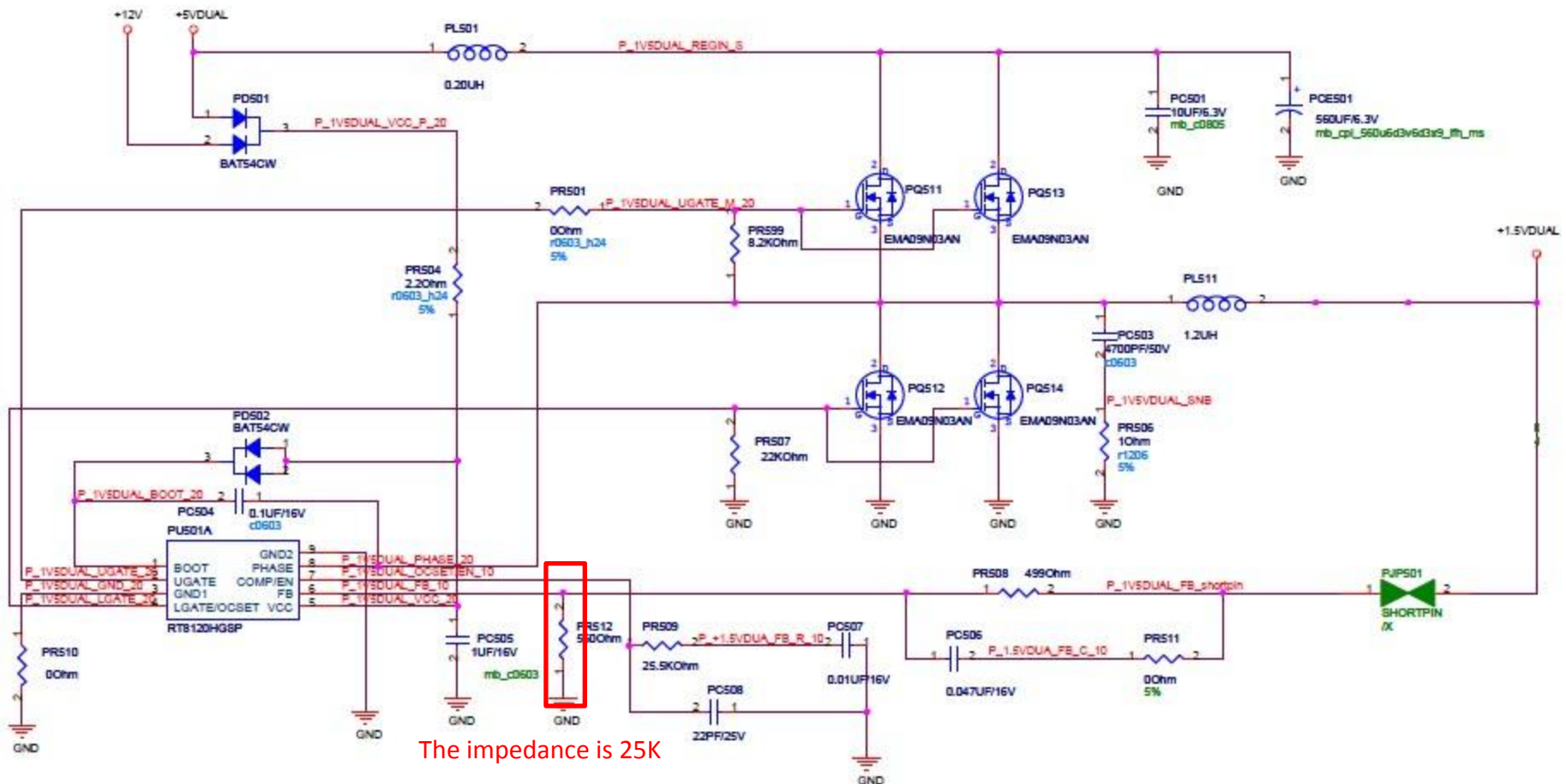
# Debug – 5VDUAL

1. Check O\_3VSBSW# (At S0 and S5 status, this signal has 3V)
2. Check PQ601 PIN1(12V) and PIN3(5V)

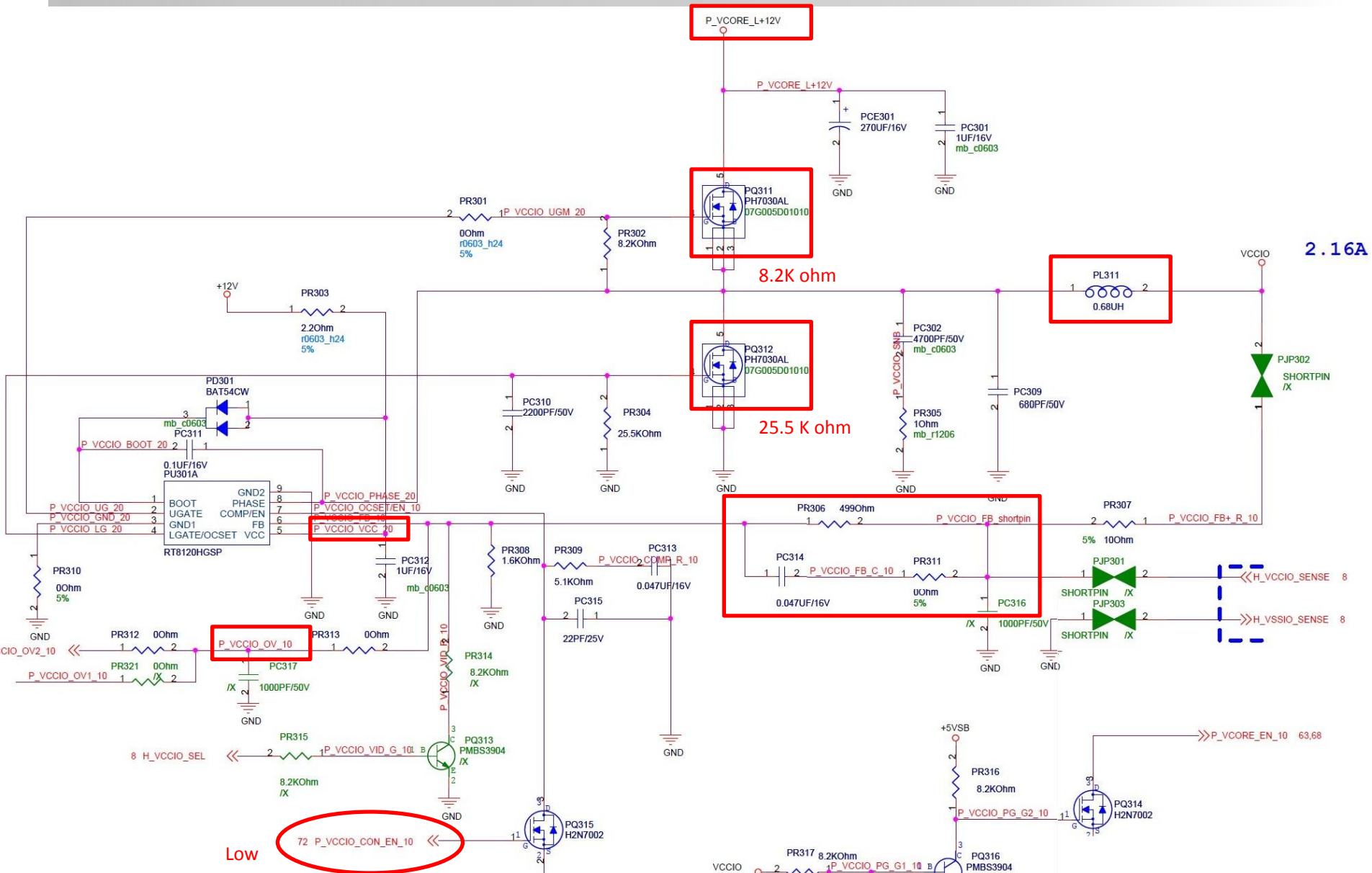


# Debug – 1.5VDUAL

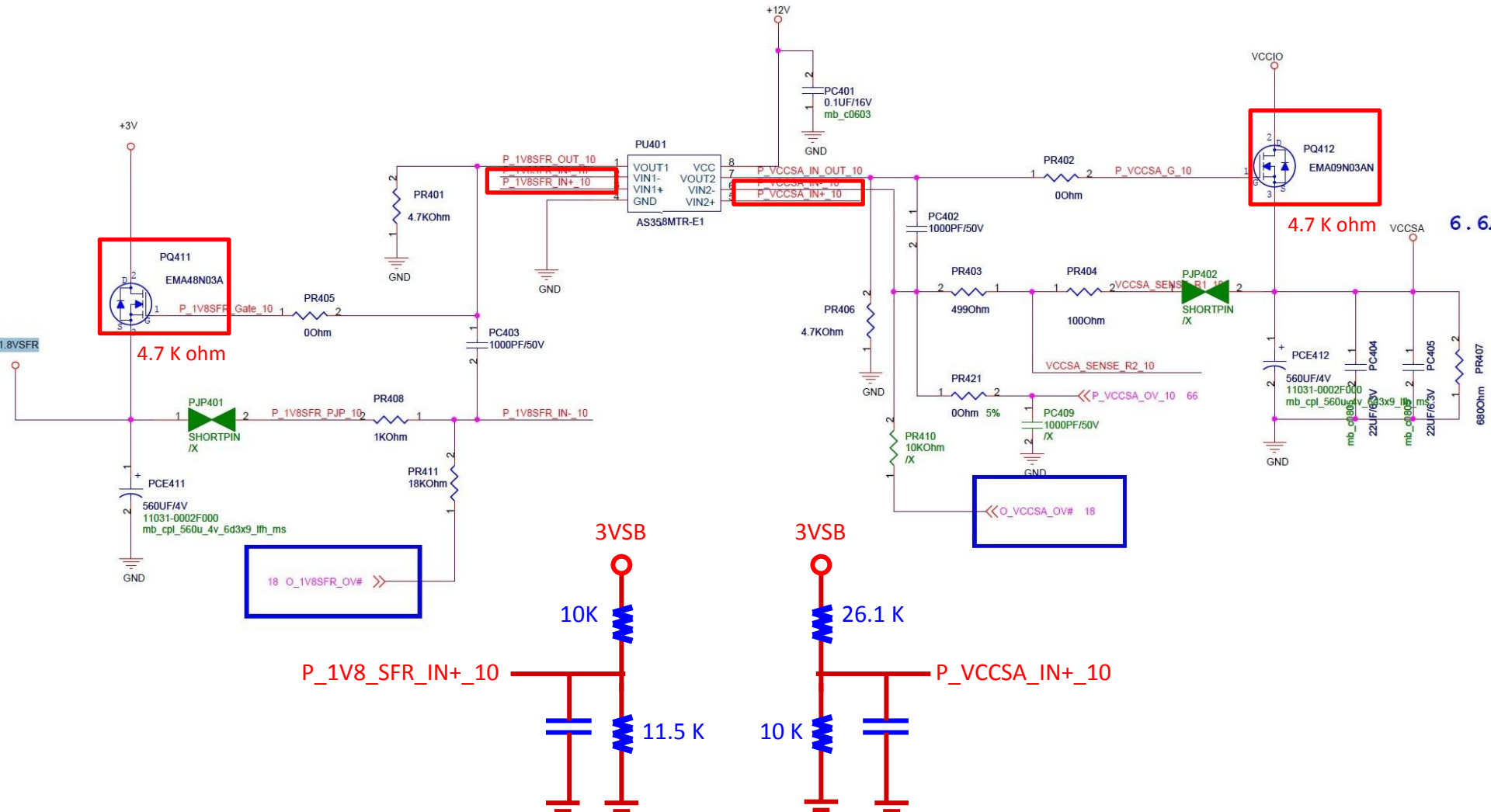
1. 5VDUAL and PU501 VCC
2. Check P\_1V5DUAL\_OCSET/EN\_10
3. Check MOS
6. Check P\_1V5DUAL\_FB\_10 has 0.8V
7. Check NCT3933 working condition (VCC, S\_SMBDATA\_VSB, S\_SMBCLK\_VSB)



# Debug – VCCIO



# Debug – 1.8SFR & VCCSA



**Thank You!**