Behavioral Modeling of Data Converters using Verilog-A

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Agenda

- Introduction
- Verilog-A
- Objectives
- Sample and Hold
  - Analysis
  - Jitter Noise
  - Thermal noise
  - Model
  - Simulation results
- Generic DAC
  - Analysis and model
  - Dynamic element matching
  - Simulation results

Agenda

- Generic ADC
  - Analysis and model
  - Simulation results
- Flash ADC
  - Analysis and model
  - Simulation results
- SAR ADC
  - Analysis and model
  - Simulation Results
- Pipelined ADC
  - Analysis
  - 1.5 bit Stage
    - 1.5 bit ADC

Agenda

- 1.5 bit MDAC
- Digital Correction
- Simulation results

- ΣΔ ADC
  - ΣΔ Modulator
    - SC integrator analysis
    - Model
    - Simulation results
- Conclusions
- Future Work
- Acknowledgements
- References

Introduction

- Transistor-level modeling and simulation is the most accurate approach for mixed-signal circuits.
- It becomes impractical for complex systems due to the long computational time required.

Cell View	No. of Transistors	No. of Equations	Simulation Time
Transistor Level	436	1111	52 s
	7000	17601	125 ks 1 day, 10 hours, 42 min.

Taken form the article: Efficient Testing of Analog/Mixed-Signal ICs using Verilog-A
Nitin Mohan, Sirific Wireless www.techonline.com

Introduction

- This situation has led circuit designers to consider alternate modeling techniques:

Approach	Accuracy	Speed	Flexibility
Device models	☺	☹	😐
Custom C++ models	😐	☺	☹
Finite-difference equations	😐	☺	😐
Circuit-based macromodels	☺	😐	☺
Time-domain macromodels	☺	😐	☹
Behavioral models	☺	☺	☺

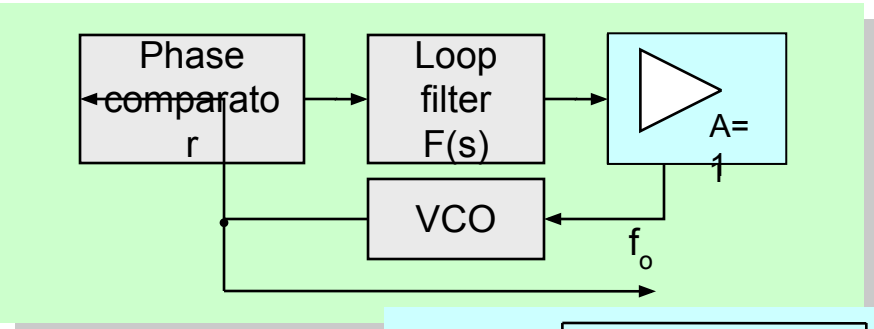
Cell View	No. of Transistors	No. of Equations	Simulation Time
Transistor Level	436	1111	52 s
Behavioral	270	697	4 s
Transistor Level	7000	17601	125 ks 1 day, 10 hours, 42 min.
Behavioral	439	1148	124s

www.techonline.com **Efficient Testing of Analog/Mixed-Signal ICs using Verilog-A, Nitin Mohan, Sirific Wireless**

- In addition, behavioral modeling can be effectively used in a top-down design approach.

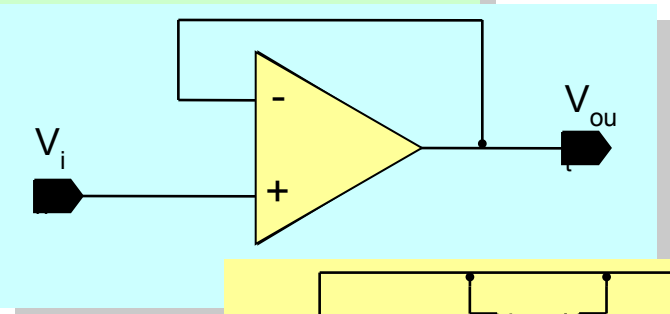
Introduction

System Level
(Matlab, C++, SystemC, AHDLs, etc…)

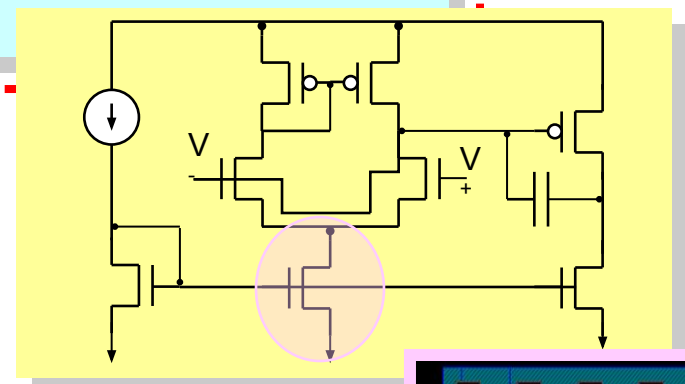


Behavioral models

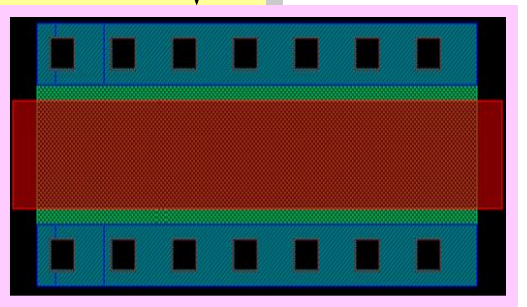
Functional Level (SPICE, AHDLs)



Transistor Level (SPICE)



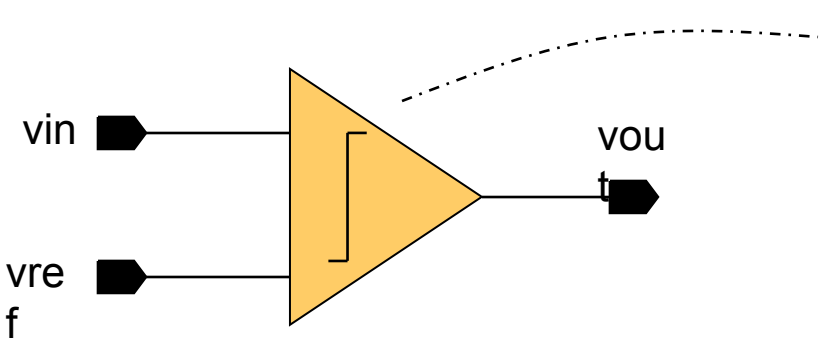
Layout



Top-Down Design Approach

Verilog-A

- The Verilog-A is a high-level language developed to describe the structure and behavior of analog systems and their components.
- It is an extension to the IEEE 1364 Verilog HDL specification for digital design.
- The analog systems are described in Verilog-A in a modular way using hierarchy and different levels of modeling complexity.
- The motivation is to invest in a new higher level of abstraction in analog design and its combination with the digital one.




```
`include "constants.vams"
`include "disciplines.vams"

module COMP (vin, vref, vout);
output vout;
electrical vout;
input vin;
electrical vin;
input vref;
electrical vref;
parameter real slope = 100.0;
parameter real offset = 0.0 ;
```

Objectives

- Build a set of analog and mixed-signal behavioral models using the Verilog-A AHDL, that allows a high level simulation of ADCs.
- Simulate some popular ADCs architectures such as:
  - Flash ADC
  - SAR ADC
  - Pipelined ADC
- Simulate other common used mixed-signal circuits such as:
  - $\Sigma\Delta$ Modulator
  - Sample and Hold
- Provide a general modeling approach for noise sources and other non-idealities.
- Provide performance results for the simulated data converters such as spectrum measures SNR, SNDR, THD etc.

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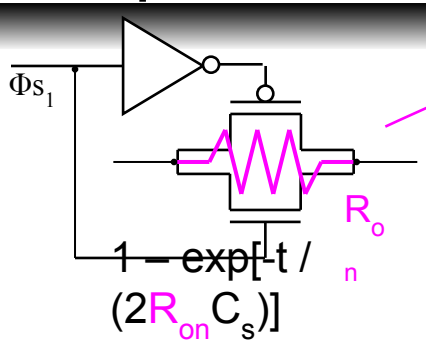
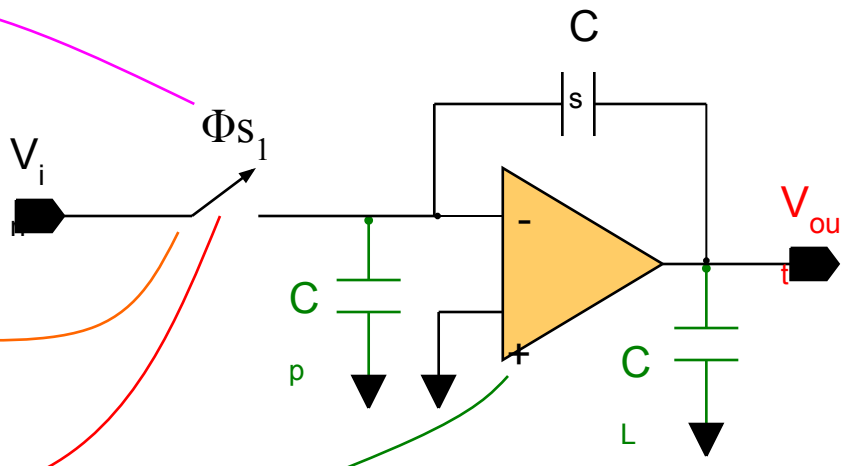
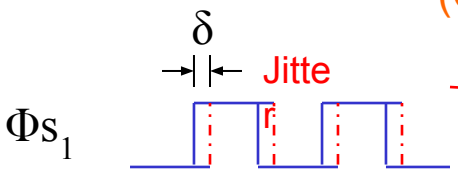
Sample and Hold





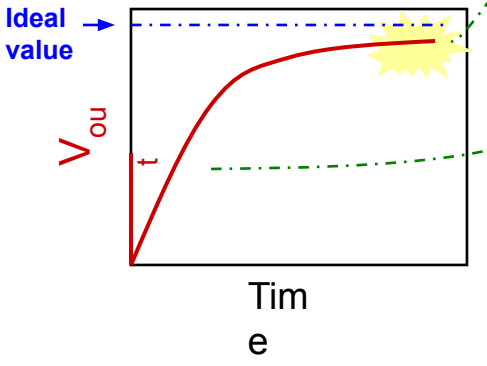
Thermal noise
$V_{th} \approx kT/C_s$
(Opamp noise neglected)

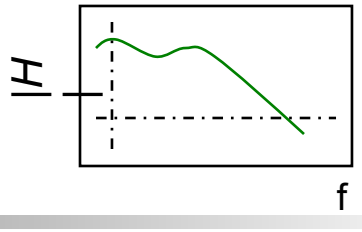


$x(t+\delta) - x(t) \approx \delta \quad x(t)$

$\varepsilon_g = 1 - C_s /[\, C_s + (C_s + C_p)/A_0]$

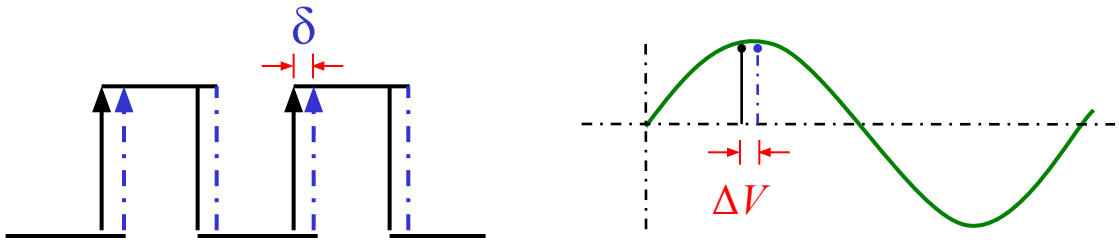
- Finite DC gain A_0
- Finite GBW
- C_p and C_L
- Defective settling
  - Linear
  - Slewing
  - Partial Slewing





Jitter Noise

- Clock jitter is due to the non-uniform sampling of the input signal.



- The magnitude of this error is a function of the statistical properties of the jitter and the input signal to the system.

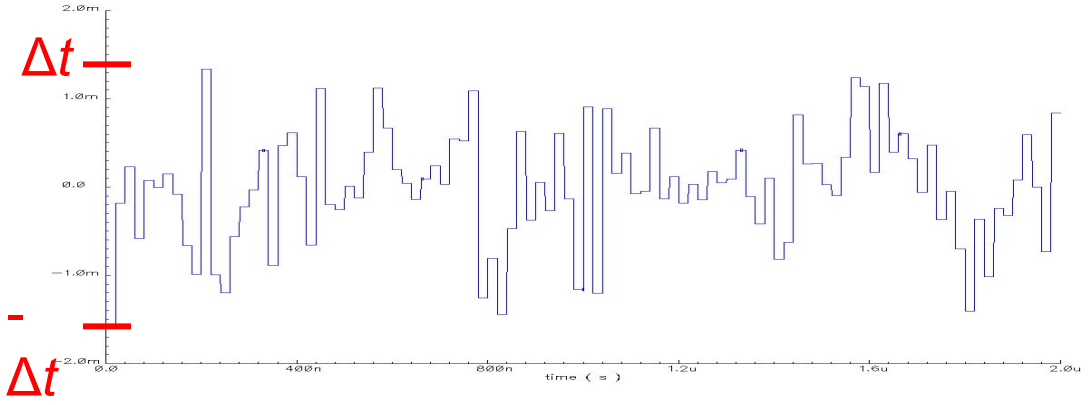
- In sampled data systems, when a sinusoidal input is taken, the error introduced by jitter can be modeled by,

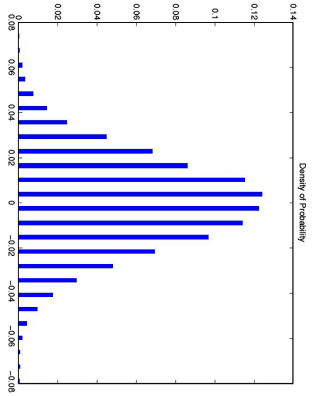
$$x(t+\delta) - x(t) \approx 2\pi f_{in}\,\delta A\cos(2\pi f_{in} nt) \approx \delta \qquad x(t)$$

where δ is the sampling uncertainty, this is taken to be a Gaussian random process with standard deviation Δt.

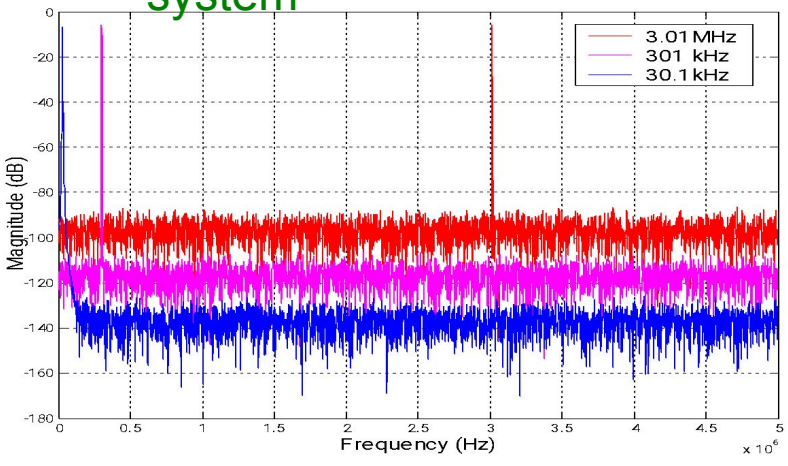
Jitter Noise

- It is assumed that is a Gaussian random process with zero mean and standard deviation Δt.

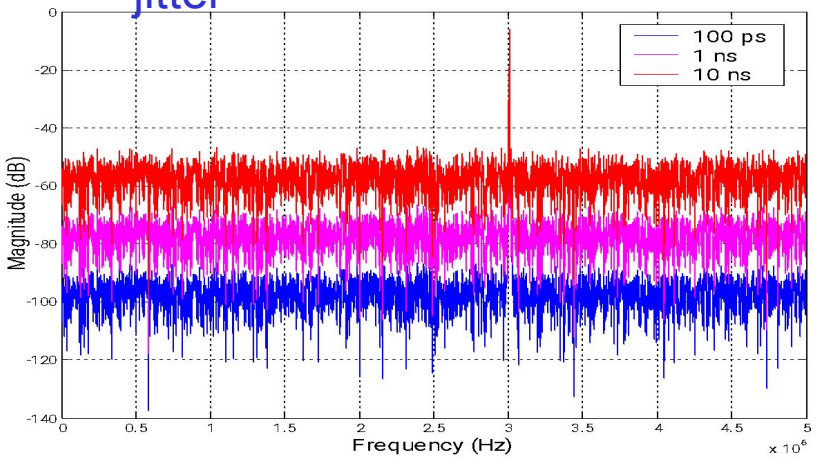




Input signal to the system

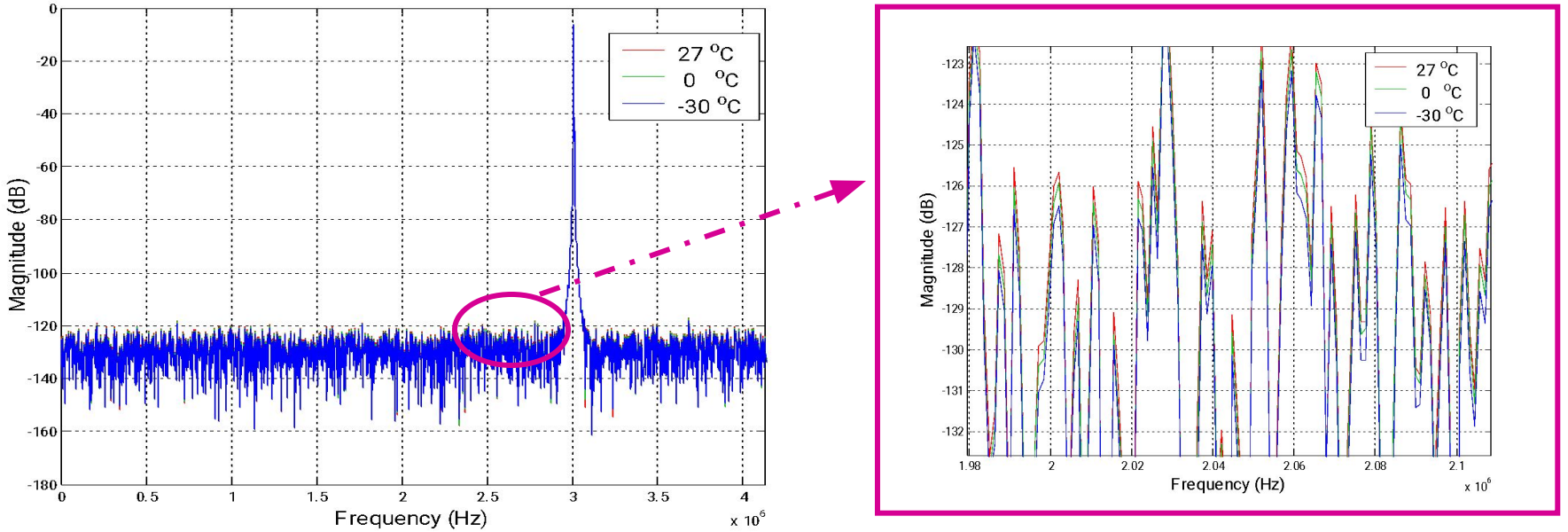


Statistical properties of the jitter

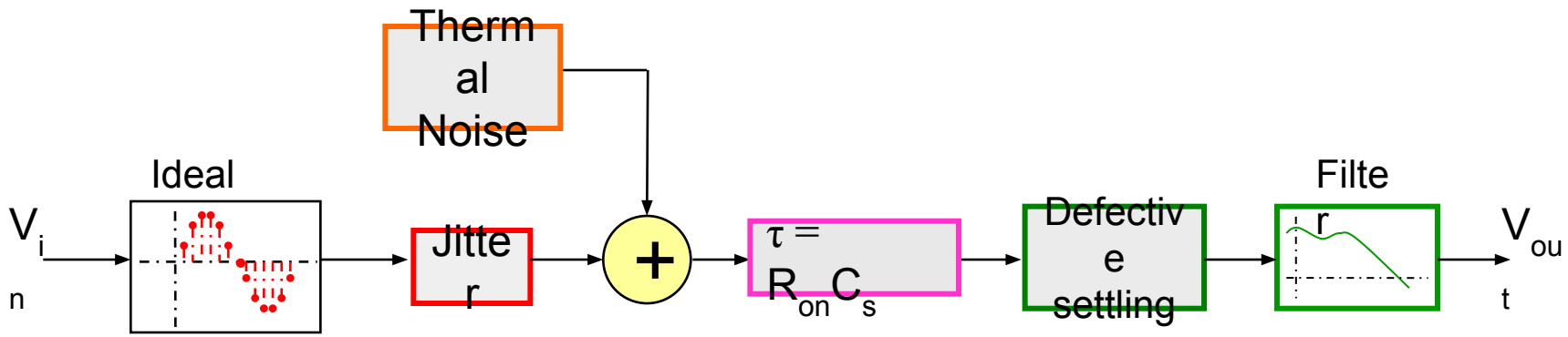


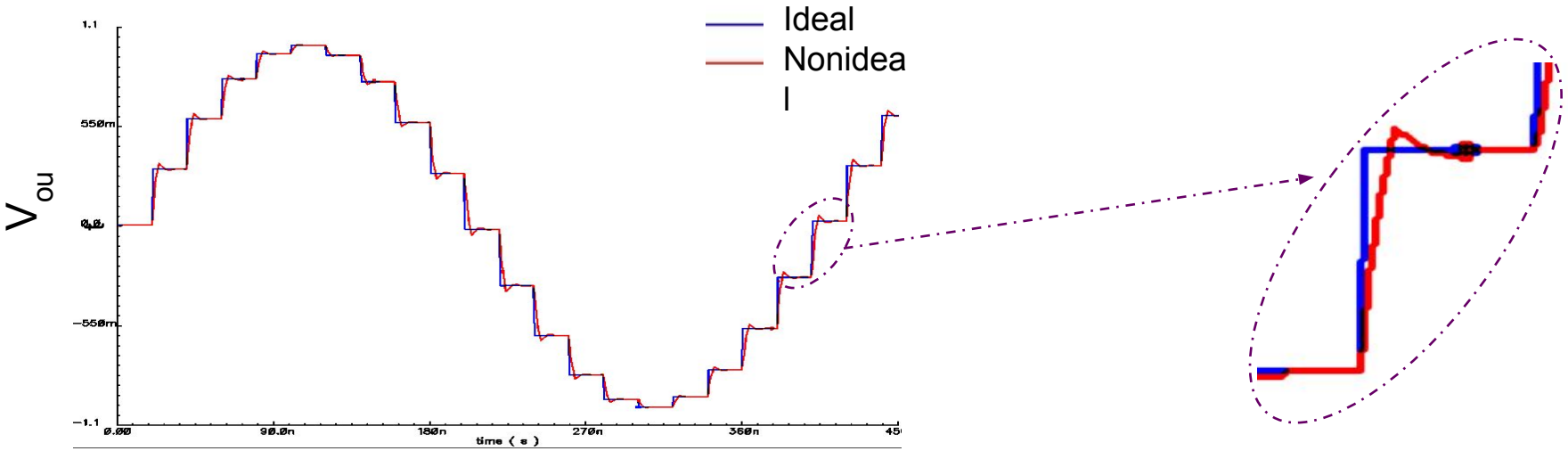
Thermal Noise

- Thermal noise in circuits is because of the random fluctuation of carriers due to thermal energy.
- Proportional to the temperature.
- It is assumed to be a Gaussian random process with zero mean.

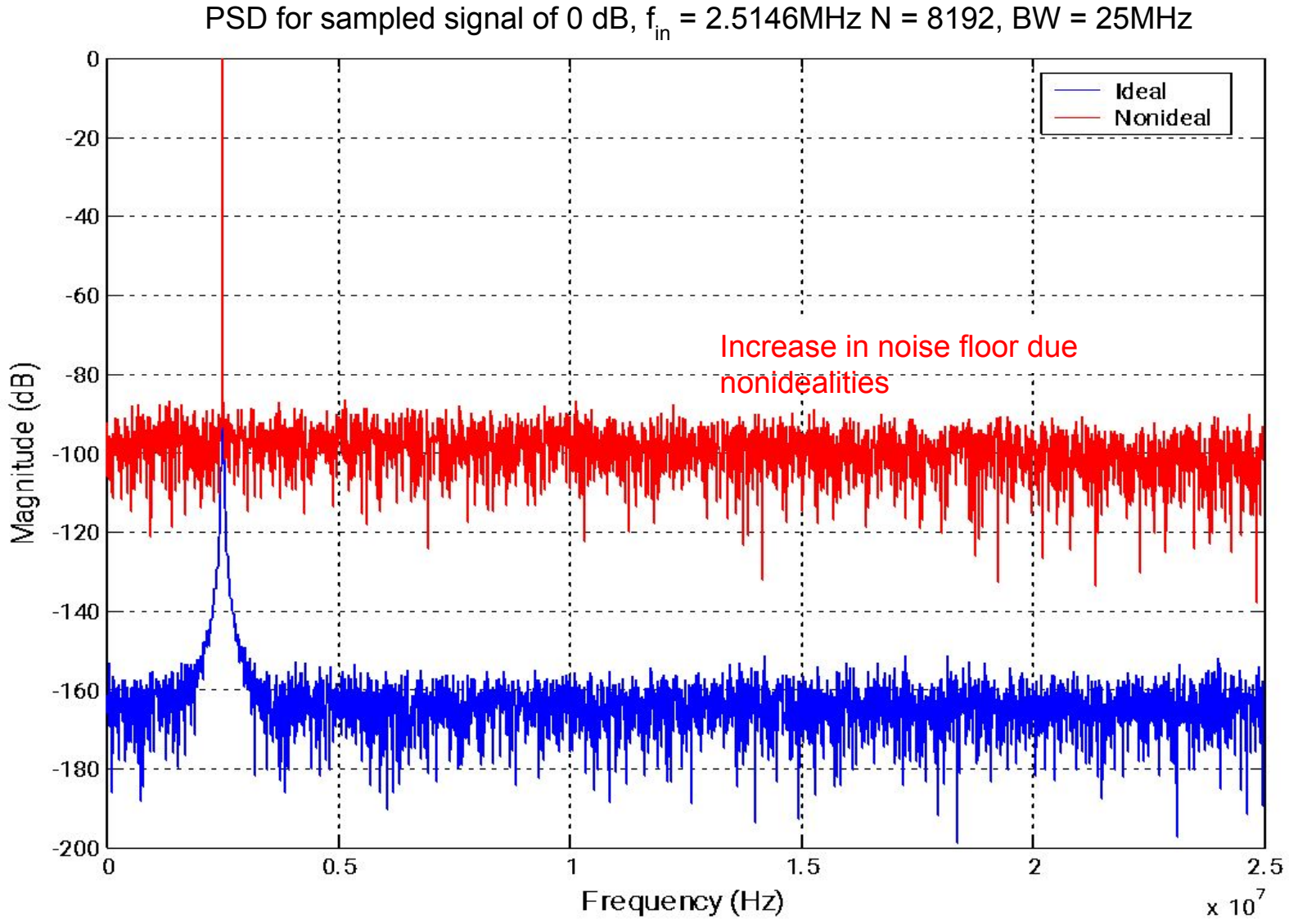


Sample and Hold model





Sample and Hold simulation results



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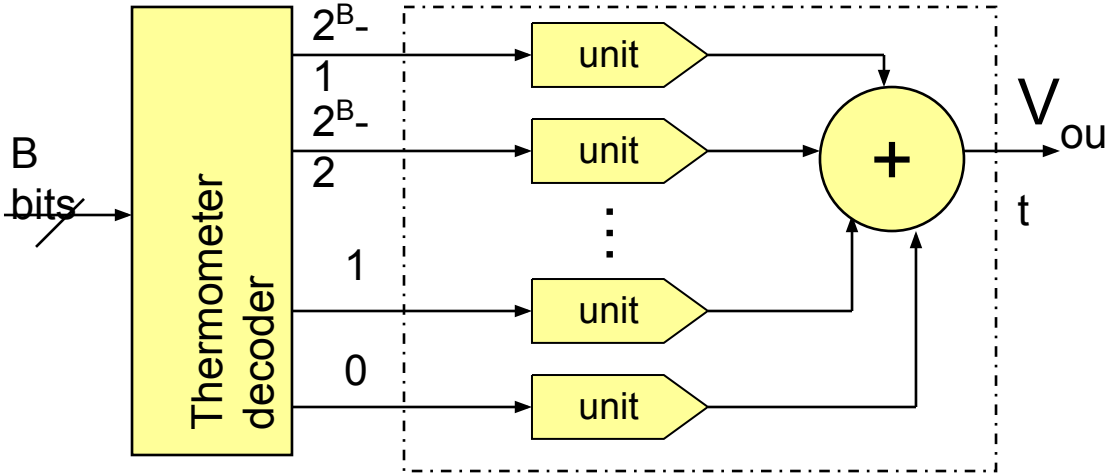
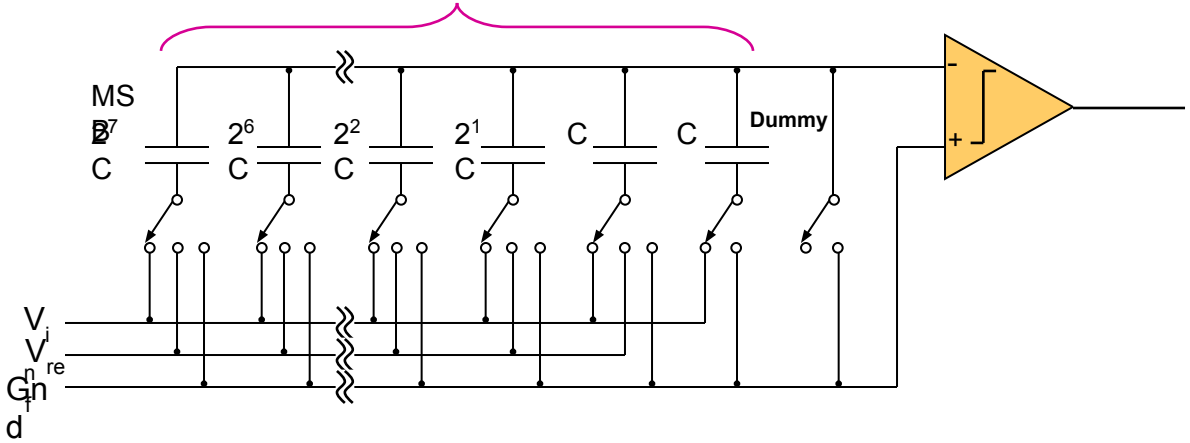
Generic DAC

- Mismatch in DAC units.
- INL
- Gain error
- Offset

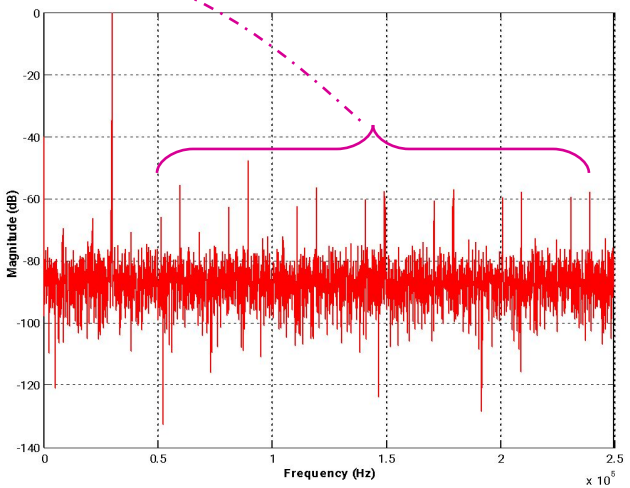


Generic DAC model including mismatch in units

Mismatch in capacitors!
(trimming can reduced it to 0.1%
Increase in harmonics content)



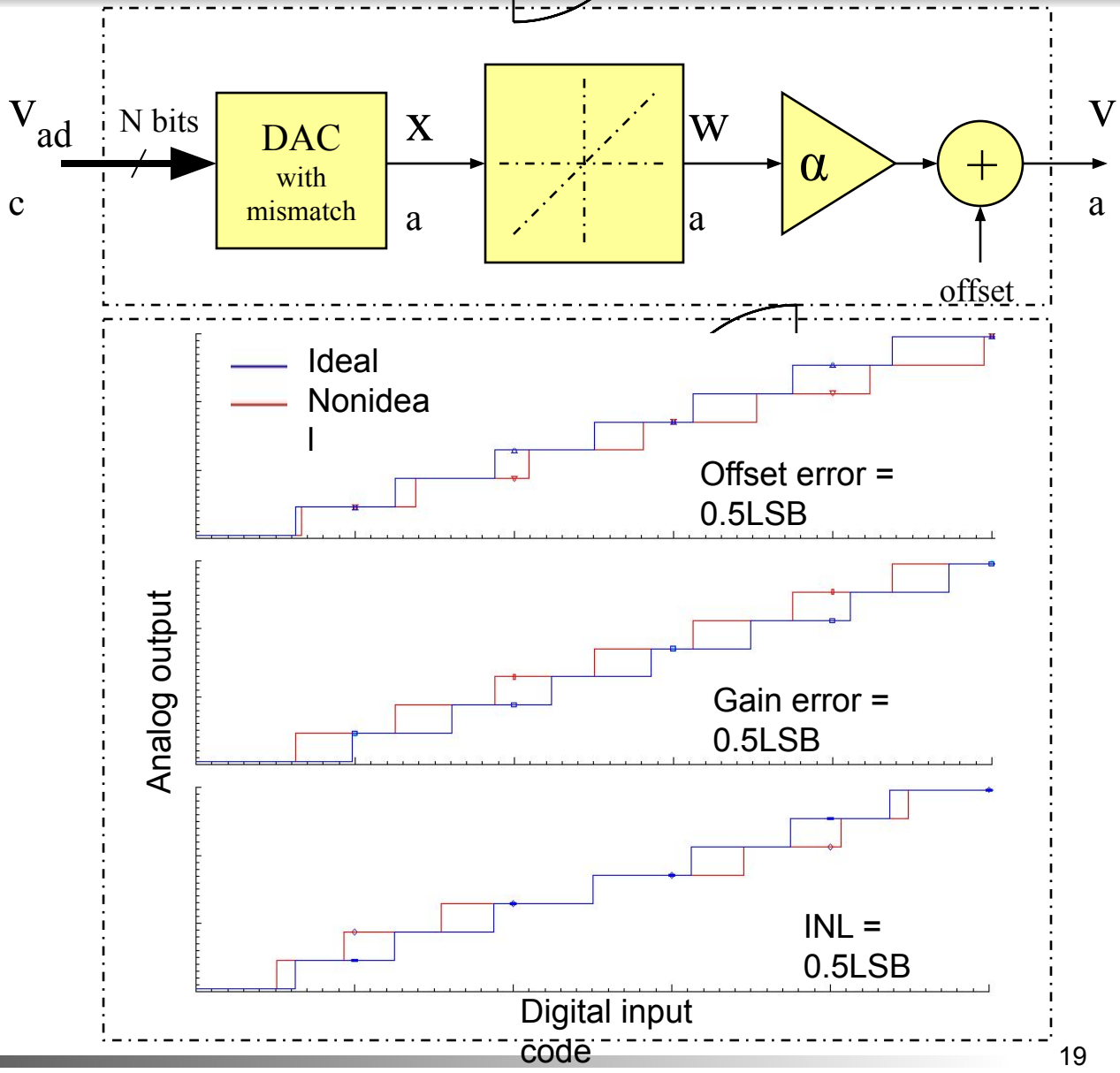
SAR Capacitive DAC, SAH and comparator



Generic DAC model

g	nominal gain
ε_g	Gain error
q	Quantization step
INL	Integral non-linearity
ε_{off}	Offset error
FS	Full scale voltage

l_1	-FS/(2g)
q	$FS/(2^N-1)$
A	$(2^{N-1}-1)q$
α	$1/(1+q\ \varepsilon_g)$
offset	$(l_1\ \varepsilon_g-\varepsilon_{off})q$
ε_0	$(INL)sqrt(27)/(2^N-2)$
w_a	$(1-\varepsilon_0)x_a + x_a^3\ \varepsilon_0/A^2$
y_a	$\alpha(w_a + off)$

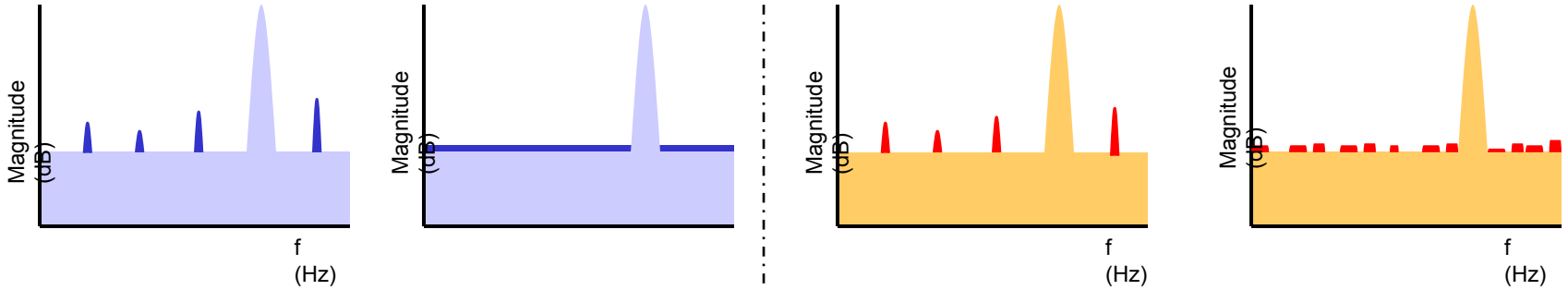


DEM

- Dynamic Element Matching (DEM) techniques are used to minimize the effect of DAC units mismatch.
- DAC DEM techniques can be divided in deterministic and stochastic.

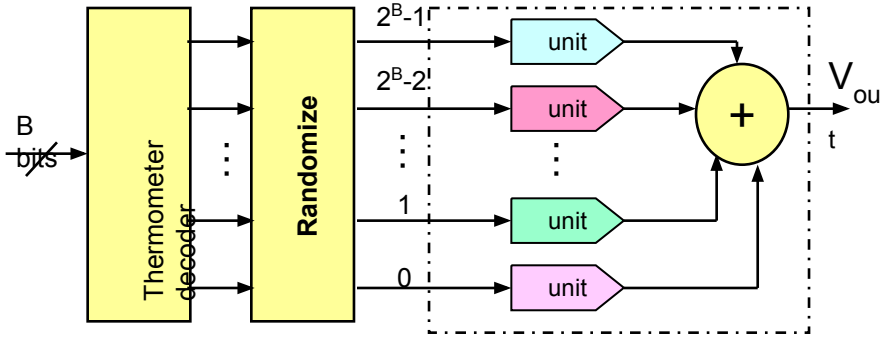
Spread the mismatch error energy across the spectrum generating white or colored noise in the DAC output.

Improve the DAC performance by locating the distortion caused by the component mismatch errors in certain frequency bands.



- Due to design complexity and non-scalability for modeling purposes it is easier to implement a general stochastic approach using randomization.

DEM simulation results

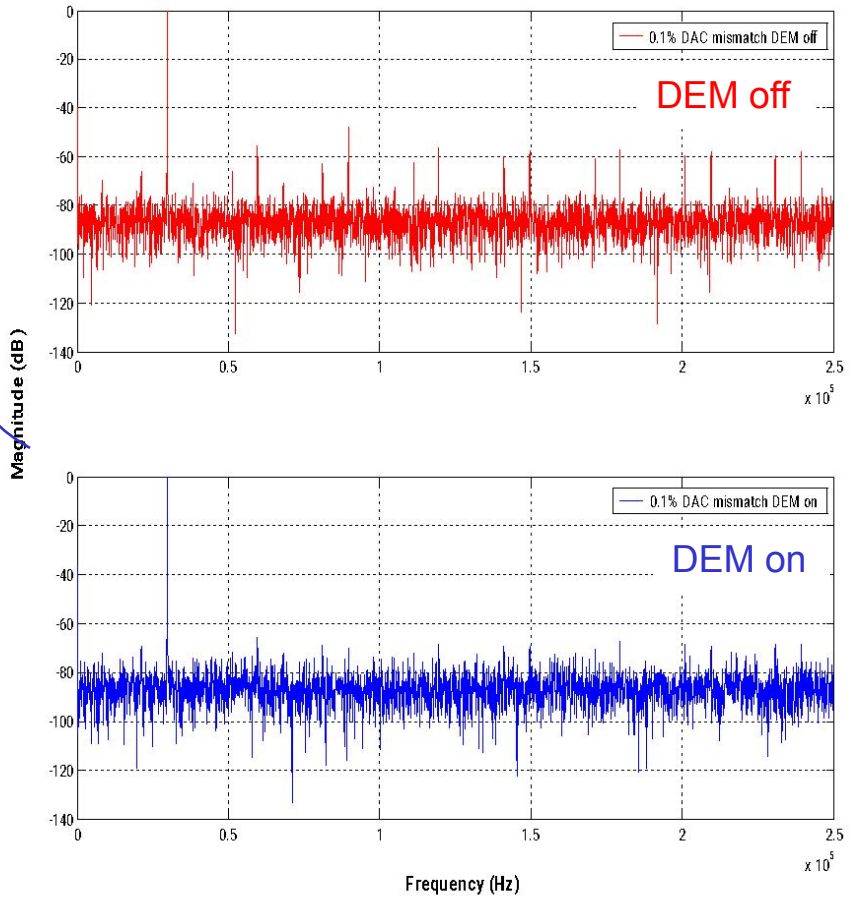


By randomizing the DAC units (i.e. using a digital circuitry FSM with a system clock) the effect of the mismatch in the spectrum is reduced by reducing the harmonic distortion.

In Verilog-A its rather simple to randomize uniformly the units. Assuming we have a system clock, for each rising edge of the clock signal we randomize the units.

```
if(DEM_enable) begin
     generate i(1,`DAC_UNITS) begin
        temp = $dist_uniform(seed, 1, `DAC_UNITS);
        if(temp - floor(temp) >= 0.5)
            DEM[i] = ceil(temp);
        else
            DEM[i] = floor(temp);
     end
end
// Then select units stored in the array DEM[ ] for conversion
```

DAC 0.1% mismatch



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FS	Full scale voltage

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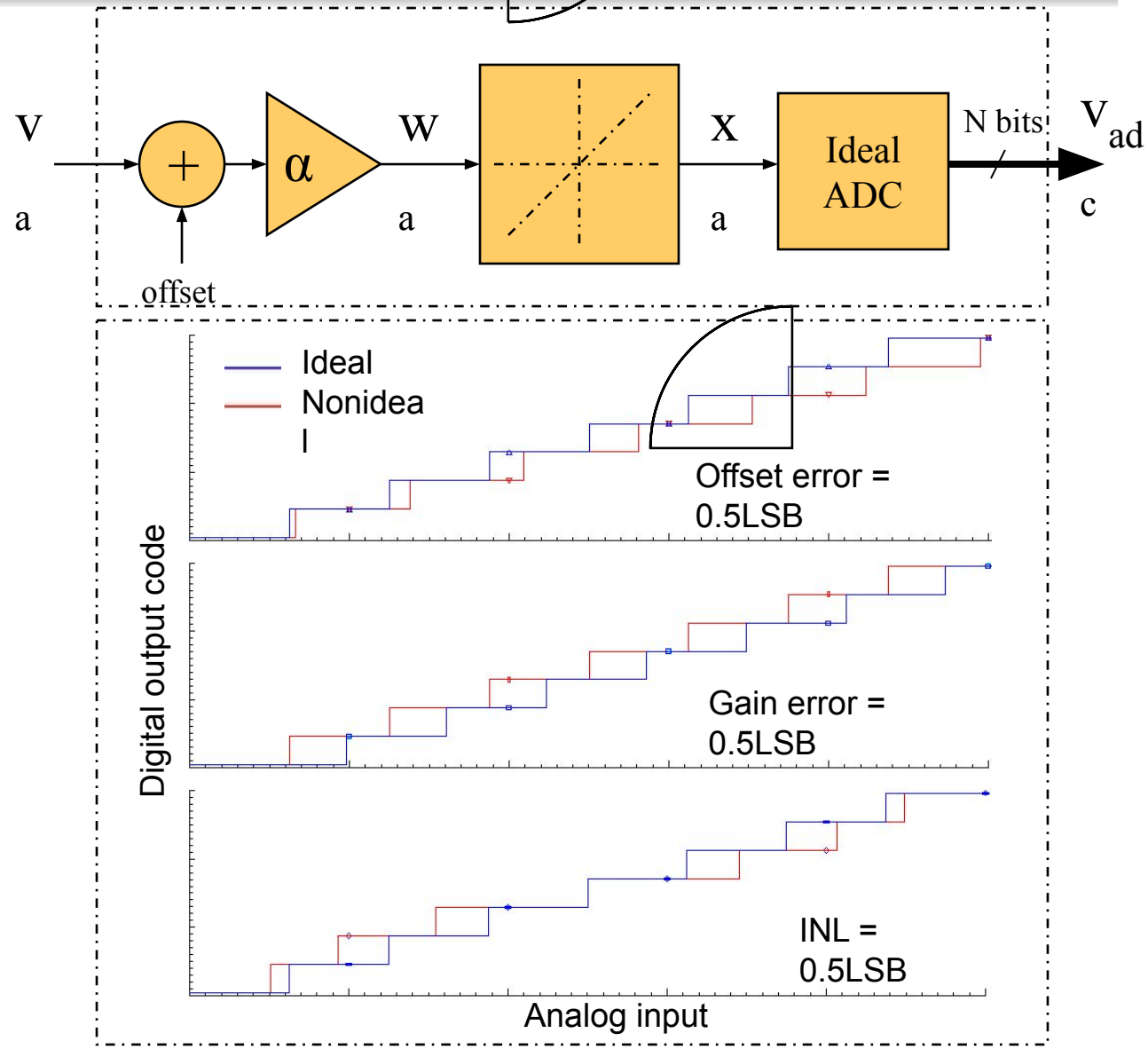
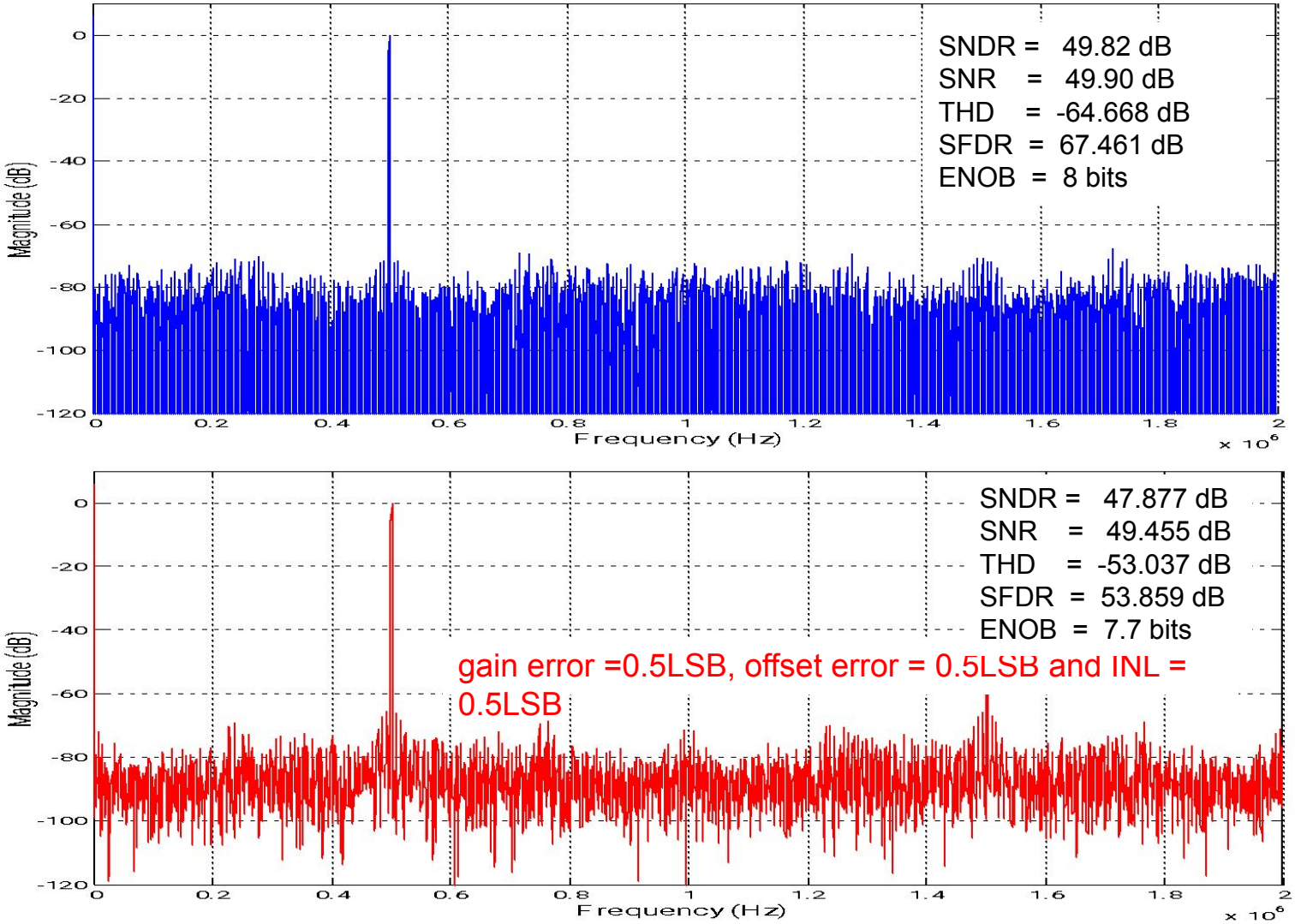
l_1	$-FS/(2g) + q/2$
A	$(2^{N-1}-1)q$
α	$1/(1+q\varepsilon_g)$
offset	$(l_1 \varepsilon_g-\varepsilon_{off})q$
ε_0	$(INL)sqrt(27)/(2^N-2)$
w_a	$\alpha(w_a + off)$
y_a	$(1- \varepsilon_0)x_a + x_a^3 \varepsilon_0/A^2$



Generic ADC simulation results

PSD plot for 8-bit generic ADC with 0 dB input signal f_{in} of 500.977KHz, Samples = 8192, BW = 2MHz



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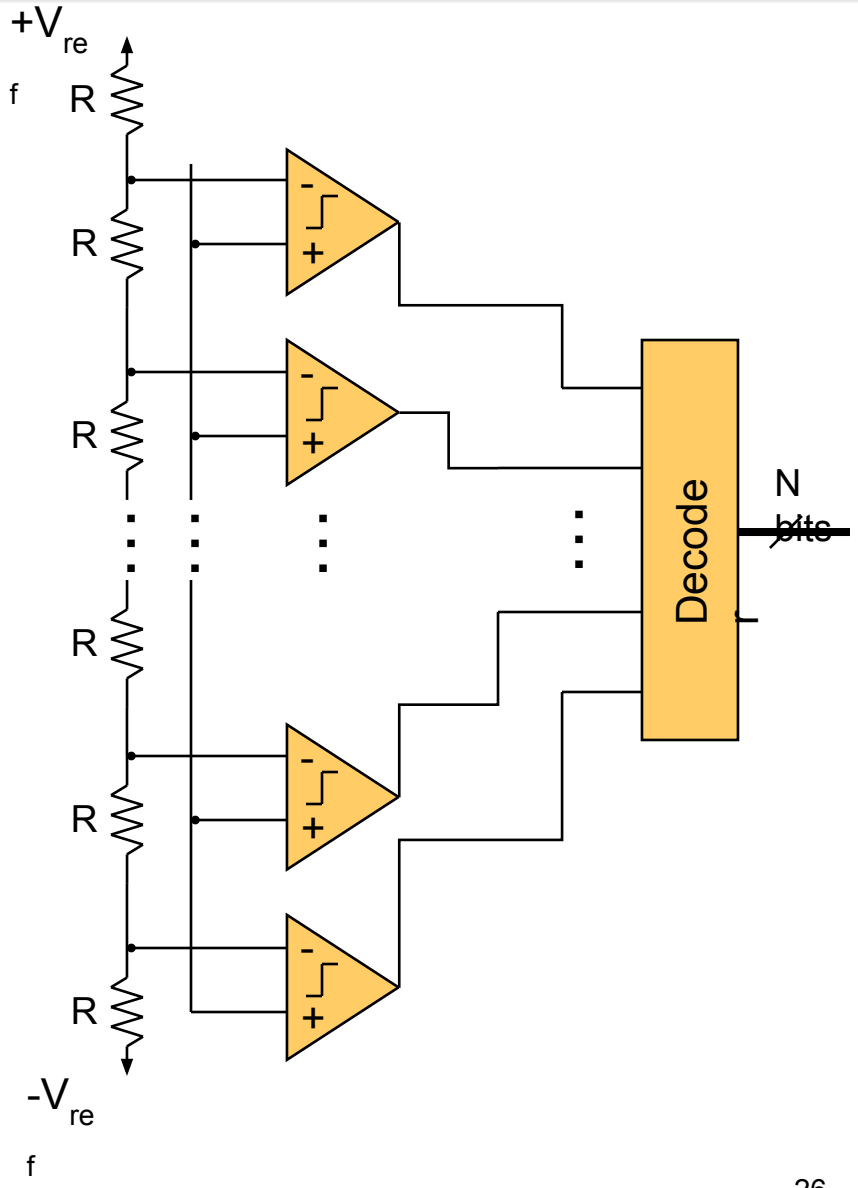
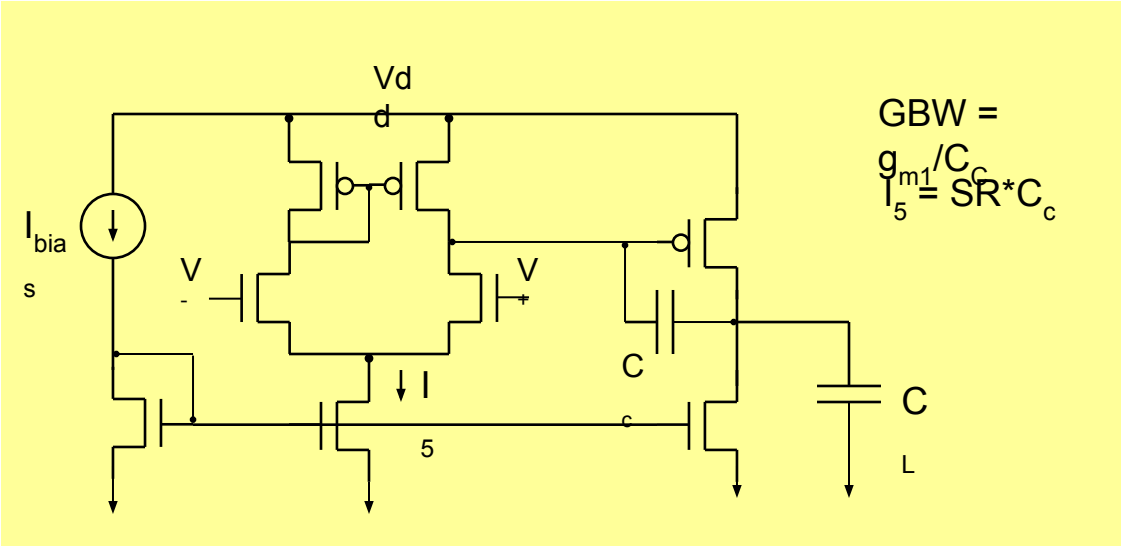
Flash ADC

- Are made by cascading high-speed comparators.
- Are the fastest way to convert an analog signal to a digital signal.
- Ideal for applications requiring very large bandwidth.
- Typically consume more power than other ADC architectures and are generally limited to 8-bits resolution.



Flash ADC non-idealities

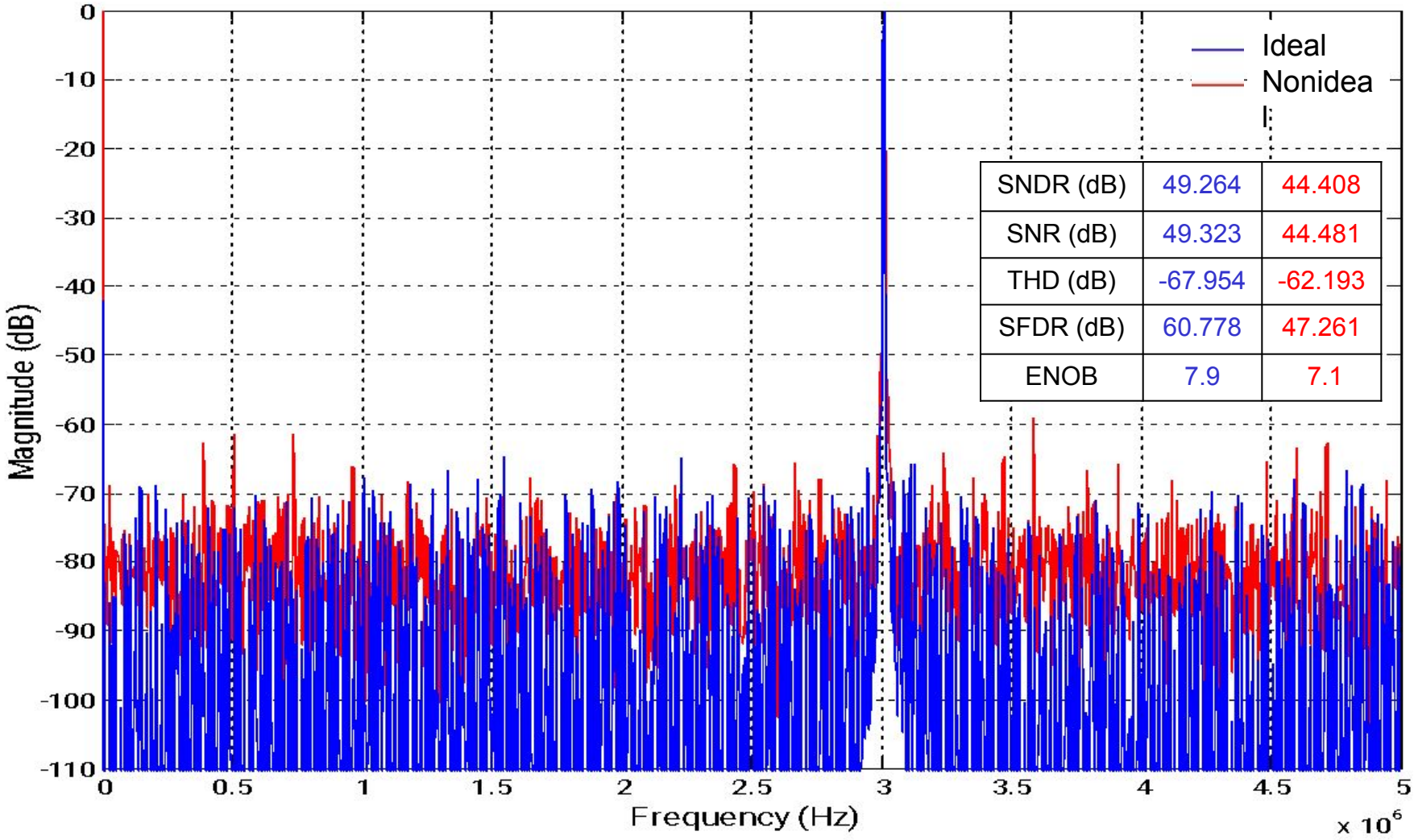
- OPAMP
  - Finite DC gain
  - Finite GBW
  - Input resistance
  - Output resistance
  - Bias current
  - Offset voltage
  - Slew Rate
- Bubbles
  - It is due the metastability of the comparators. (Future work will try model this effect)



Cadence provides a well accepted behavioral model of an non-ideal OPAMP/OTA for the most used AHDLs (Verilog-A, Verilog-AMS and VHDL-AMS)!

Flash ADC simulation results

PSD plot for 8-bit Flash ADC with 0 dB input signal f_{in} of 3.01MHz, Samples = 4096, BW = 5MHz



SNDR (dB)	49.264	44.408
SNR (dB)	49.323	44.481
THD (dB)	-67.954	-62.193
SFDR (dB)	60.778	47.261
ENOB	7.9	7.1

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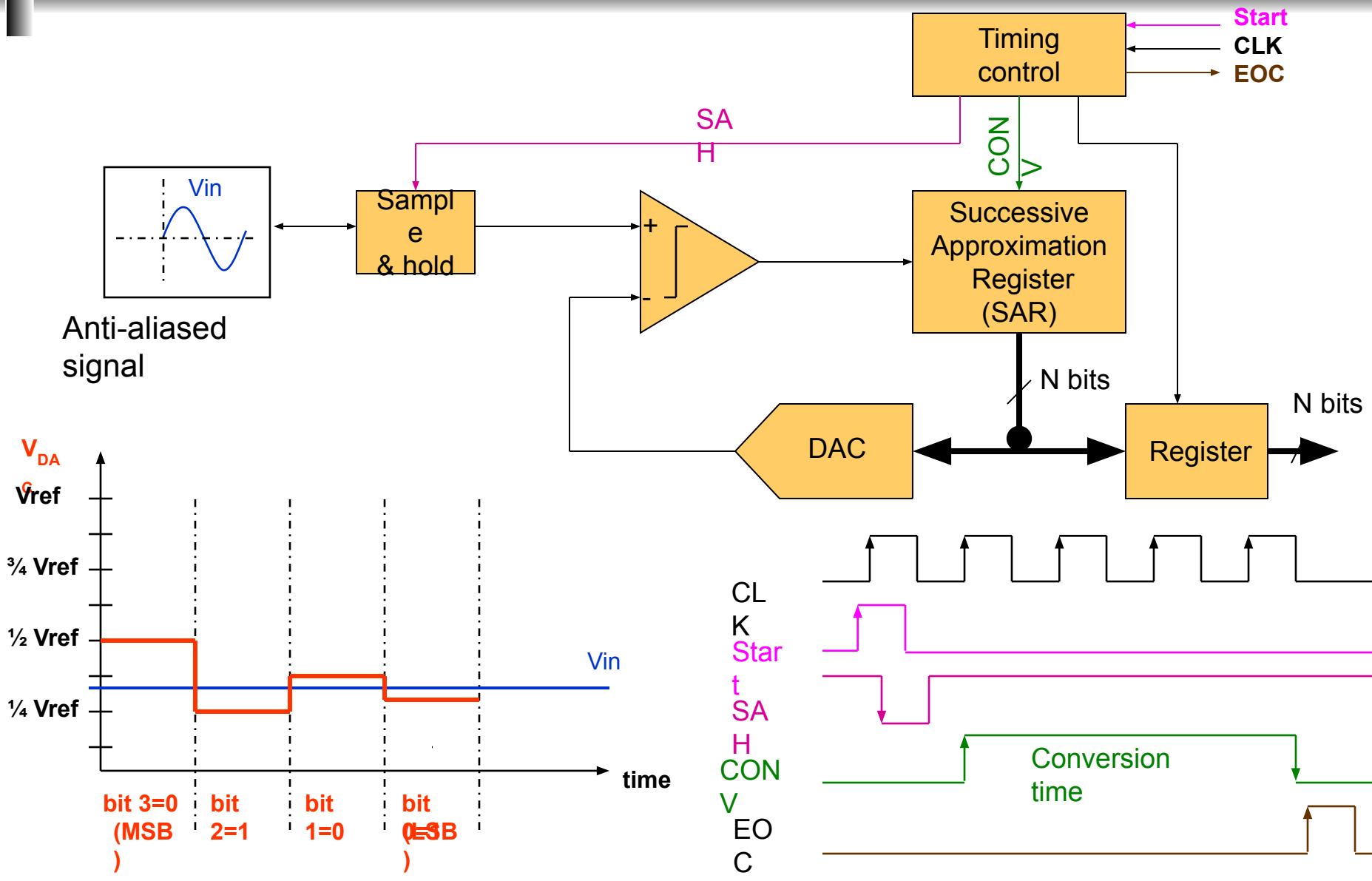
SAR ADC

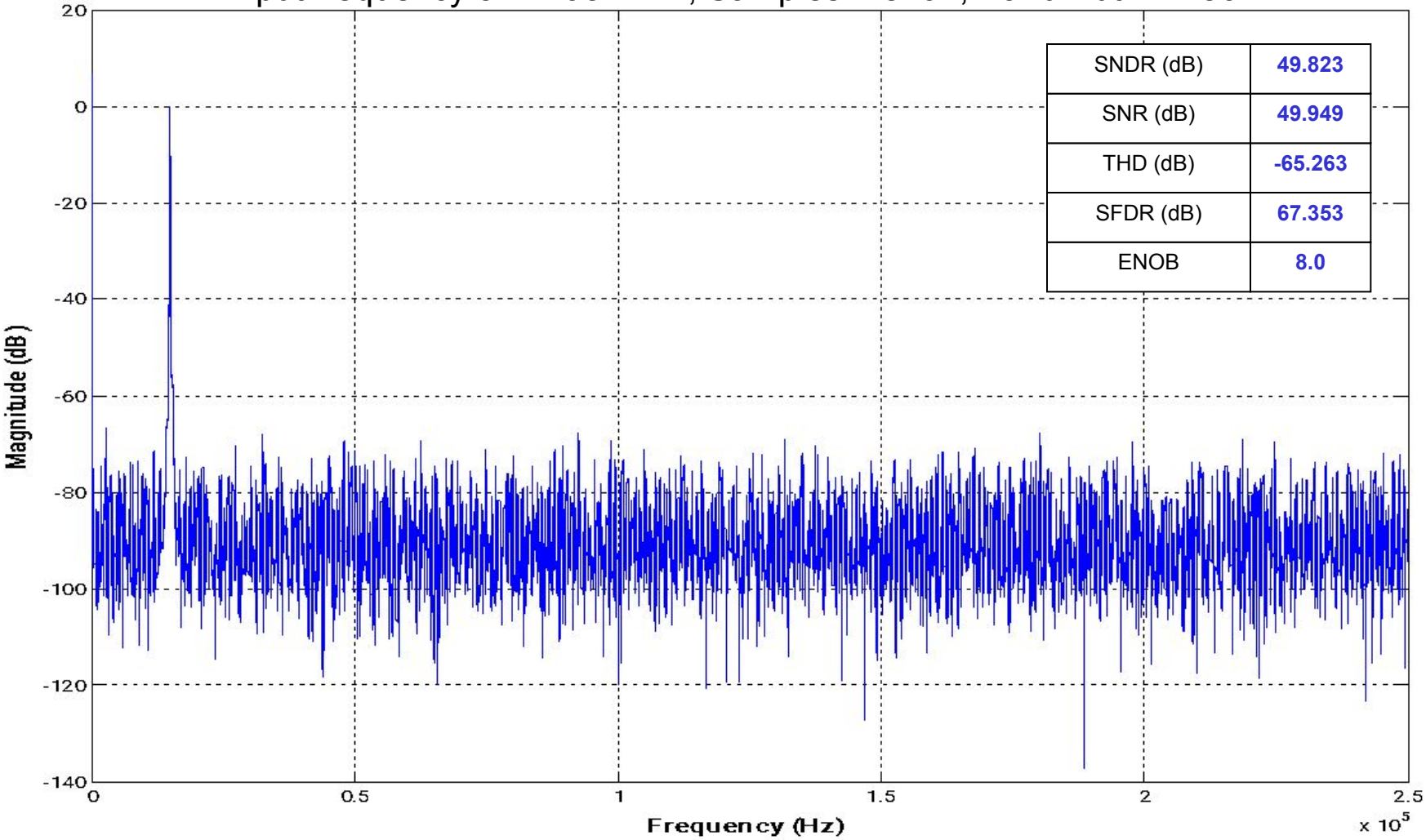
- Successive-approximation-register (SAR) ADCs) used for medium-to-high-resolution (8 to 16 bits) applications with sample rates under 5 Msps.
- Used in portable/battery-powered instruments, pen digitizers, industrial controls, and data/signal acquisition.
- Provide low power consumption.
- An N-bit SAR ADC will require N comparison periods and will not be ready for the next conversion until the current one is complete.

SAR ADC


Timing control
Start
CLK
EOC
SAH
CONV
Vin
Sample & hold
Successive Approximation Register (SAR)
N bits
DAC
Register
N bits
Anti-aliased signal
VDAC
Vref
¾ Vref
½ Vref
¼ Vref
Vin
time
bit 3=0 (MSB)
bit 2=1
bit 1=0
bit 0=LSB
CLK
Start
SAH
CONV
EOC
Conversion time

SAR 8-bit ADC simulation results

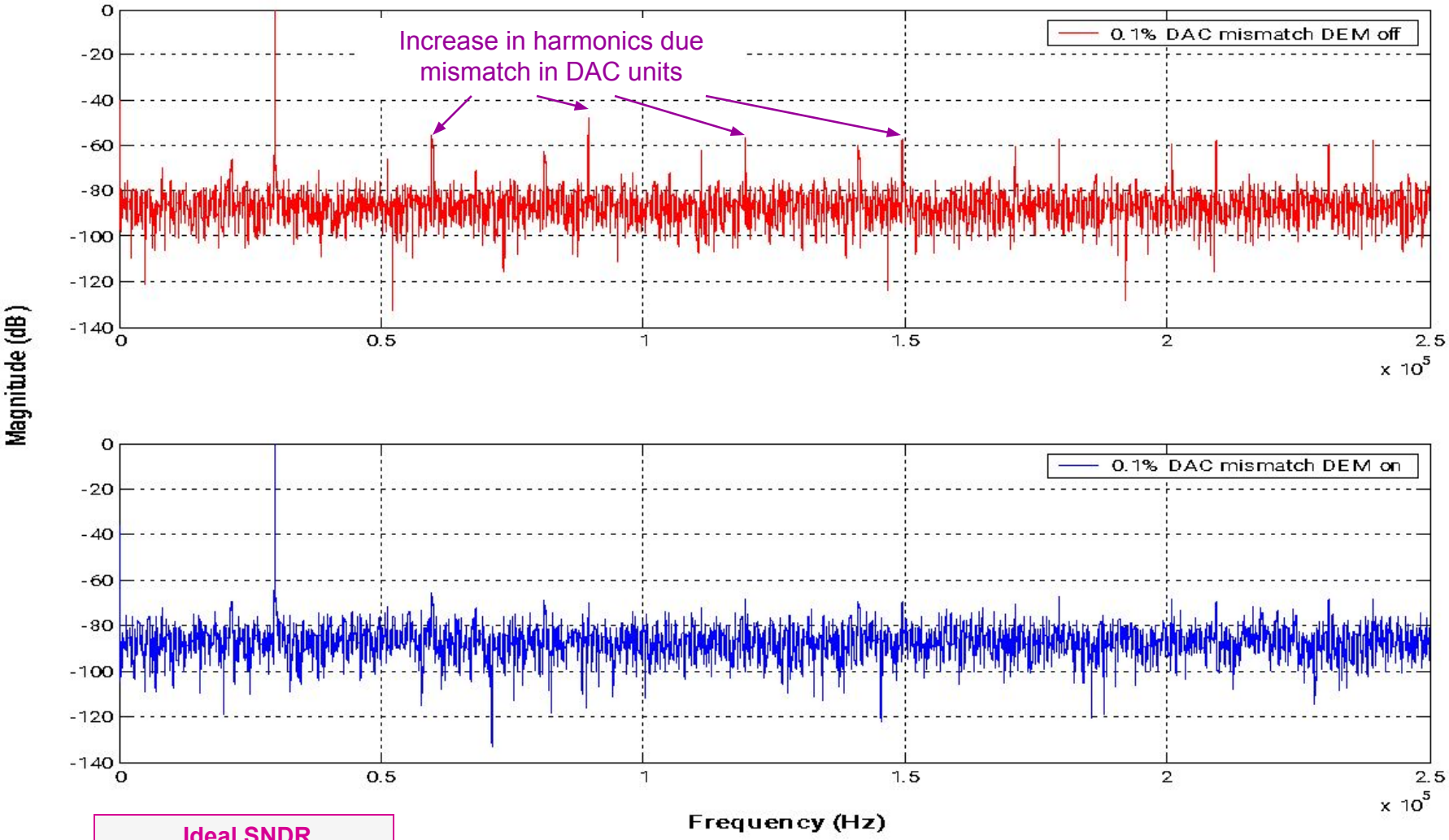
Ideal PSD plot for 8-bit SAR ADC with 0 dB input signal
Input frequency of 14.954KHz, Samples = 8192, Bandwidth = 250KHz



SNDR (dB)	49.823
SNR (dB)	49.949
THD (dB)	-65.263
SFDR (dB)	67.353
ENOB	8.0

SAR 8-bit ADC simulation results

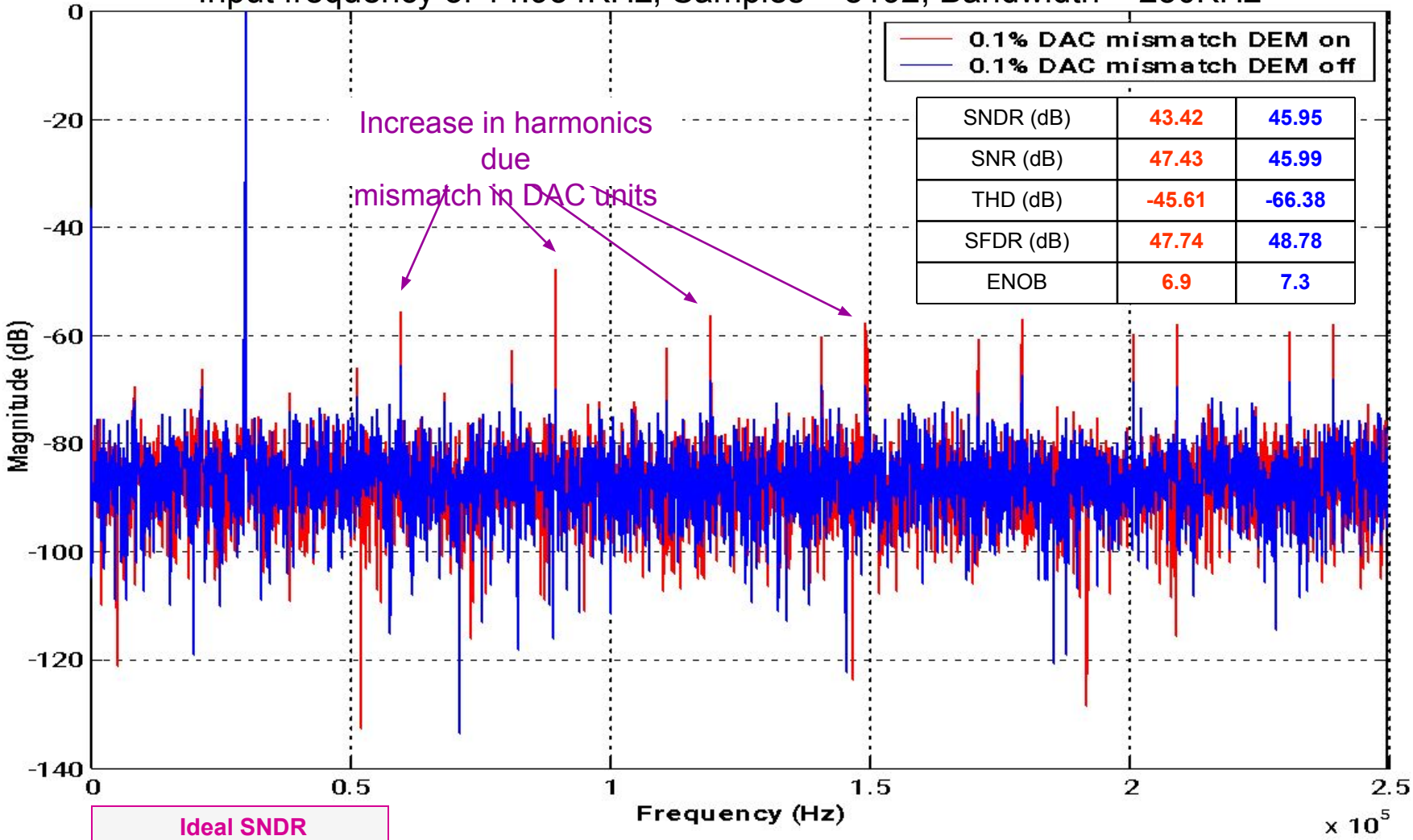
PSD plot for 8-bit SAR ADC with 0 dB input signal
Input frequency of 14.954KHz, Samples = 8192, Bandwidth = 250KHz



Ideal SNDR
6.02N+1.76=49.92 dB

SAR 8-bit ADC simulation results

PSD plot for 8-bit SAR ADC with 0 dB input signal
Input frequency of 14.954KHz, Samples = 8192, Bandwidth = 250KHz



SNDR (dB)	43.42	45.95
SNR (dB)	47.43	45.99
THD (dB)	-45.61	-66.38
SFDR (dB)	47.74	48.78
ENOB	6.9	7.3

Ideal SNDR
6.02N+1.76=49.92 dB

Agenda

- Generic ADC
  - Analysis and model
  - Simulation results
- Flash ADC
  - Analysis and model
  - Simulation results
- SAR ADC
  - Analysis and model
  - Simulation Results
- Pipelined ADC
  - Analysis
  - 1.5 bit Stage
    - 1.5 bit ADC

Agenda

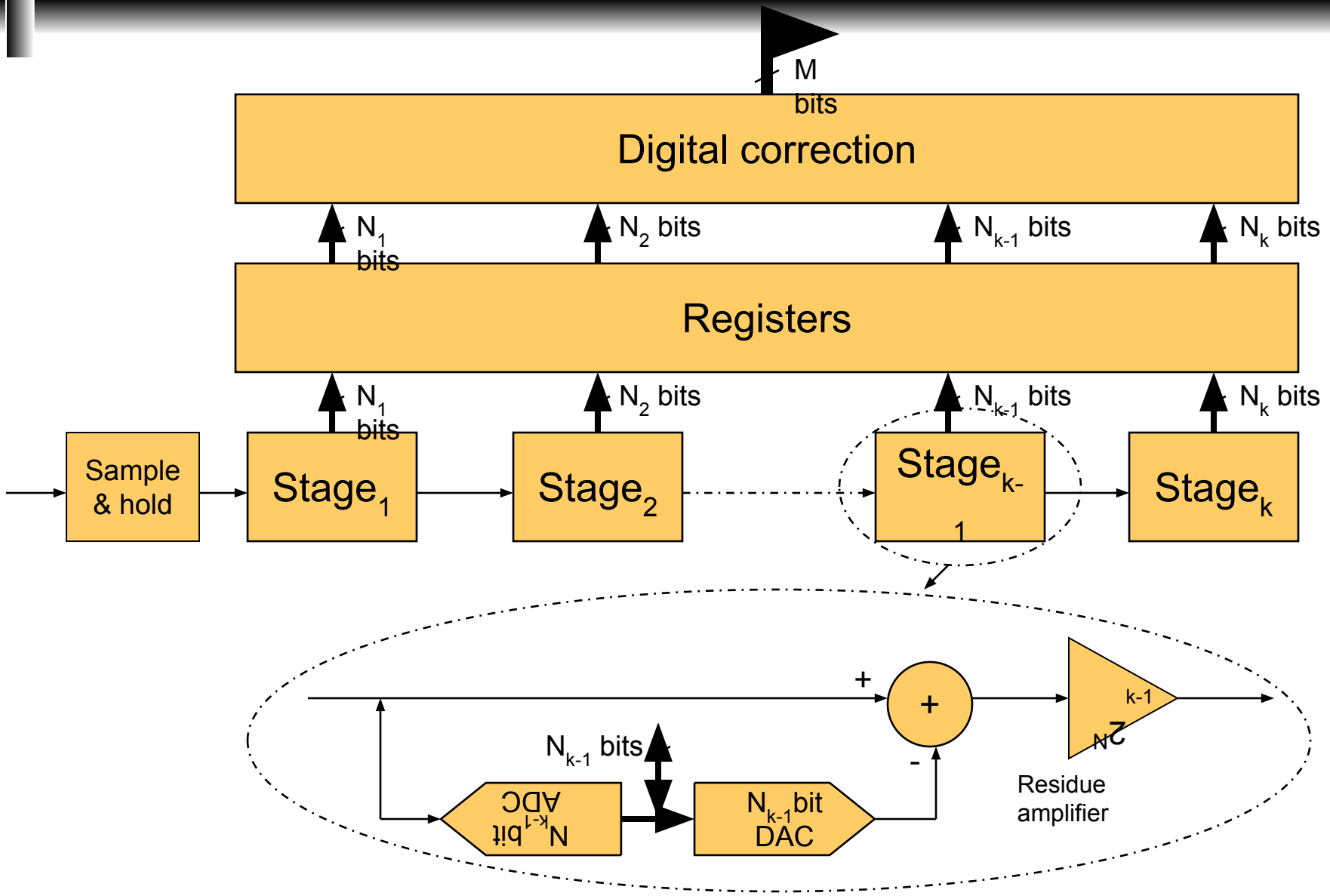
- 1.5 bit MDAC
- Digital Correction
- Simulation results

- ΣΔ ADC
  - ΣΔ Modulator
    - SC integrator analysis
    - Model
    - Simulation results
- Conclusions
- Future Work
- Acknowledgements
- References

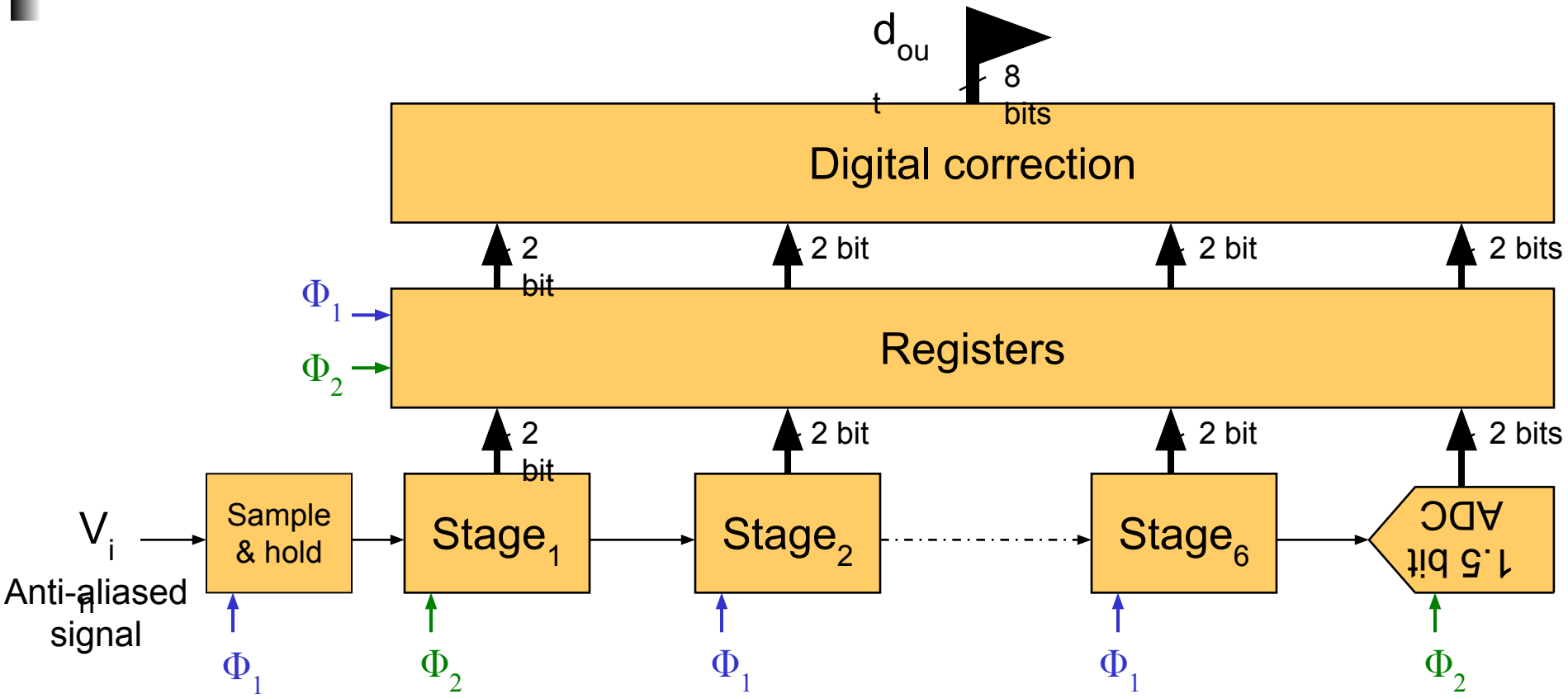
Pipelined ADC

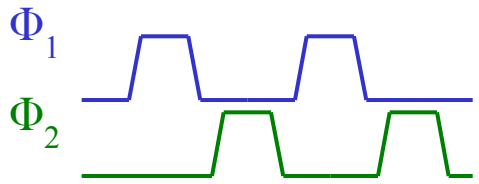
- Has become the most popular ADC architecture for sampling rates from a few MS/s up to 100MS/s, with resolutions from 8 bits at the faster sample rates up to 16 bits at the lower rates.
- Low-power capability.
- Allows the use of "digital error correction" and “digital calibration” to greatly reduce the accuracy requirement of the internal flash ADCs and DACs respectively.
- Because each sample has to propagate through the entire pipeline before all its associated bits are available there is some data latency.

Pipeline ADC

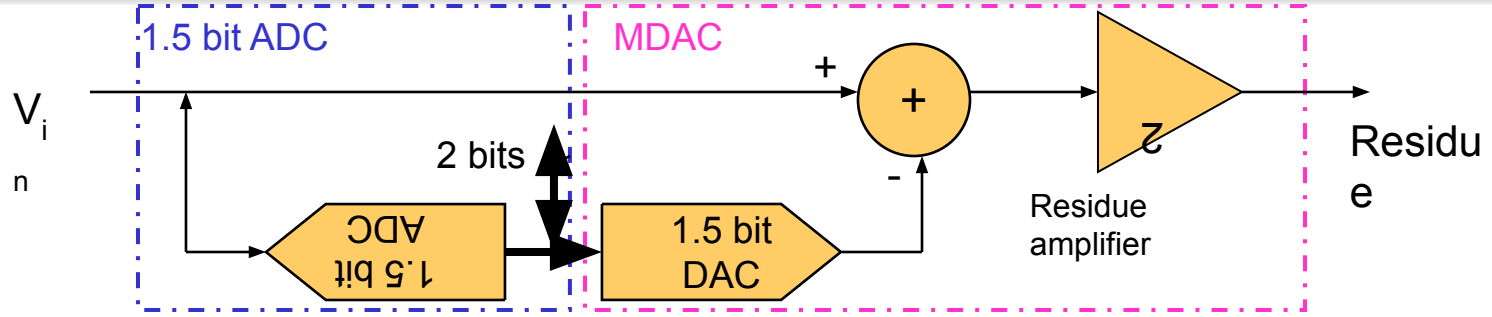


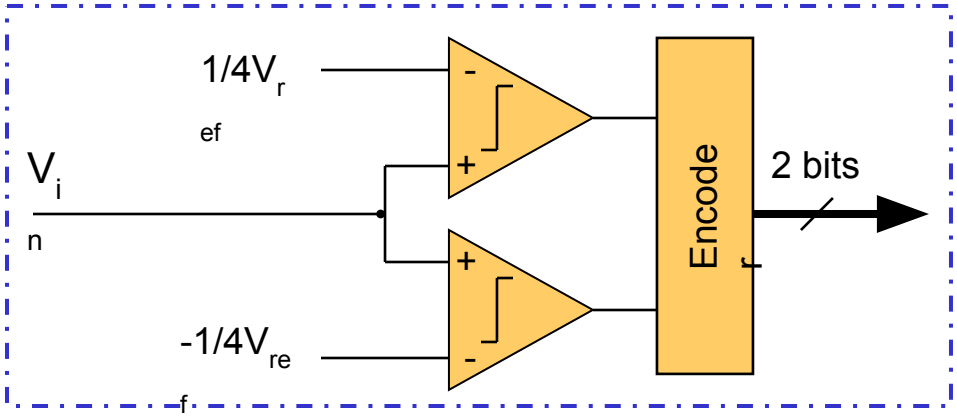
Pipeline ADC 8-bit (1.5-bit per stage)

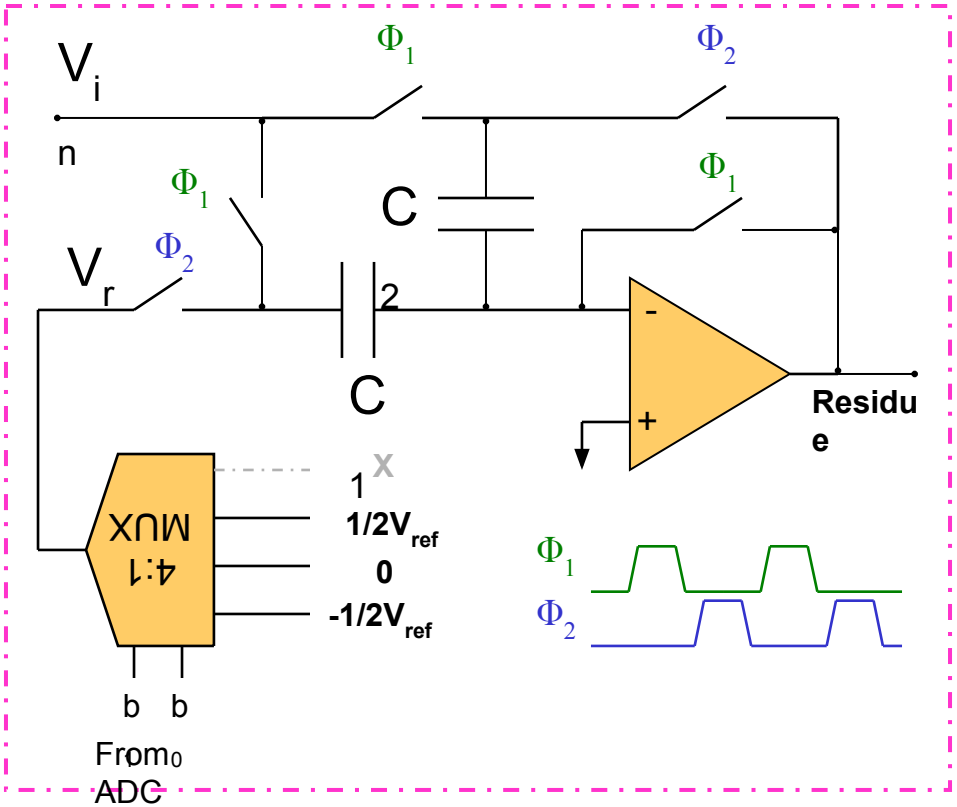




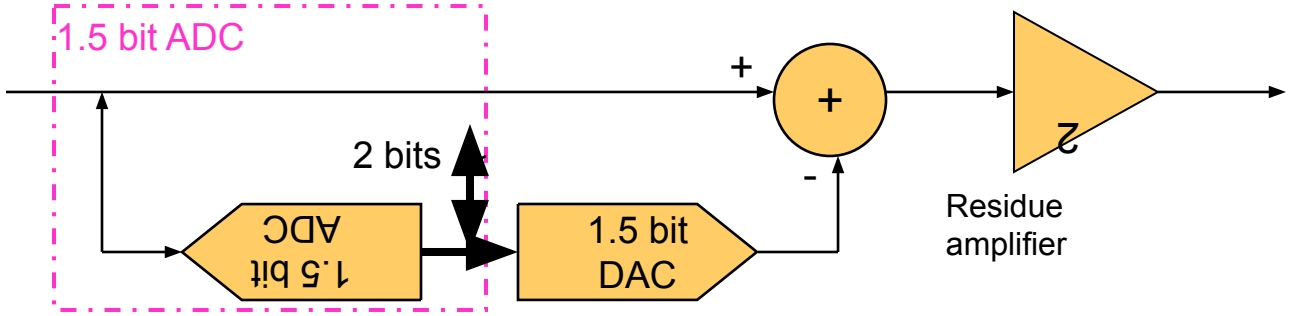
1.5-bit Pipelined Stage

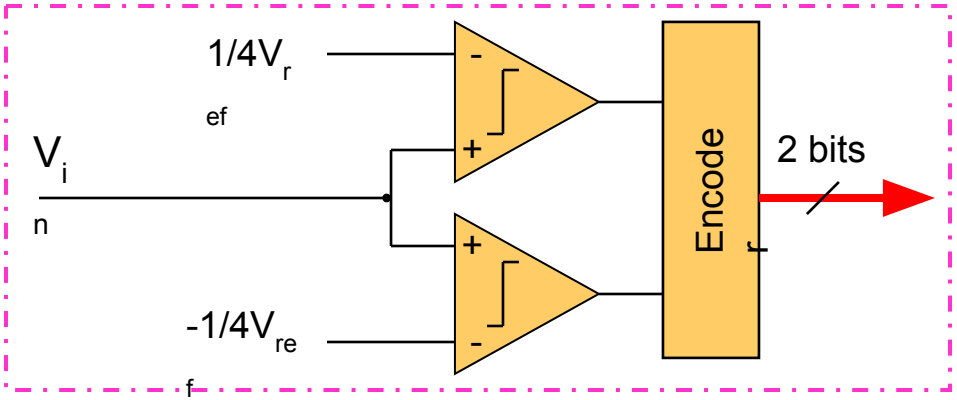


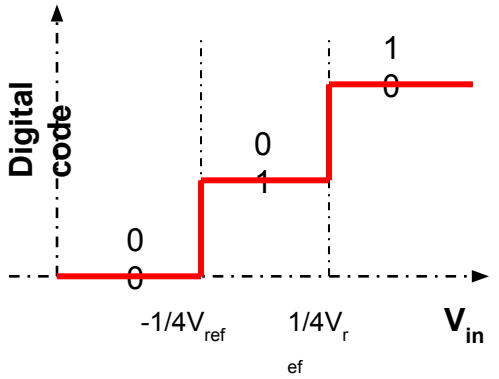




1.5-bit ADC

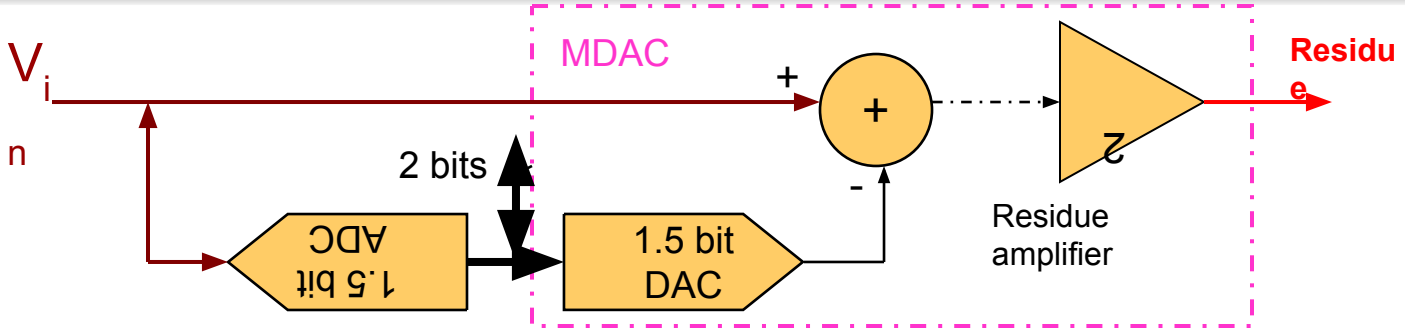


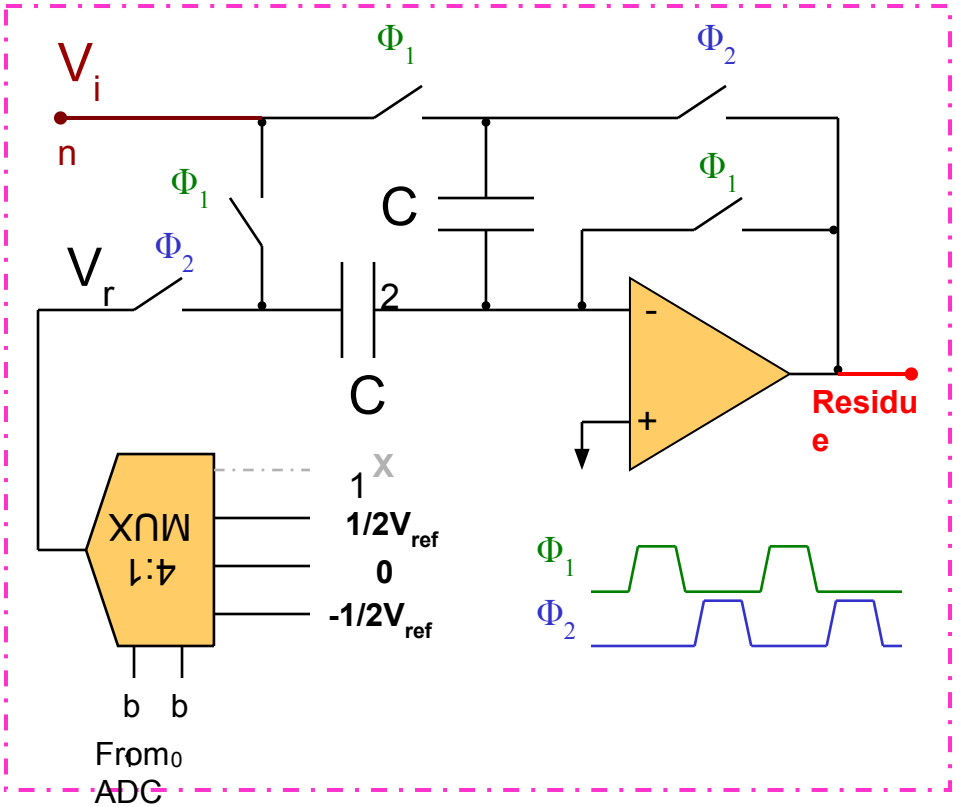




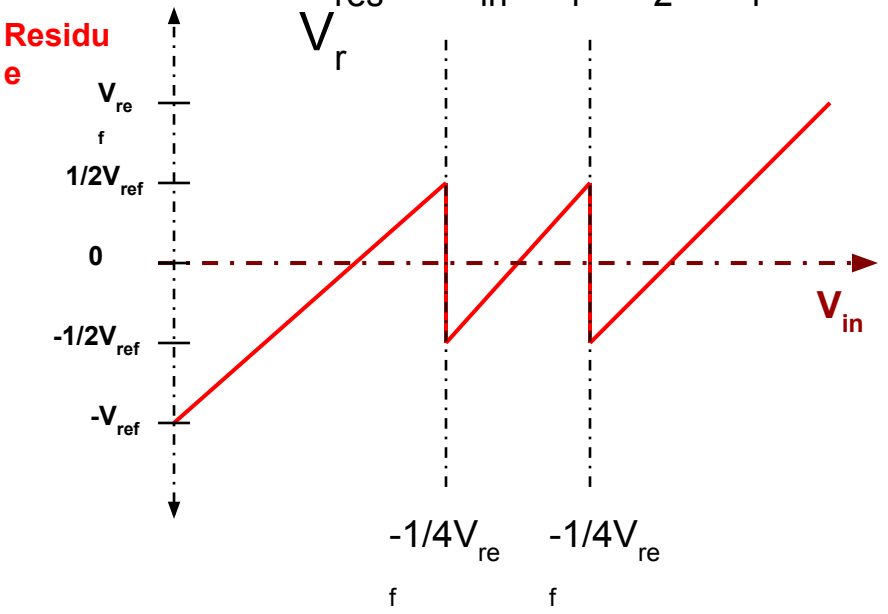
Modeled as a Generic ADC with the specified reference levels

1.5-bit MDAC





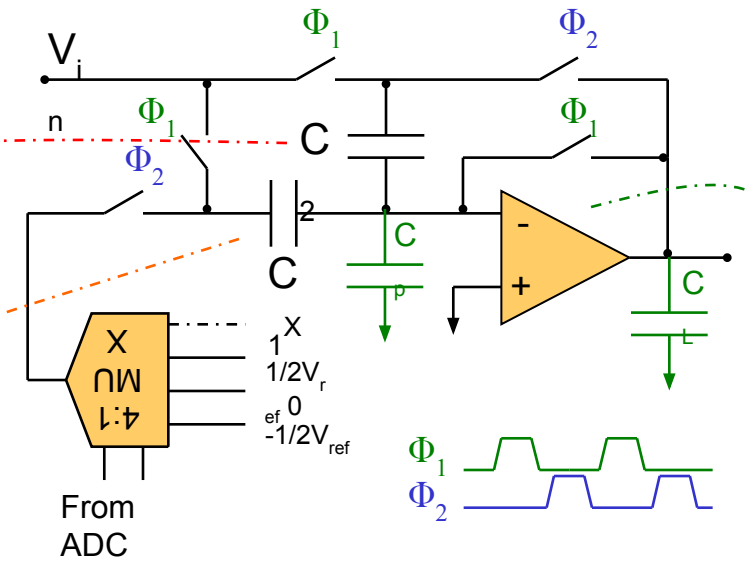
$$V_{res} = V_{in}(C_1+C_2)/C_1 + V_r$$

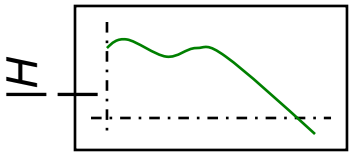


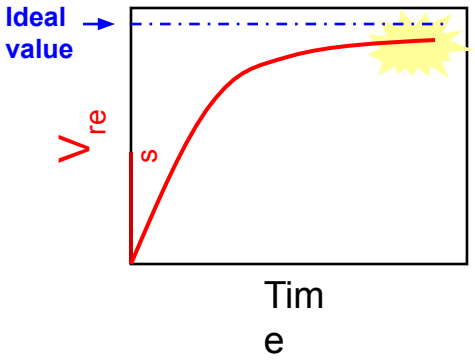
1.5-bit MDAC nonidealities

Capacitors mismatch

Thermal noise $V_{th} \approx kT/C_1$
(Opamp noise neglected)

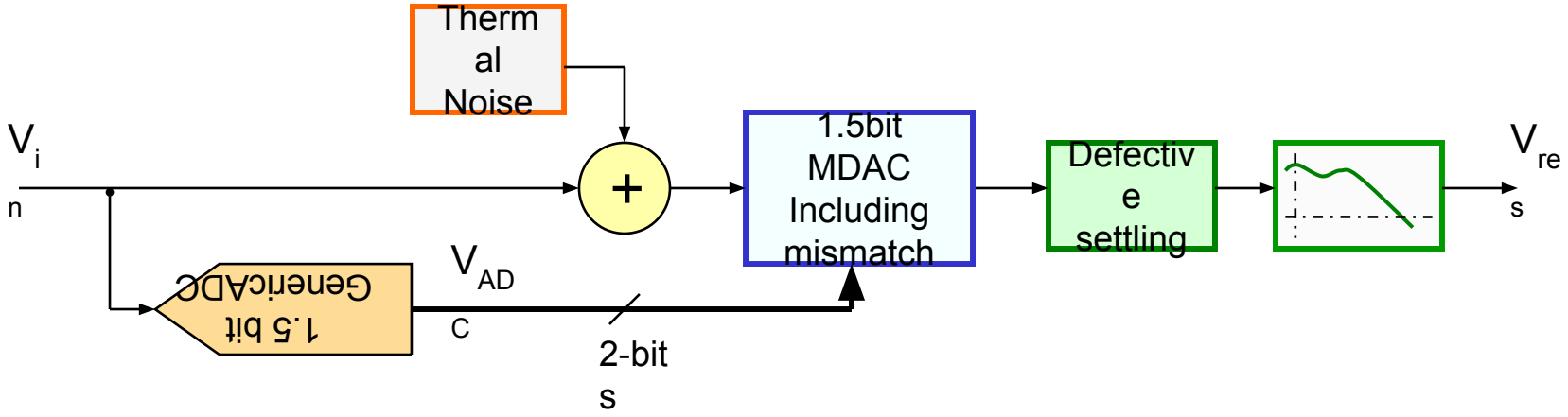


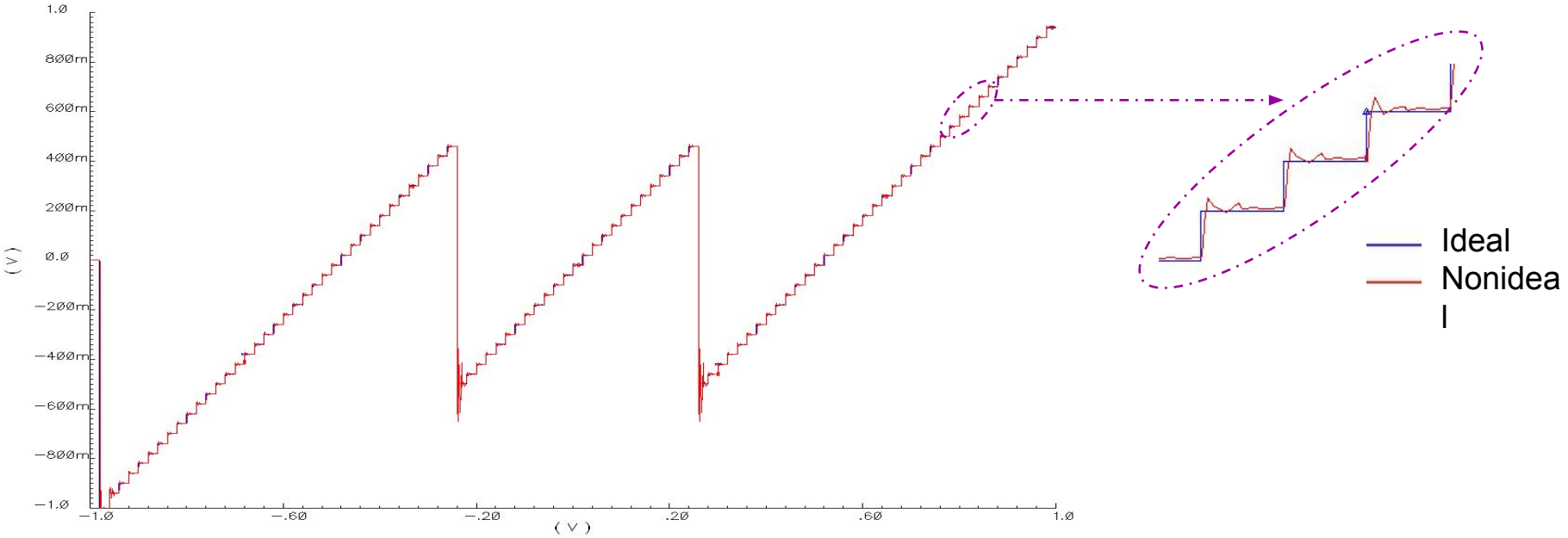




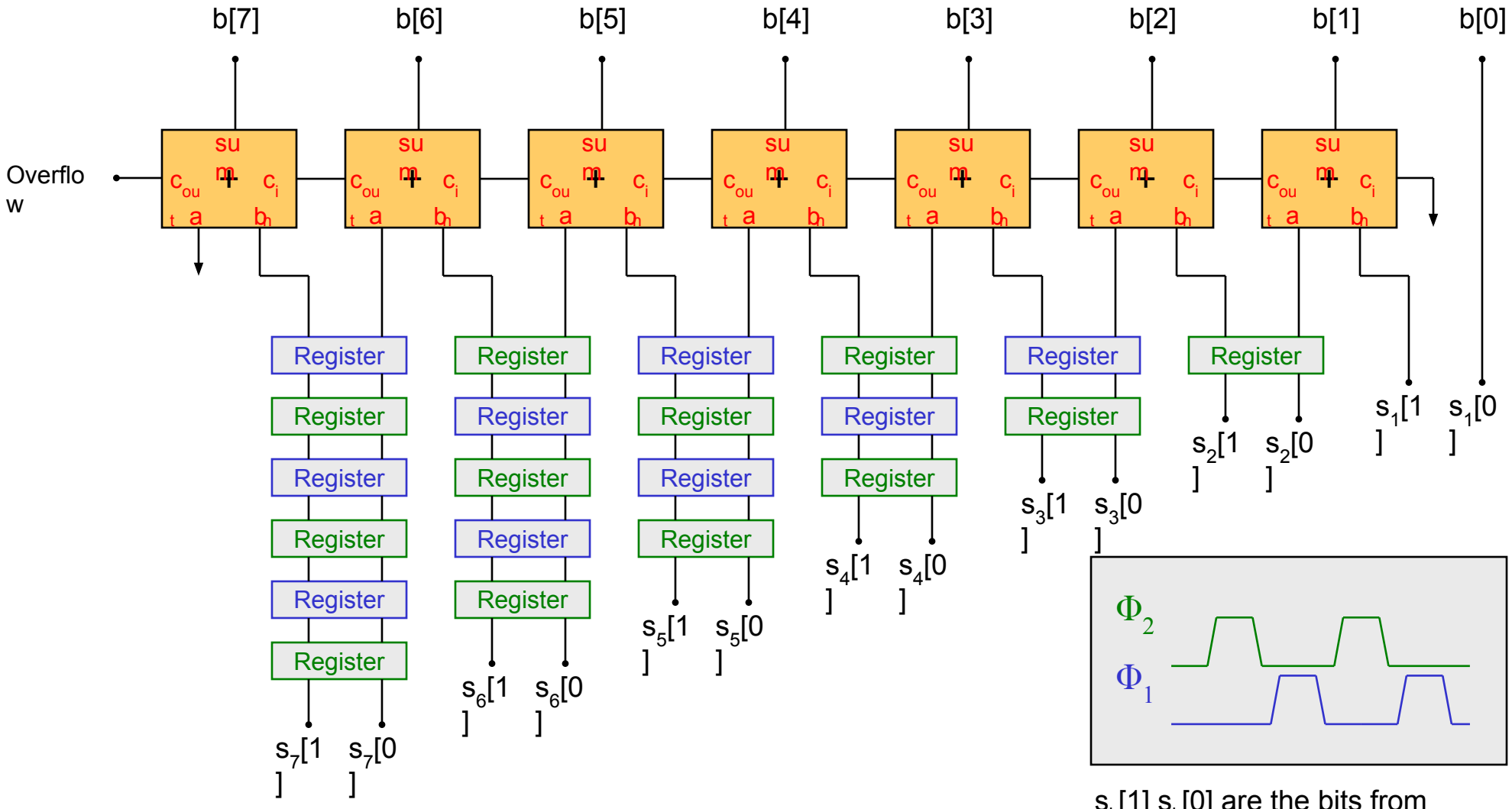
- Finite DC gain A_0 → $\varepsilon_g = C_1 + (C_1 + C_2 + C_p)/A_0$
- Finite GBW, C_p and C_L
- Defective settling
  - Linear
  - Slewing
  - Partial Slewing

1.5-bit Stage model



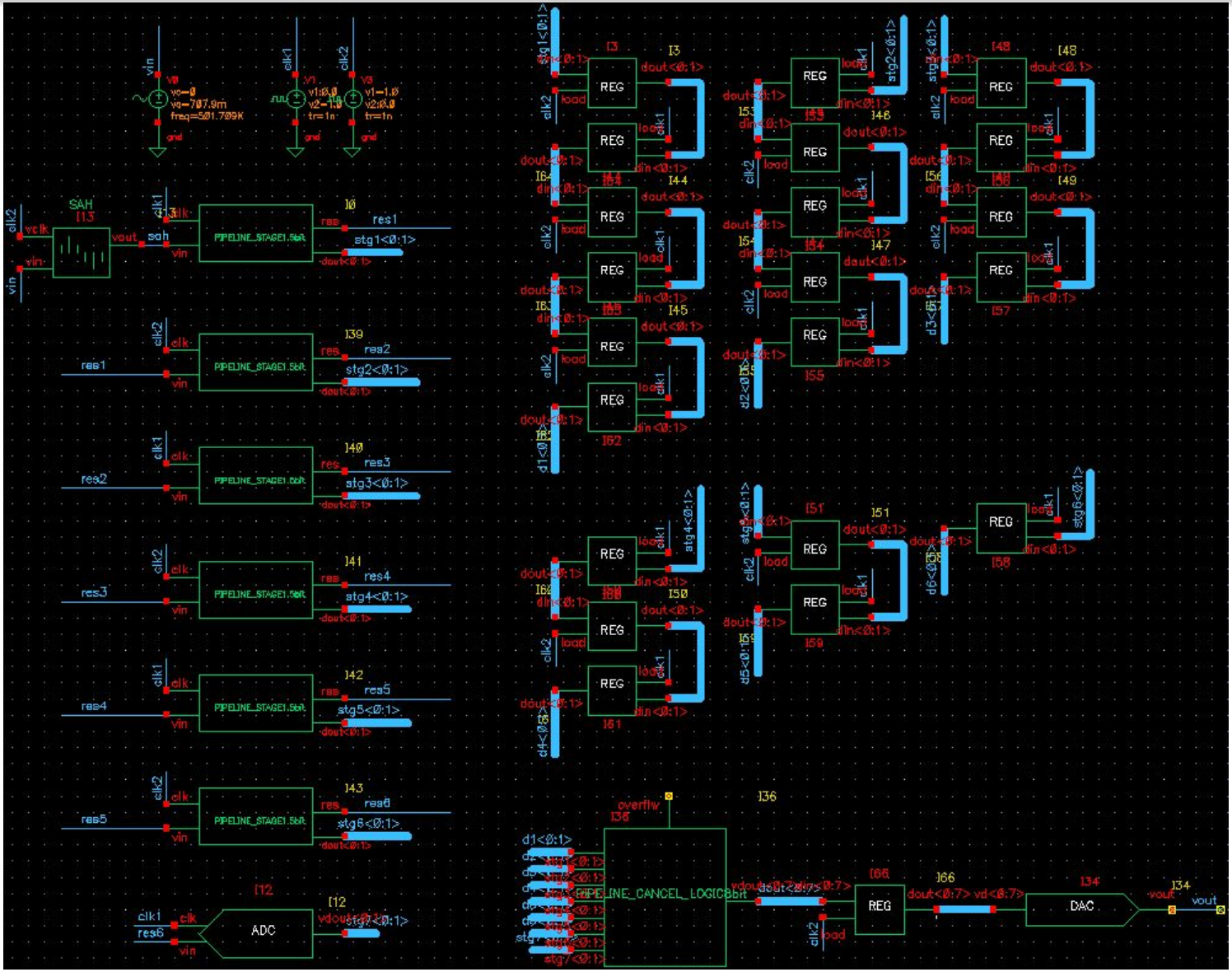


Digital Correction



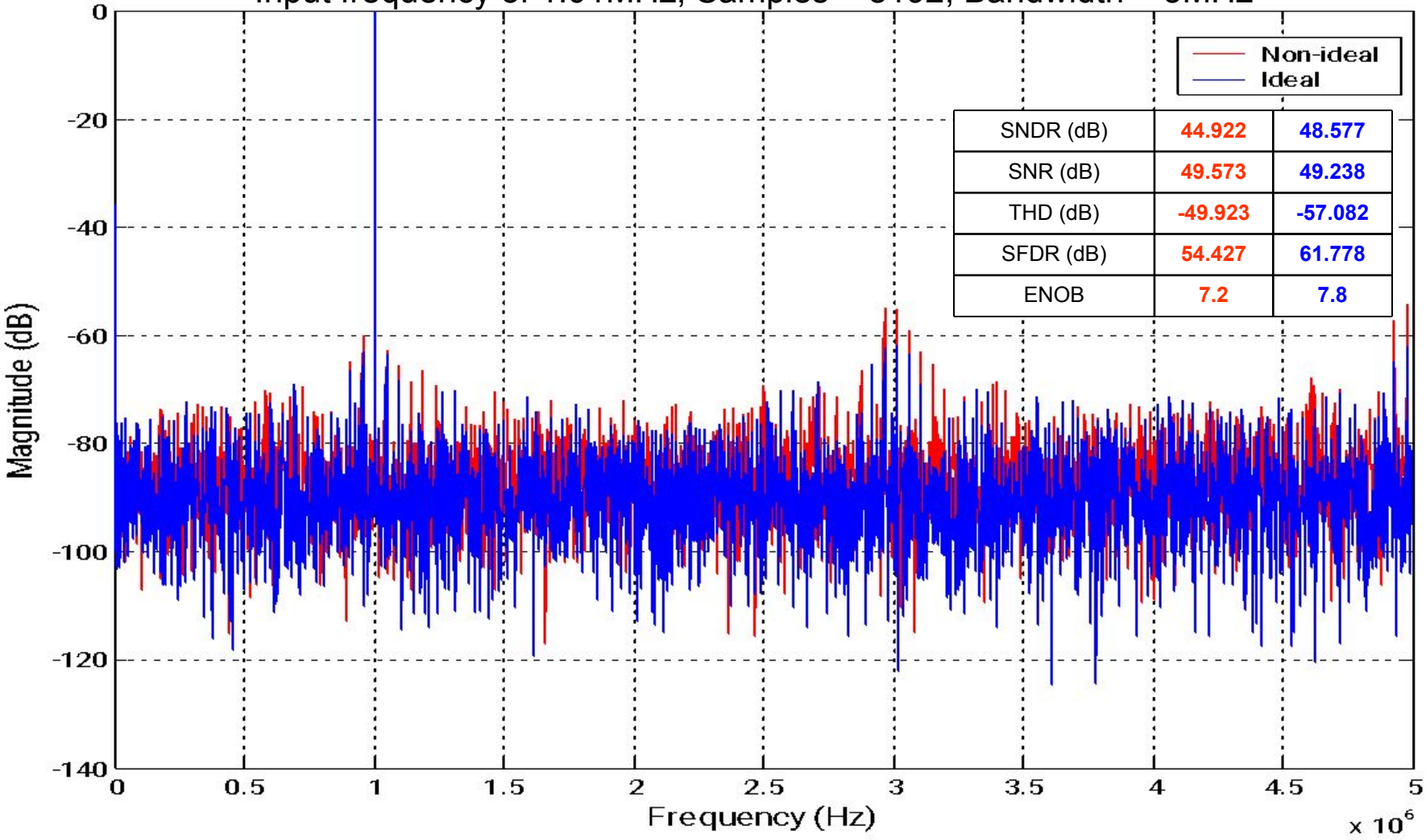
$s_k[1]$ $s_k[0]$ are the bits from stage k

Pipelined 8-bit ADC model (Cadence)



Pipelined 8-bit ADC simulation results

PSD plot for 8-bit Pipelined ADC with 0 dB input signal
Input frequency of 1.01MHz, Samples = 8192, Bandwidth = 5MHz



SNDR (dB)	44.922	48.577
SNR (dB)	49.573	49.238
THD (dB)	-49.923	-57.082
SFDR (dB)	54.427	61.778
ENOB	7.2	7.8

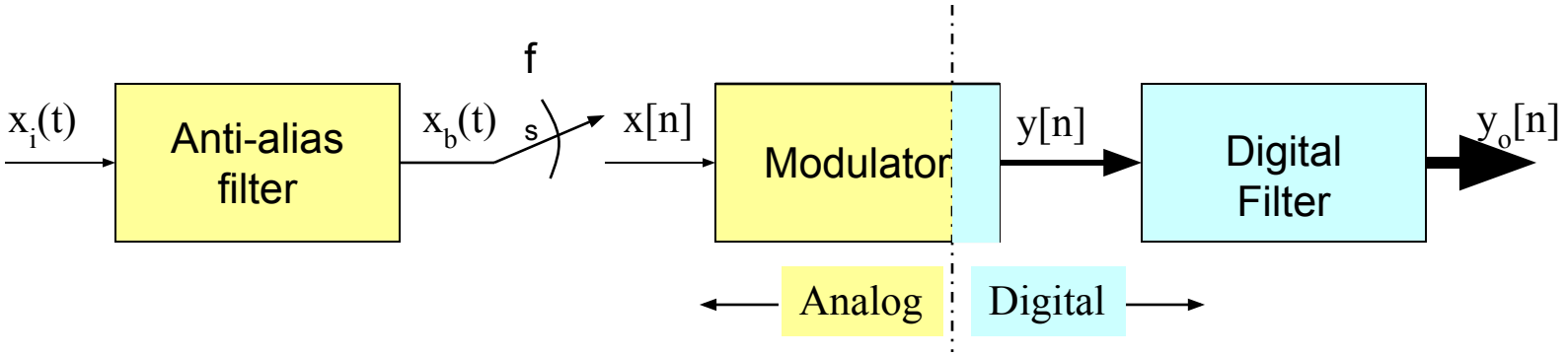
Agenda

- 1.5 bit MDAC
- Digital Correction
- Simulation results

- ΣΔ ADC
  - ΣΔ Modulator
    - SC integrator analysis
    - Model
    - Simulation results
- Conclusions
- Future Work
- Acknowledgements
- References

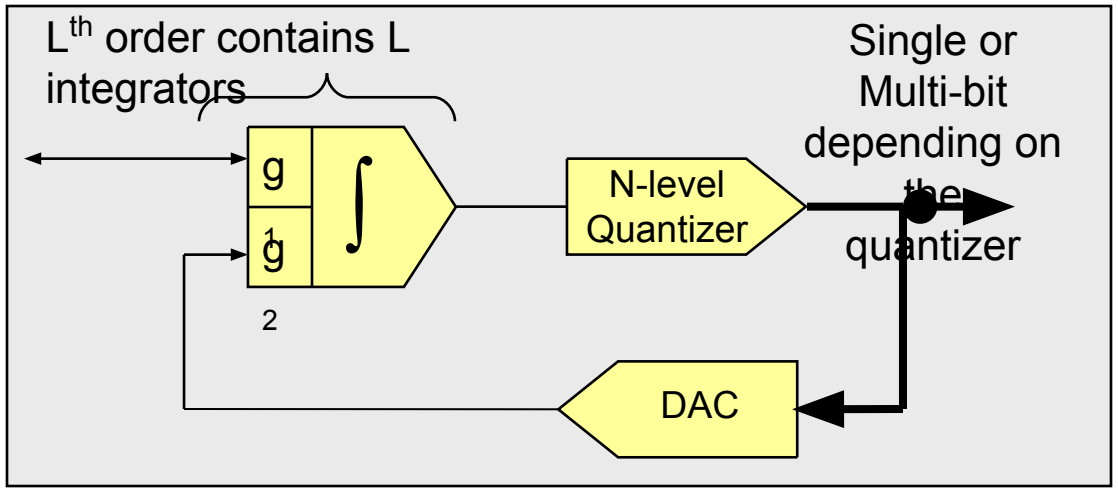
ΣΔ ADC

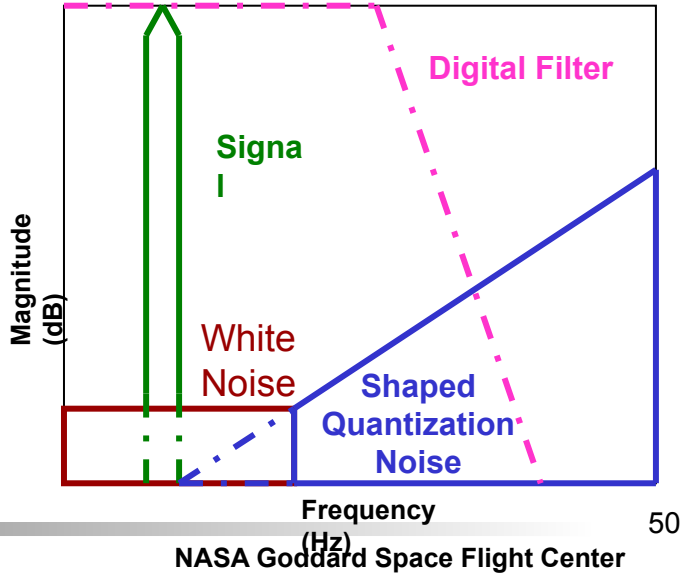
- Makes use of oversampling and ΣΔ modulation techniques to achieve high resolution.
- Used for low bandwidth and high-resolution applications but recently there is great interest for medium to high bandwidth applications.
- Due oversampling the requirements of the anti-aliasing filter are reduced.



ΣΔ Modulator (ΣΔM)

- ΣΔM is the major analog component of the ADC.
- Due to its mixed-signal nature, non-idealities largely affect the performance of the ADC, i.e. the integrator, DAC mismatch.
- Quatization noise is shaped outside the band of interest.
- Several architectures exists depending on the number of integrators and the quantizer levels.

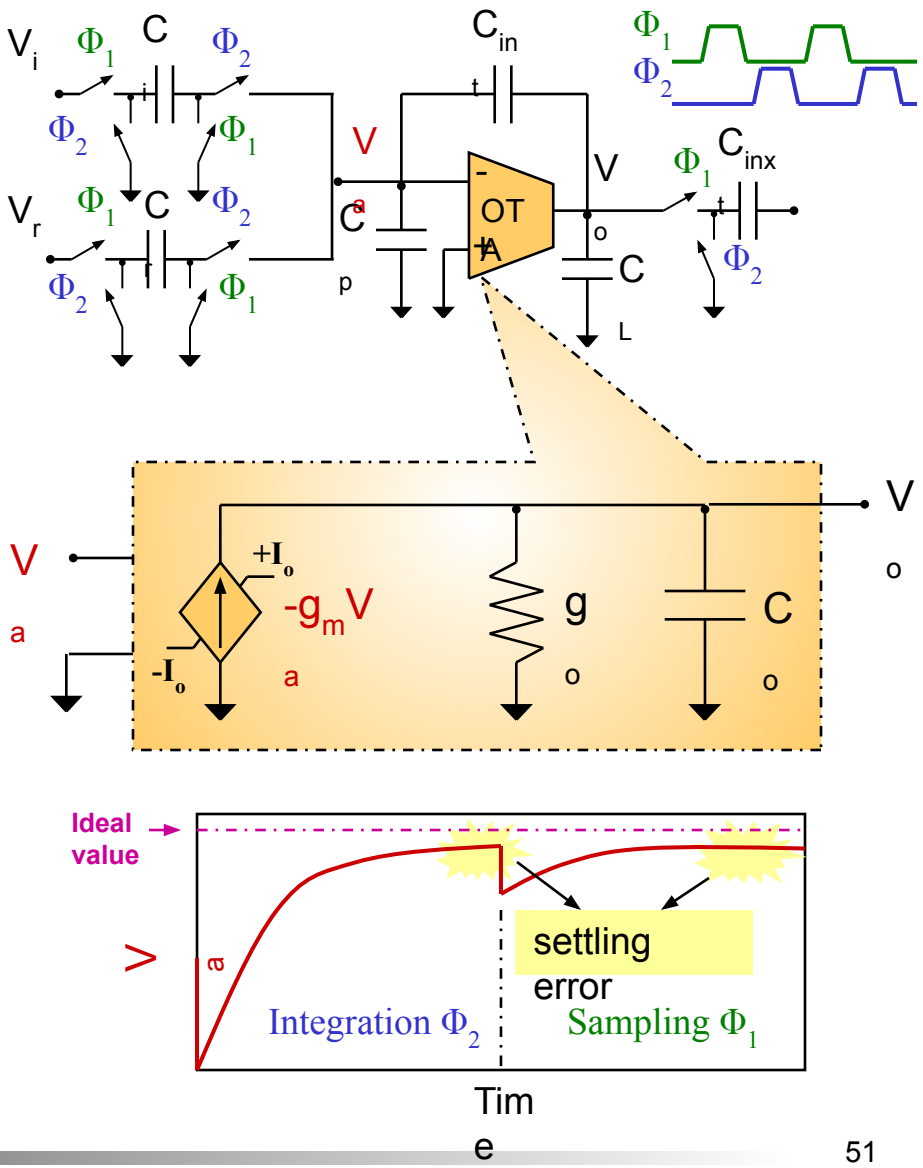




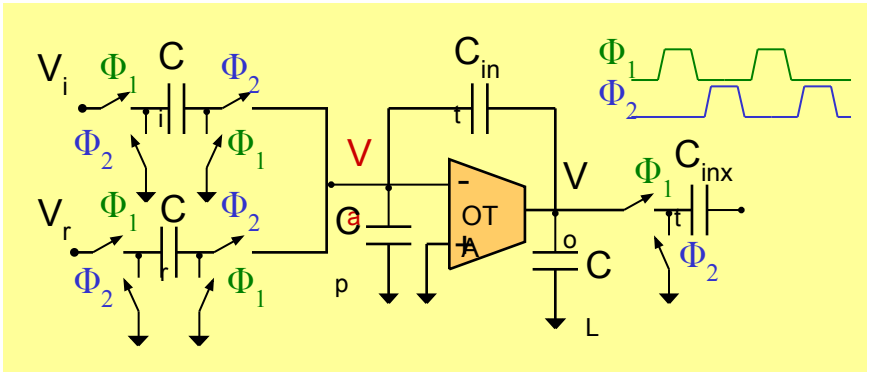
SC integrator transient model

- Single pole OTA model
- Defective settling due to the OTA finite DC gain, GBW and SR limitations.
- Possible settling scenarios:
  - Linear
    - $|V_{ai}| \le I_o/g_m$
  - Slewing
    - $|V_{ai}| > I_o/g_m$ and $t < t_o$
  - Partial Slewing
    - $|V_{ai}| > I_o/g_m$ and $t \ge t_o$

Parameter	Description
C_i, C_r	Sampling capacitors
C_{int}	Integrating capacitor
C_p,C_o	Input and output parasitic capacitances
C_{inxt}	Next stage input capacitance
g_m	OTA transconductance
g_o	OTA output conductance
I_o	OTA max output current
t_o	slewing time
V_{ai}	Initial voltage at V_a



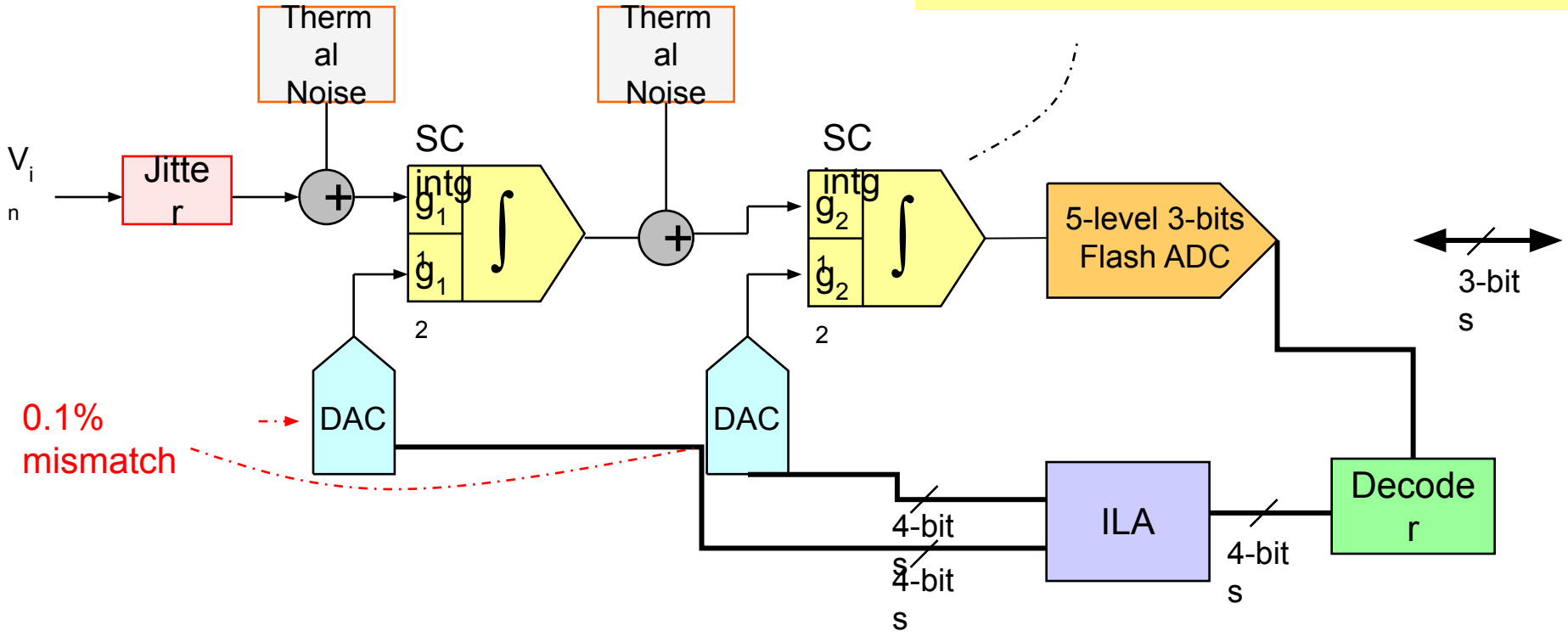
Second-Order ΣΔM Model



$g_{X1} = C_i/C_{int}$

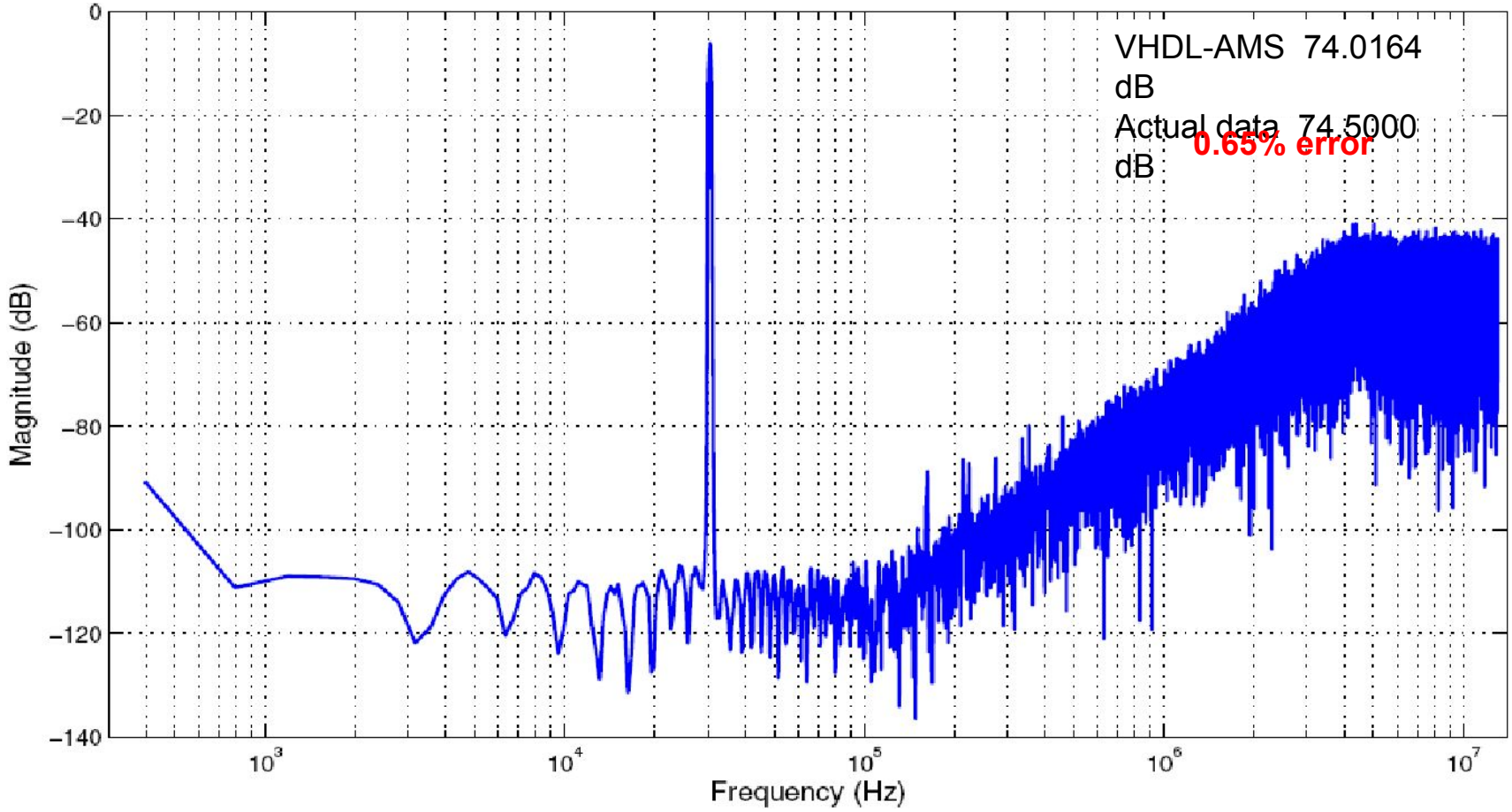
$g_{X2} = C_r/C_{int}$

OTA + switches for both phases Φ_1 and Φ_2



ΣΔM Simulation Results GSM mode

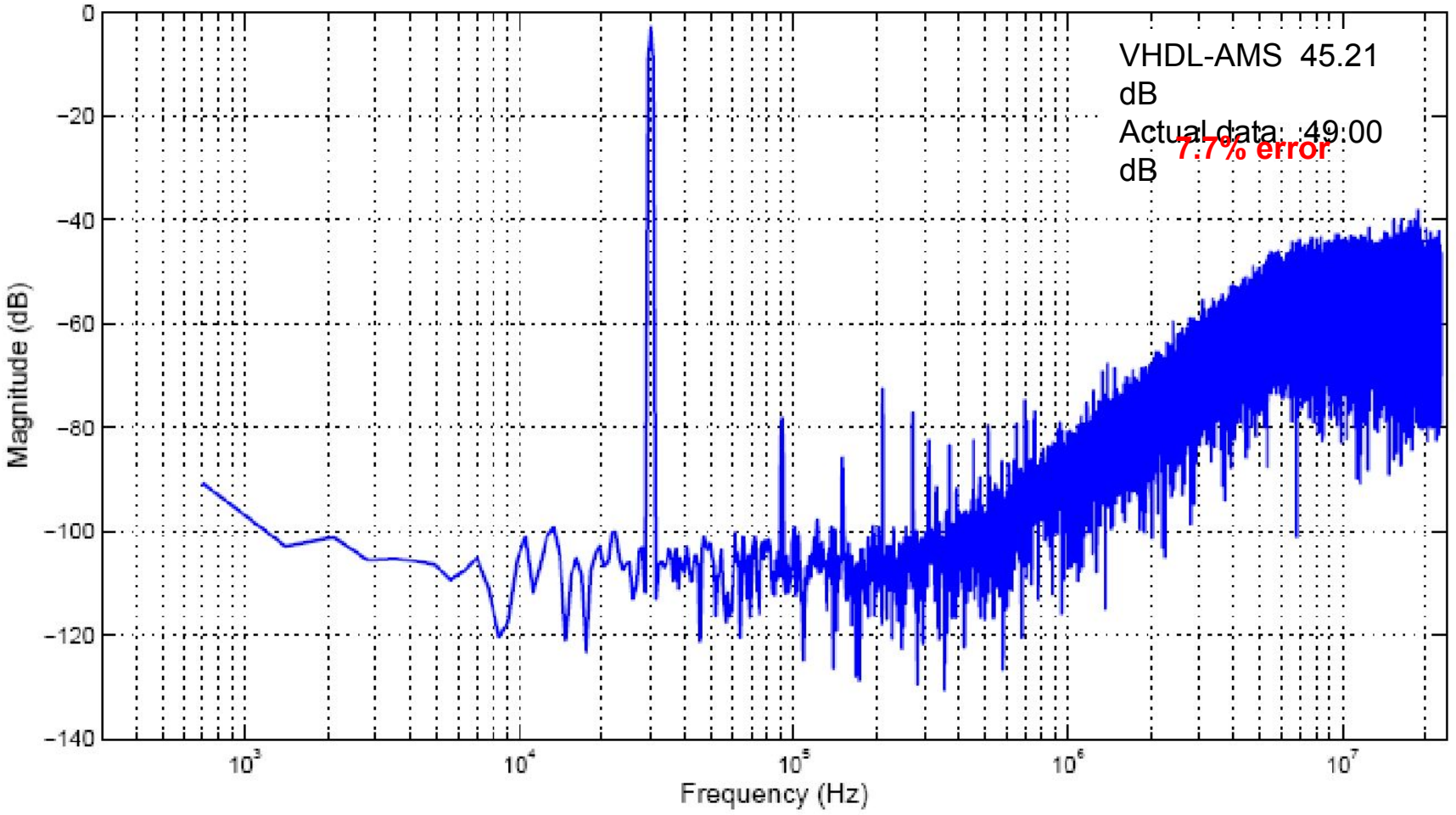
*Second order sigma-delta modulator with -6 dB input signal
Input frequency of 30kHz, OSR = 65, N = 65536, BW = 200kHz (GSM mode)



*This work has been accepted as a lecture presentation at the IEEE MWCAS 2005 conference, August 7-10 Cincinnati, Ohio.

ΣΔM Simulation Results WCDMA mode

Second order sigma-delta modulator with -6 dB input signal
Input frequency of 300kHz, OSR = 12, N = 65536, BW = 200kHz (GSM mode)



Conclusions

- Behavioral modeling is a viable solution for the complex modeling and simulation of mixed-signal circuits.
- Verilog-A AHDL is suitable for modeling and simulation of mixed-signal circuits providing modularity and flexibility.
- Accurate behavioral models are achieved via validation.
- Behavioral modeling can be used as part of a Top-Down design approach but an iterative procedure is needed in order to refine the models.
- Effective circuits modeling techniques involves deep analysis including noise sources.

Future Work

- Include more ADCs architectures such as integrating, sub-range and inter-leaved.
- Add specific DAC architectures such as resistor-string, capacitive, ΣΔ, multiplying, algorithmic and current-steering.
- Explore current based techniques.
- Model some other effects in common blocks such as the comparator metastability.
- Validate some of the models with available or future designs.

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- Dr. Umesh Patel
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- Damon Bradley
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- George Winkert
- Betsy Pugel

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- “Understanding Pipelined ADCs”. Maxim-IC Application Note 383: Mar 01, 2001.
- “Understanding Flash ADCs”. Maxim-IC Application Note 810: Oct 02, 2001

```
#include
<stdio.h>
int main ()
 {
 char str
 [100];
        printf (“Questions?“);

  scanf
  ("%s",str);
} return 0;
```

Acronyms

ADC – Analog-to-digital converter
AHDL – Analog Hardware Description Language
DAC – Digital-to-analog converter
DEM – Dynamic Element Matching
ENOB – Effective number of bits.
FS – Full scale voltage
GBW – Gain bandwidth
ILA – Individual Level Averaging
INL – Integral non-linearity
MDAC – Multiplying DAC
SAR – Successive Approximation Register
SFDR - Spurious Free Dynamic Range
SNDR – Signal-to-noise plus distortion ratio
SNR – Signal-to-noise ratio
THD – Total Harmonic Distortion
ΣΔM – Sigma-Delta Modulator