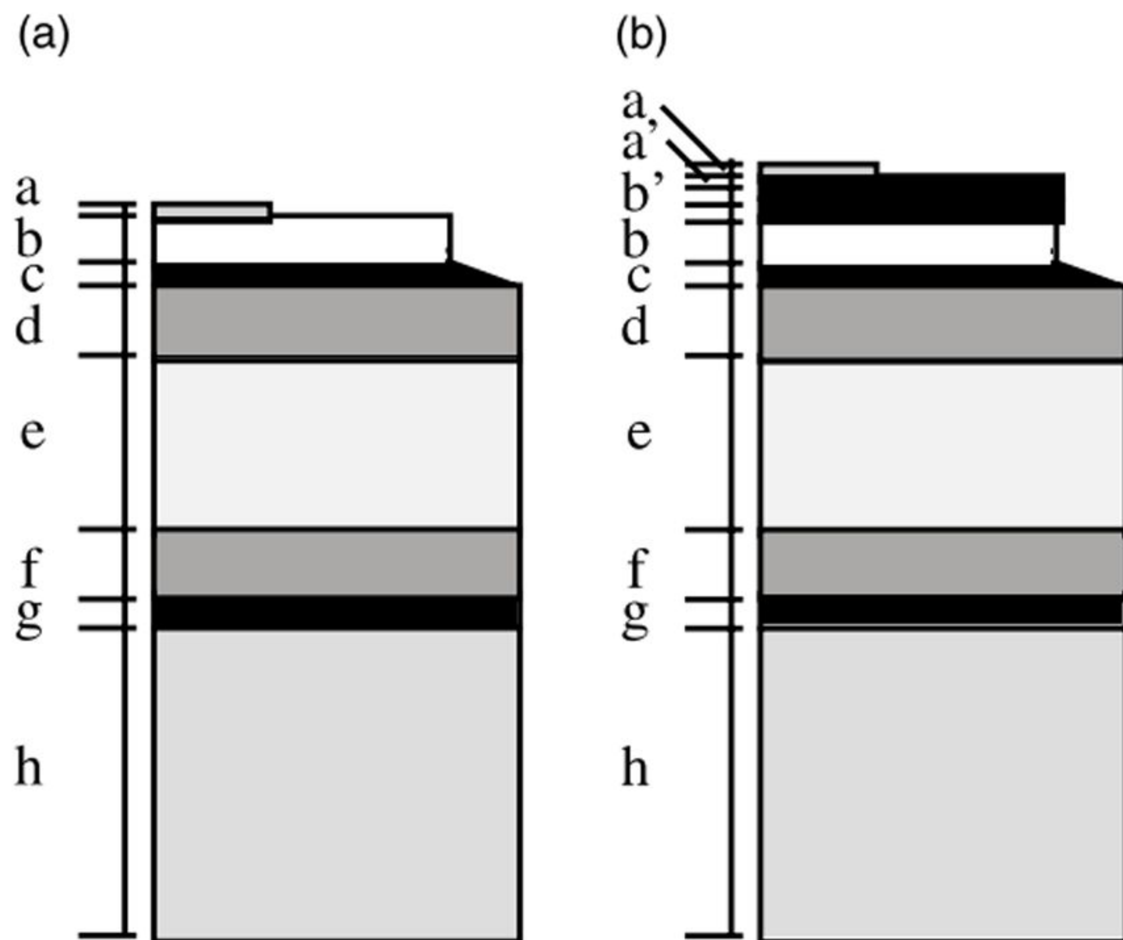


Fig. 1. Schematic representation of the multilayer in a multichip module of type A (a) and of type B (b).

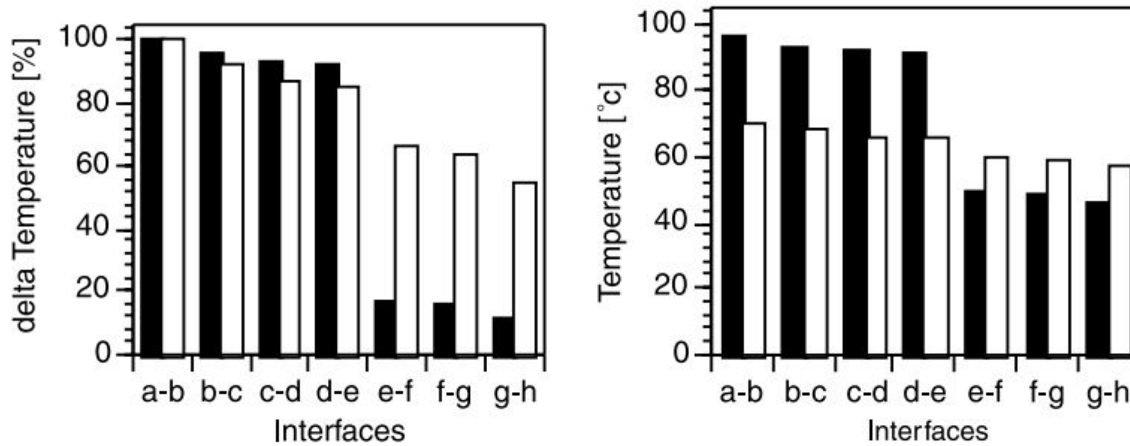


Fig. 2. (a) Temperature swing distribution at the interfaces of both stacks in Fig. 1 (black: type A, white: type B); a–b: Si, b–c: Si–solder, c–d: solder–Cu, d–e: Cu–ceramic, e–f: ceramic–Cu, f–g: Cu–solder, g–h: solder–base plate. (b) Temperature at the interfaces for a dissipated power of 100 W and a heat sink temperature of 40 °C (black: type A, white: type B).

Table 2
Differential elongation at the conditions of Fig. 2

Type A	
Si–bond wire	2 on 1000 μm
Si–Al_2O_3	4 on 12,000 μm
Al_2O_3–copper	28 on 55,000 μm
Type B	
Si–bond wire	0 on 1000 μm
Si–AlN	1 on 12,000 μm
AlN–AlSiC	7 on 30,000 μm

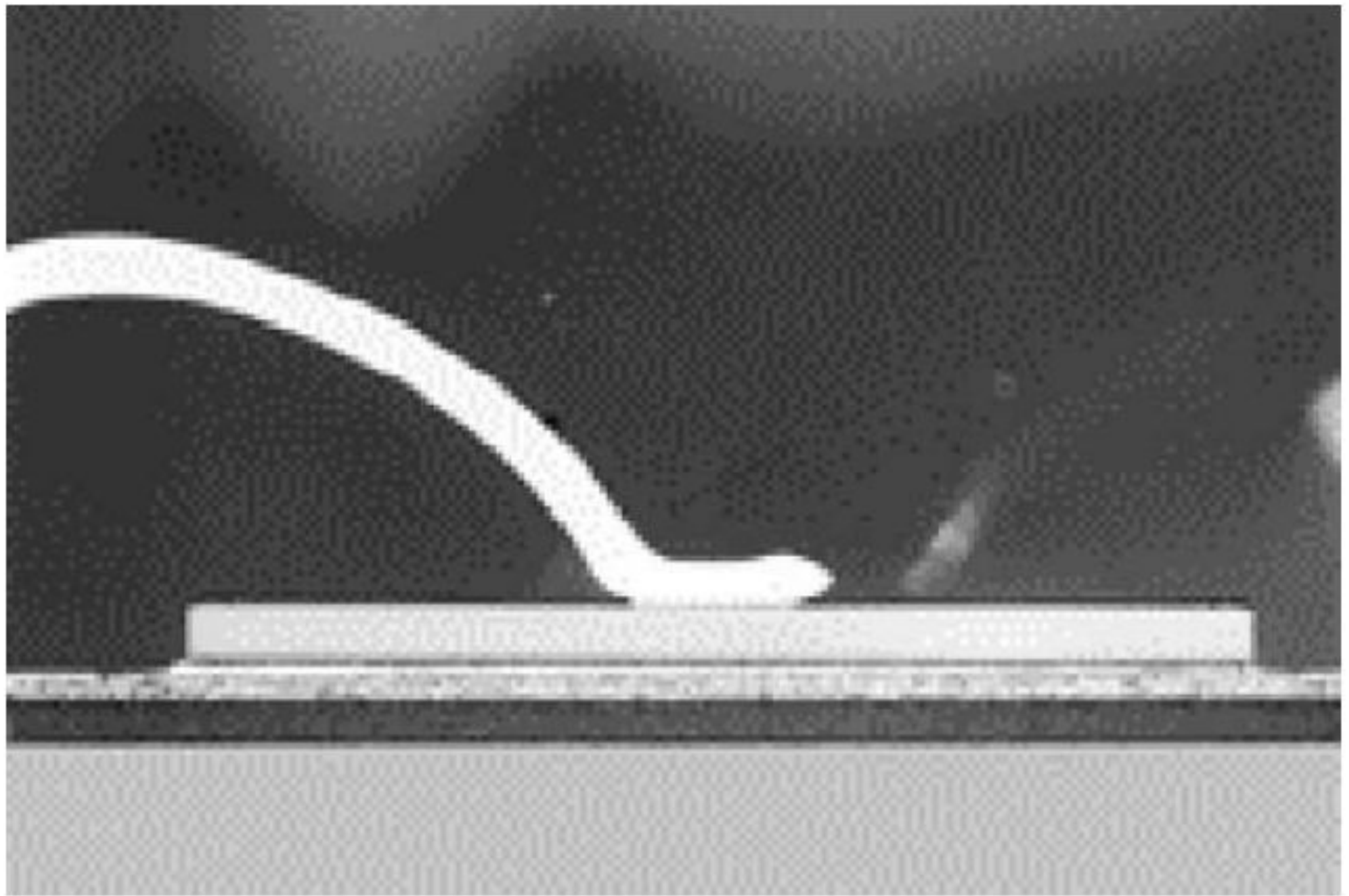


Fig. 3. Cross-section through the gate bond wire of an IGBT module of type A (cross-section, optical image 3×).

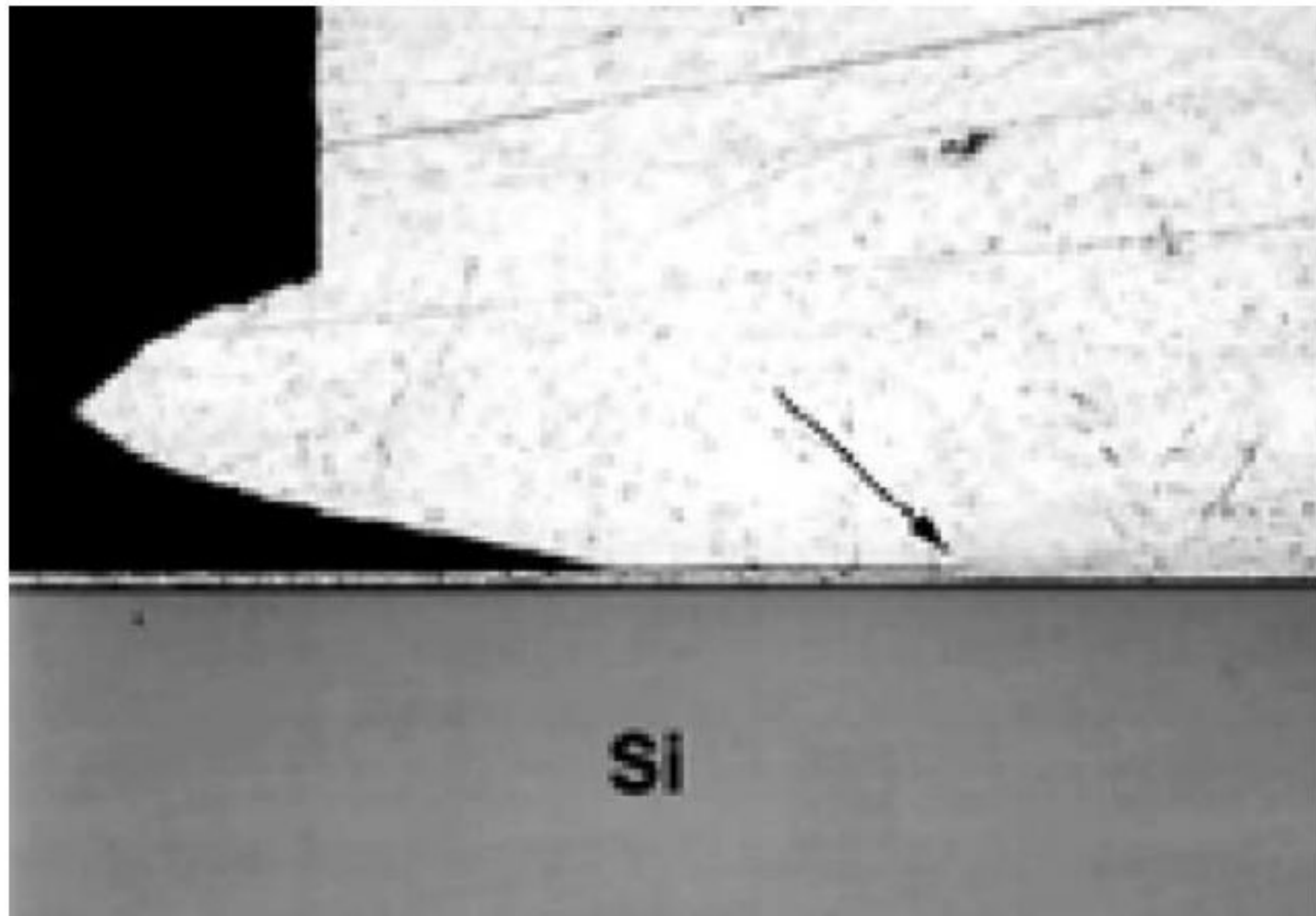


Fig. 4. Cross-section of a virgin wedge bond (tail side) on aluminum metalization, showing the transition to the interdiffused region (optical image, 120×).

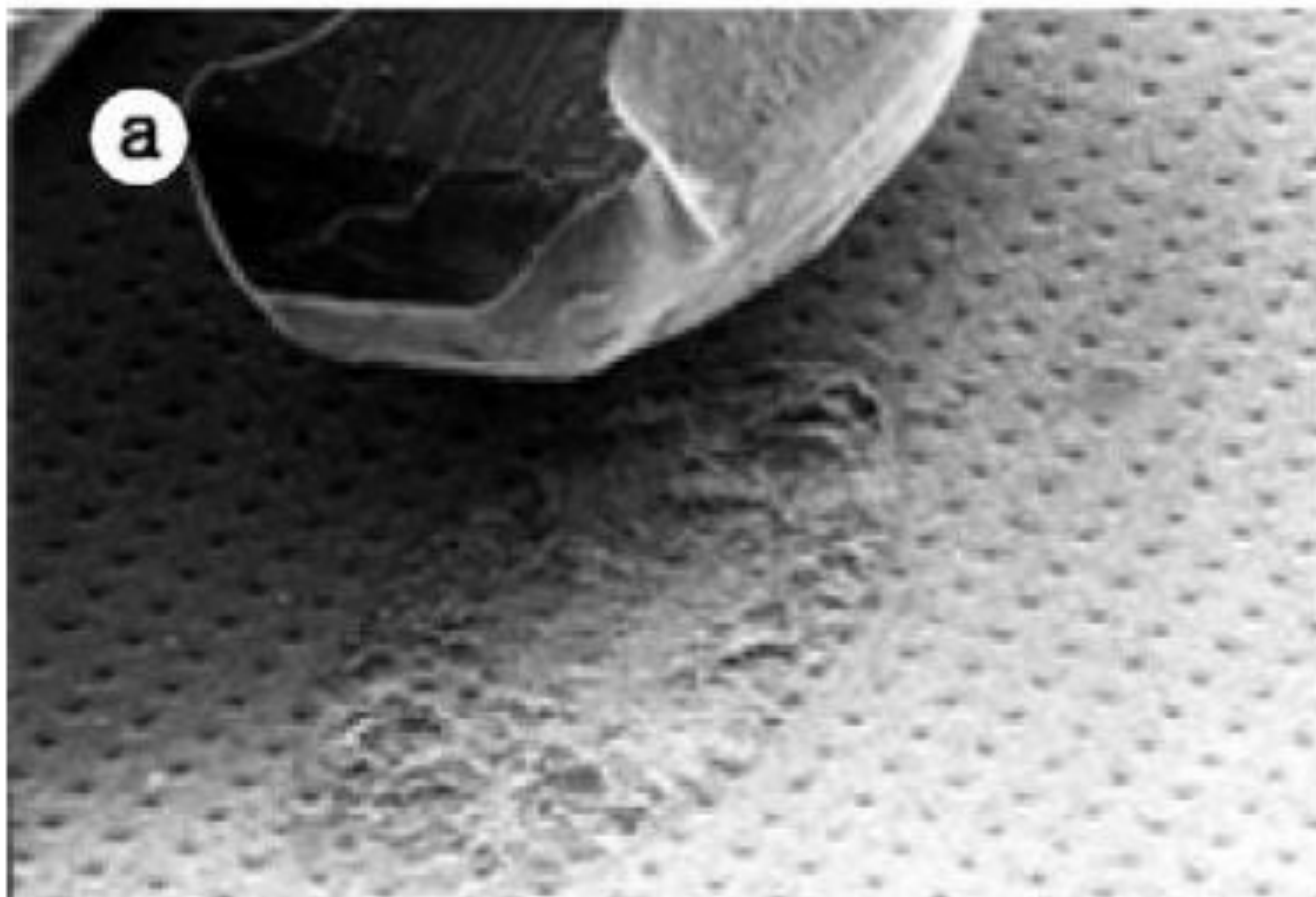
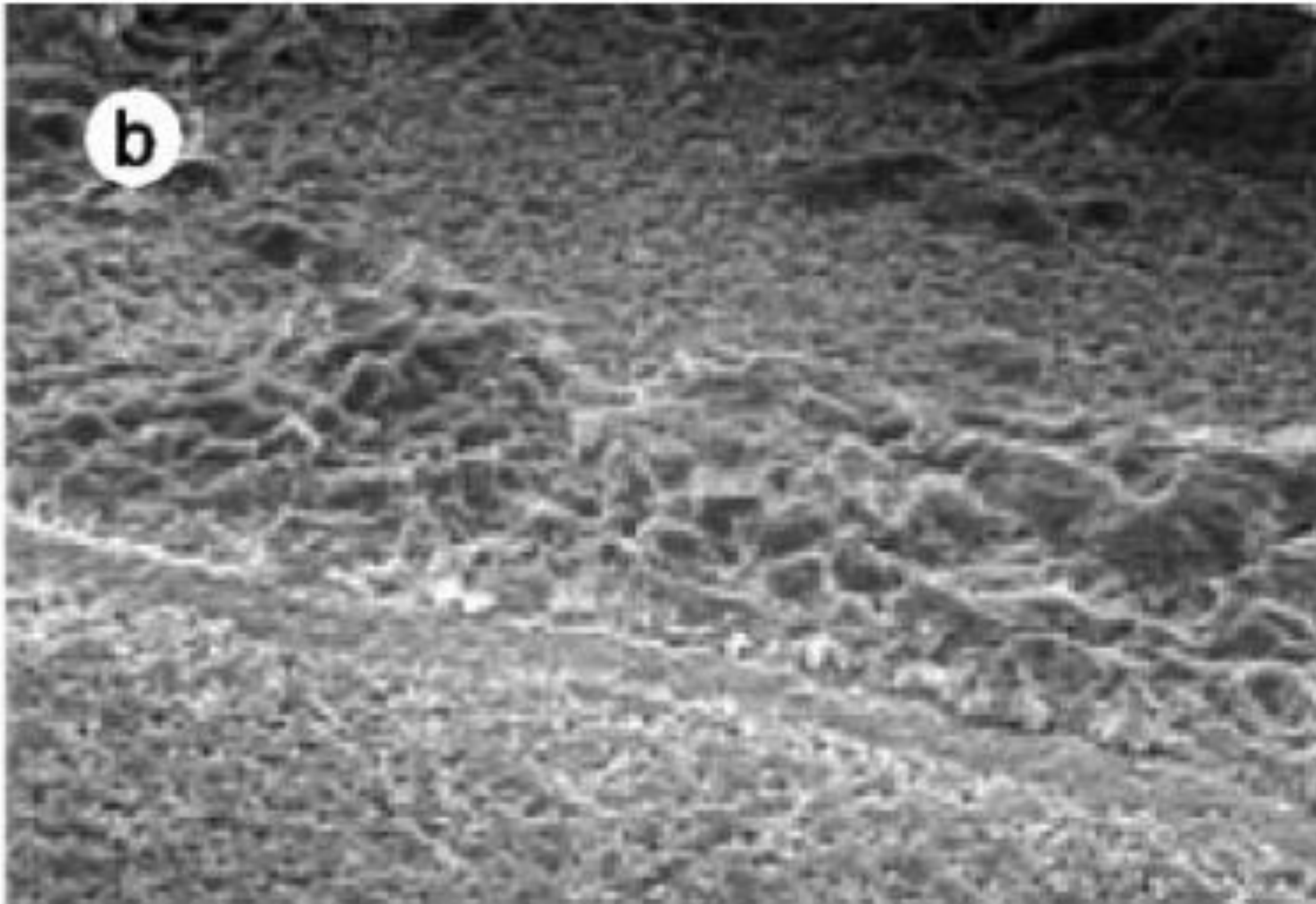


Fig. 5. (a) Bond wire lift off (SEM image, 40×). (



(b) Close view of the footprint of an aluminum bond wire after lift off (SEM image,

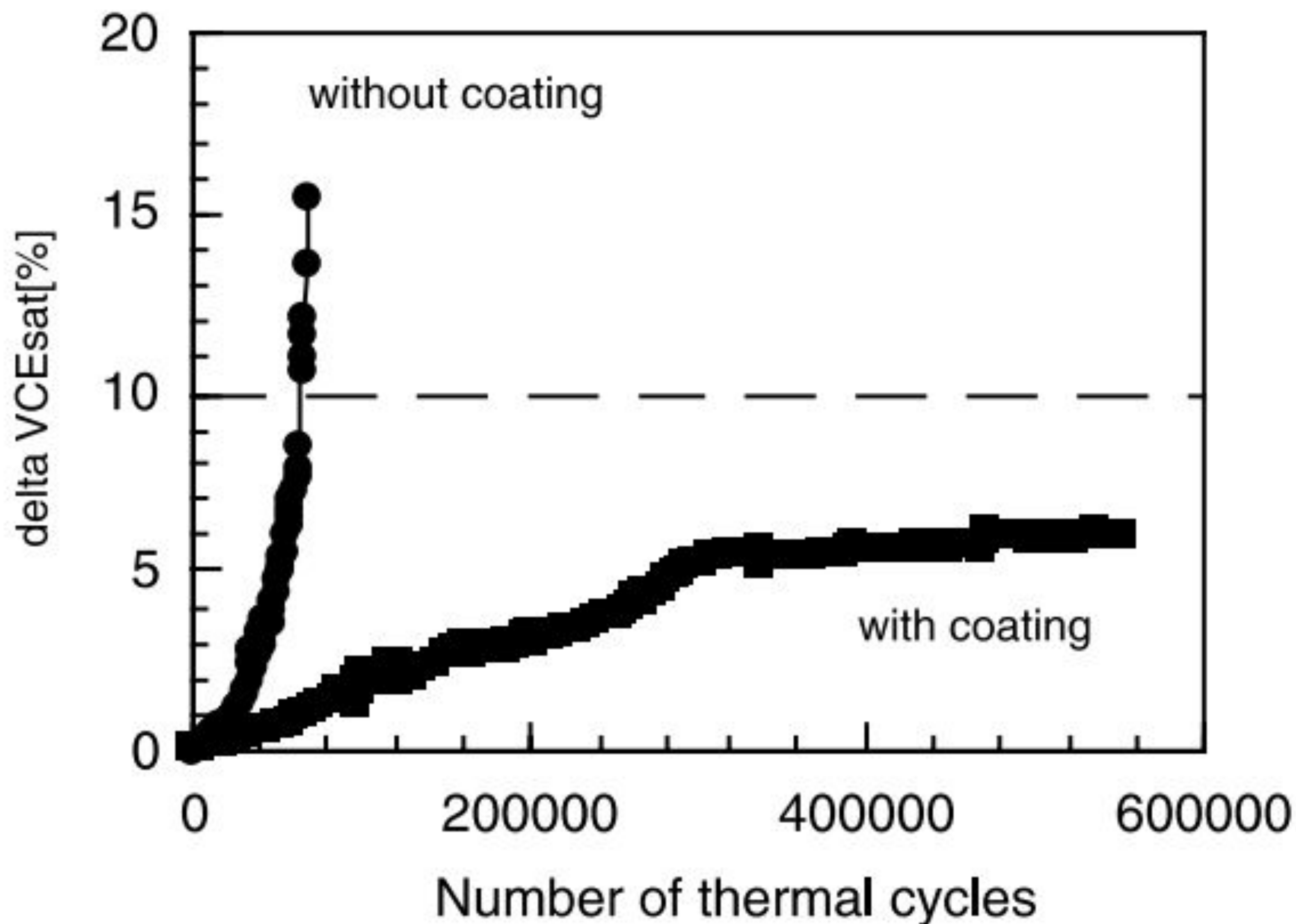


Fig. 6. Degradation of $V_{\mathrm{CE\,sat}}$ in an IGBT module without and with a polymeric bond wire coating layer; $T_{\mathrm{l}} = 65$ °C, $T_{\mathrm{h}} = 125$ °C, $t_{\mathrm{on}} = 0.8$ s, duty cycle 0.5.

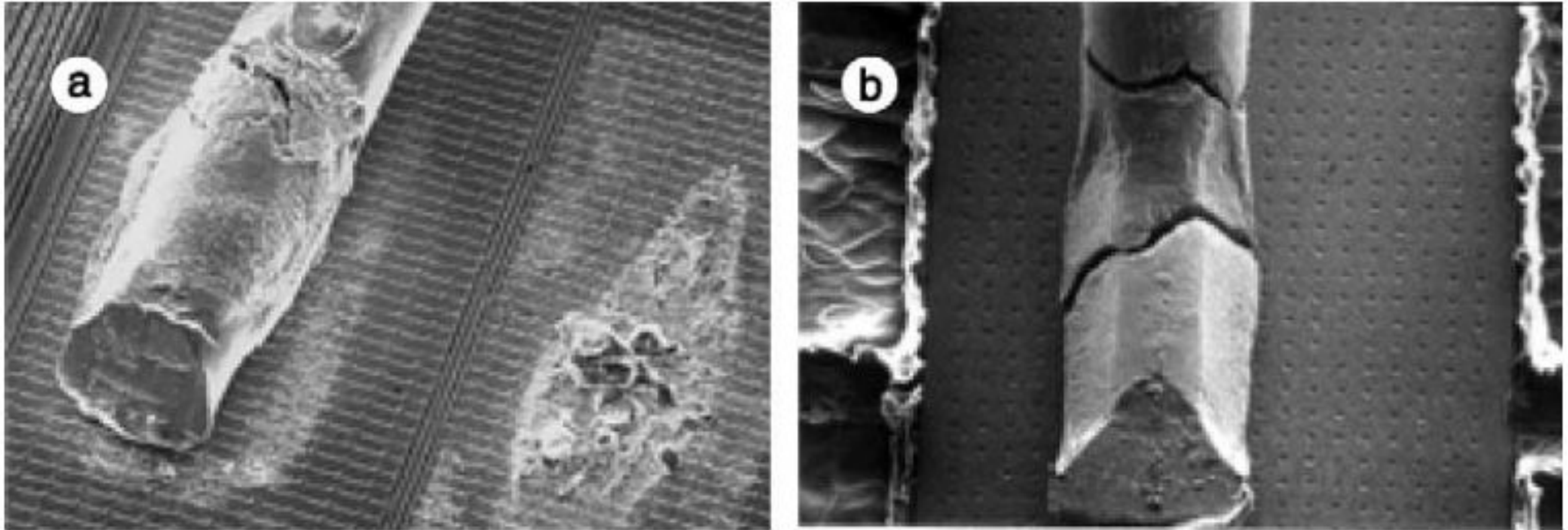


Fig. 7. (a) Bond wire heel cracking due to low-cycle fatigue stressing (SEM image, 25×). (b) Bond wire cracking due to improper bond wire coating (SEM image, 25×).

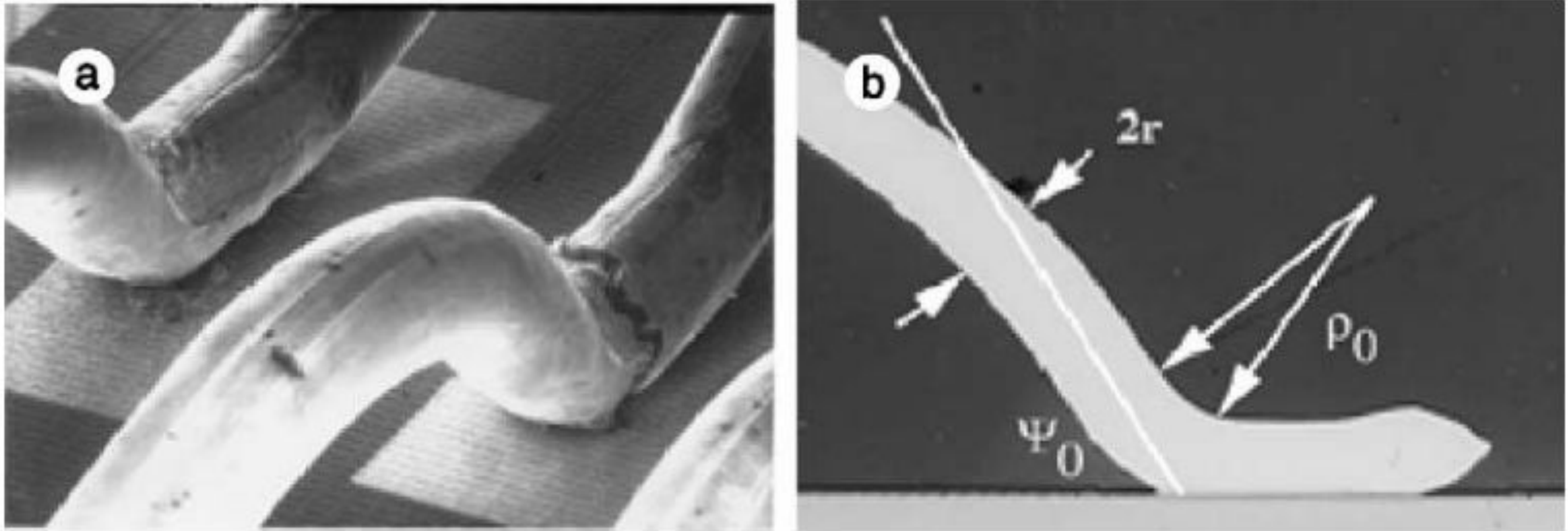


Fig. 8. (a) Heel cracking in a double wire bond. Crack initiation can also be observed in the double bond in the back (SEM image, 25×). (b) Parameter definition for the lifetime model.

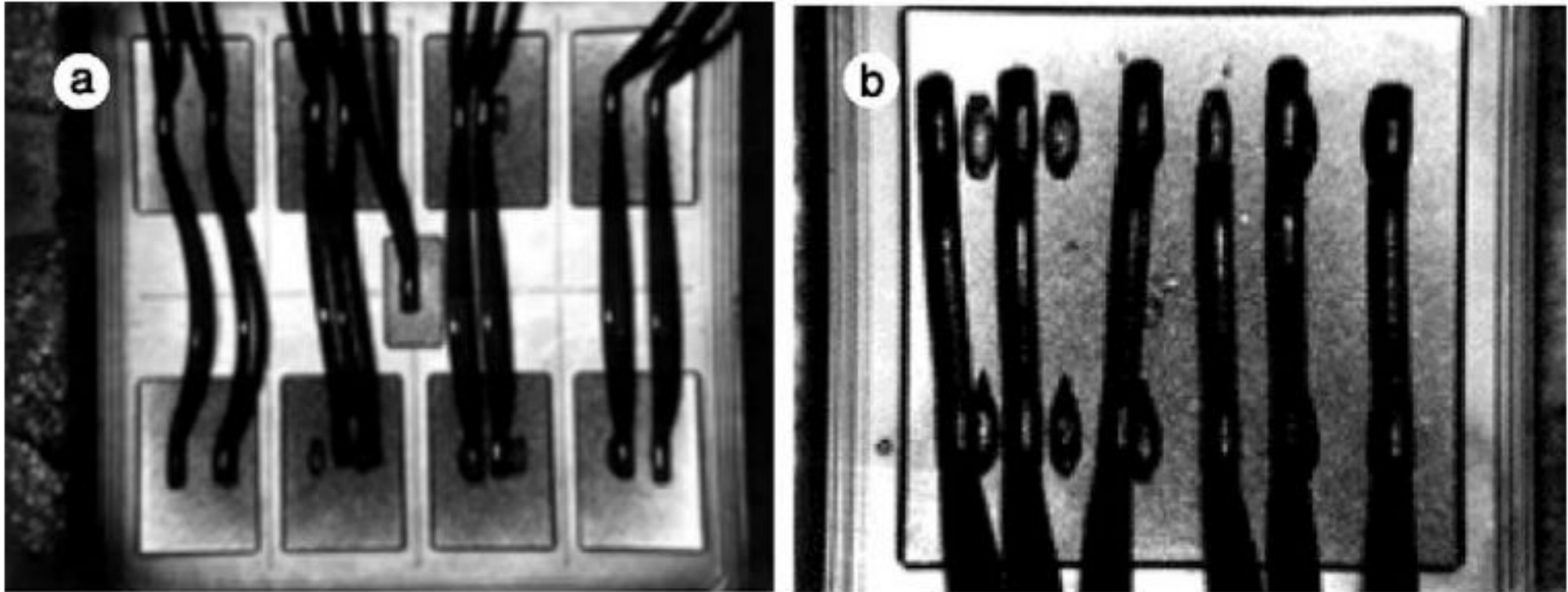


Fig. 9. (a) Reconstructed emitter and gate metalization of an IGBT (optical image, 4×). (b) Reconstructed metalization of a free-wheeling diode (optical image, 5×).

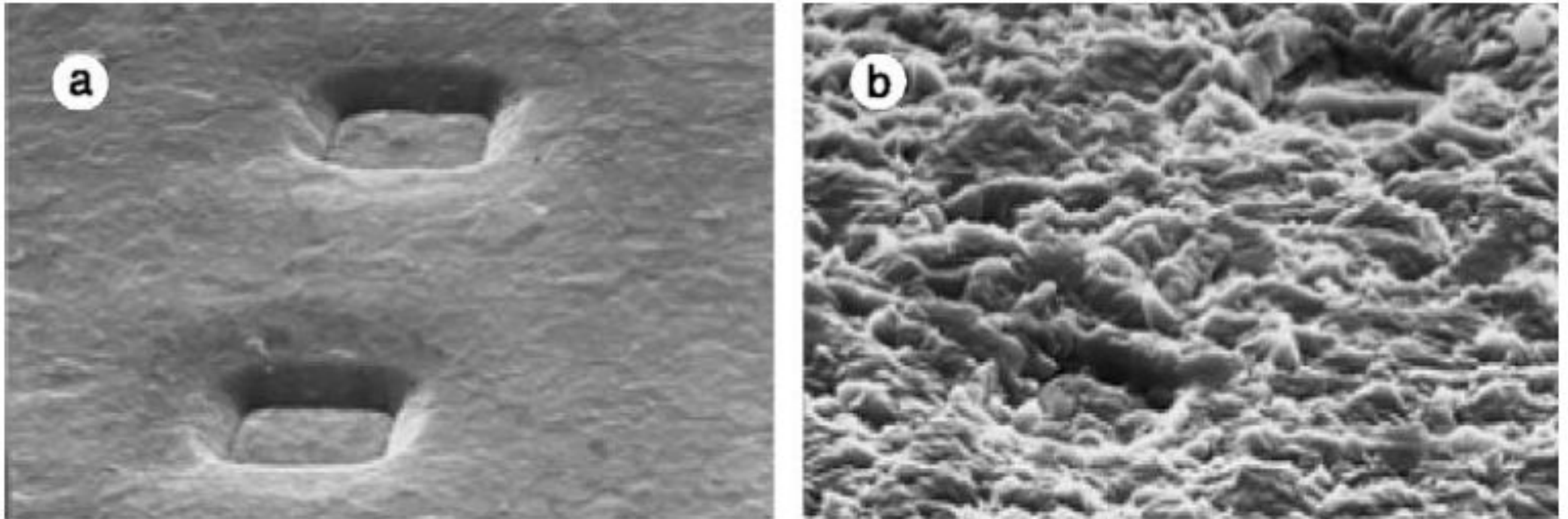
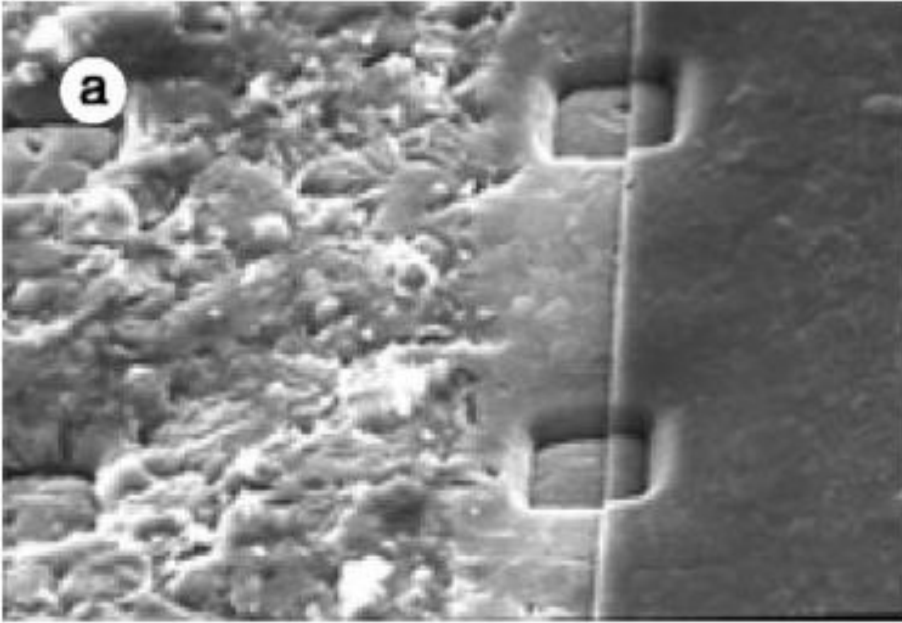


Fig. 10. (a) Emitter metalization of an IGBT chip before power cycling (SEM image, 1000×). (b) Reconstructed emitter metalization after 3.2 millions of power cycles between 85 and 125 °C (SEM image, 1000×).



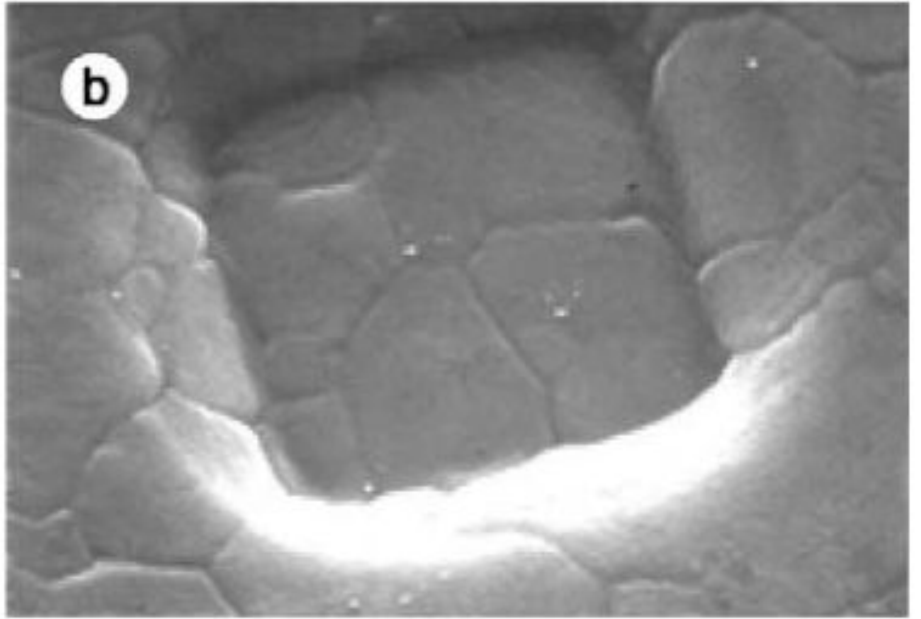


Fig. 11. (a) Reconstructed emitter metalization after removal of the polyimide passivation (SEM image, 800×). (b) Grain boundary depletion in a passivated emitter contact after power cycling (SEM image, 1500×).

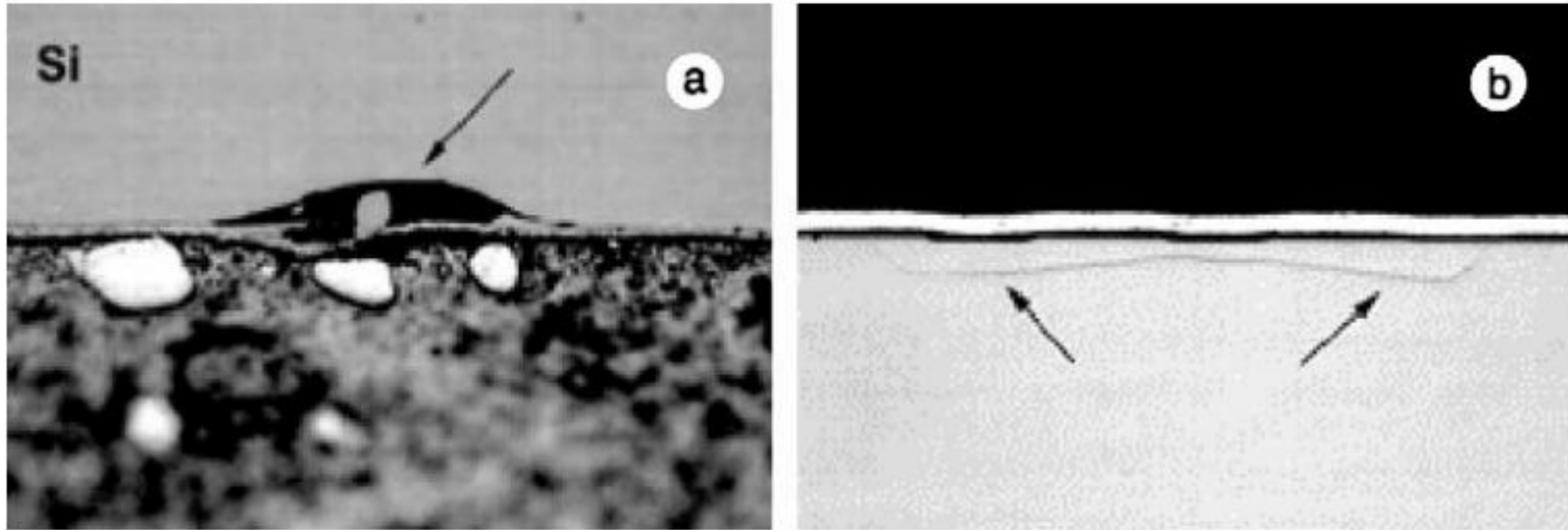


Fig. 12. (a) Notch in the silicon chip (micro-section, optical image, 250×). (b) Crack in the silicon chip due to bending stresses in the base plate (micro-section, optical image, 300×).

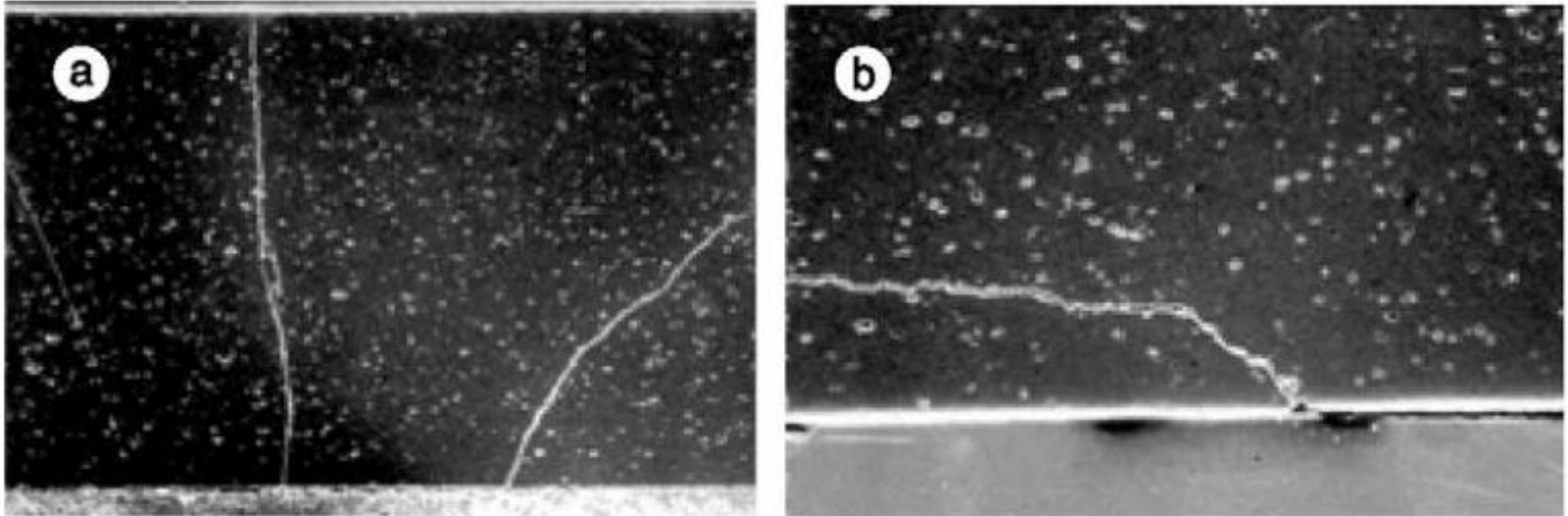


Fig. 13. (a) Vertical crack within an Al_2O_3 ceramic substrate, due bending stresses (micro-section, SEM image, 400×). (b) Crack within an Al_2O_3 ceramic substrate initiated from an inhomogeneity in the solder layer (micro-section, SEM image, 600×).

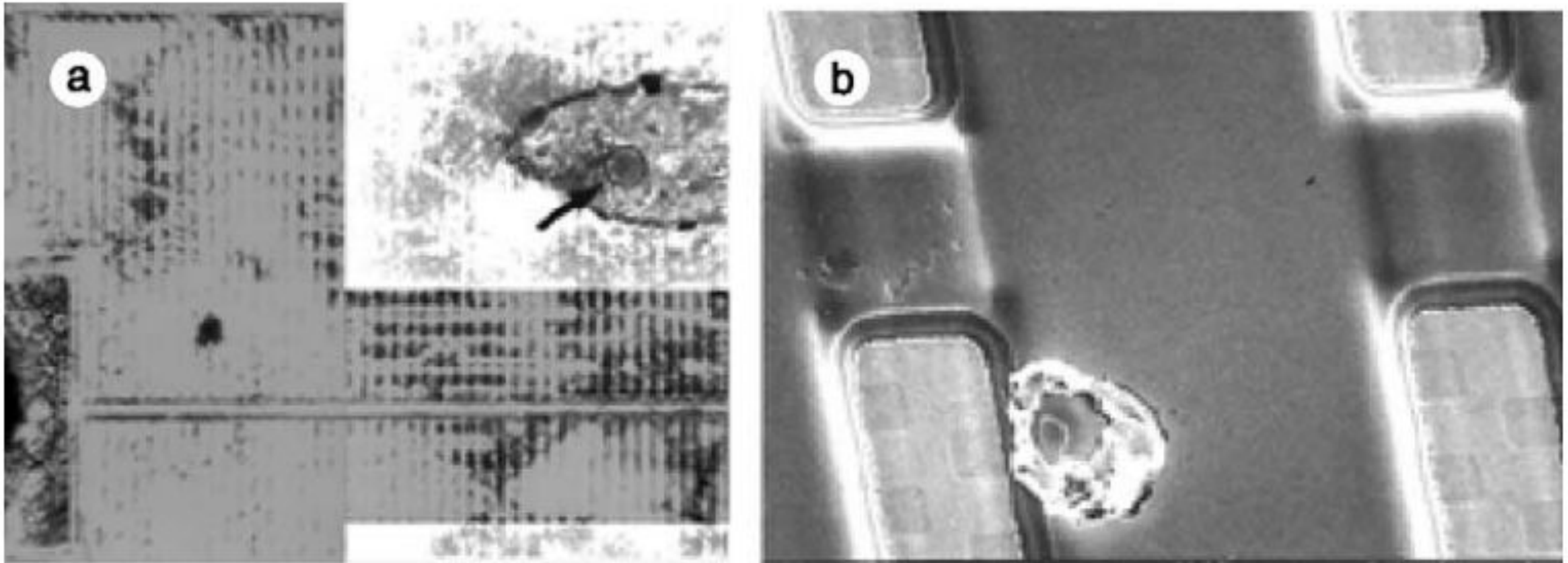


Fig. 14. (a) Localization of a leakage path between emitter and gate by liquid crystal microthermography (80×). (b) The hot spot is located below an emitter bond wire, and it is due to a mechanical damage of the polyoxide (SEM image 500×).

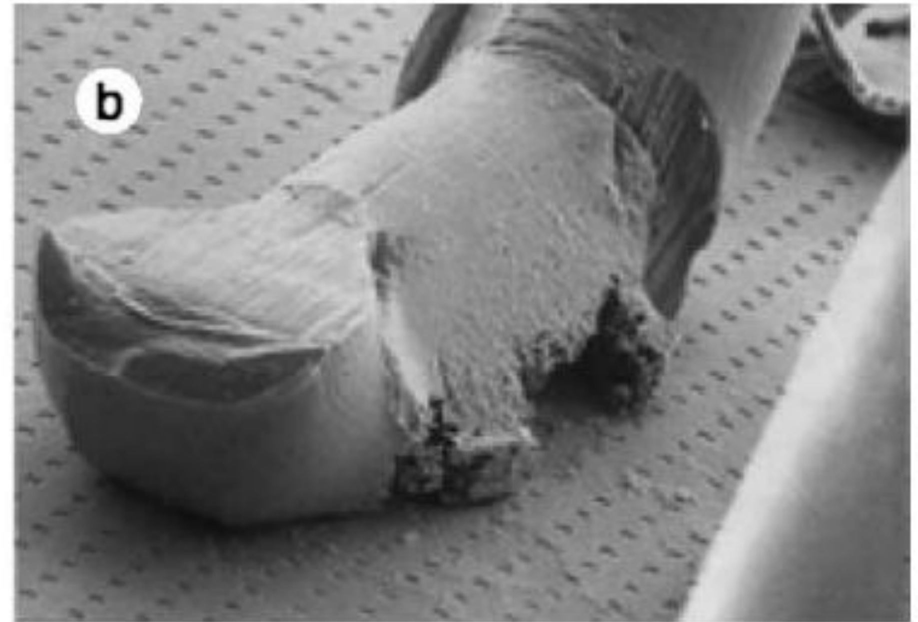
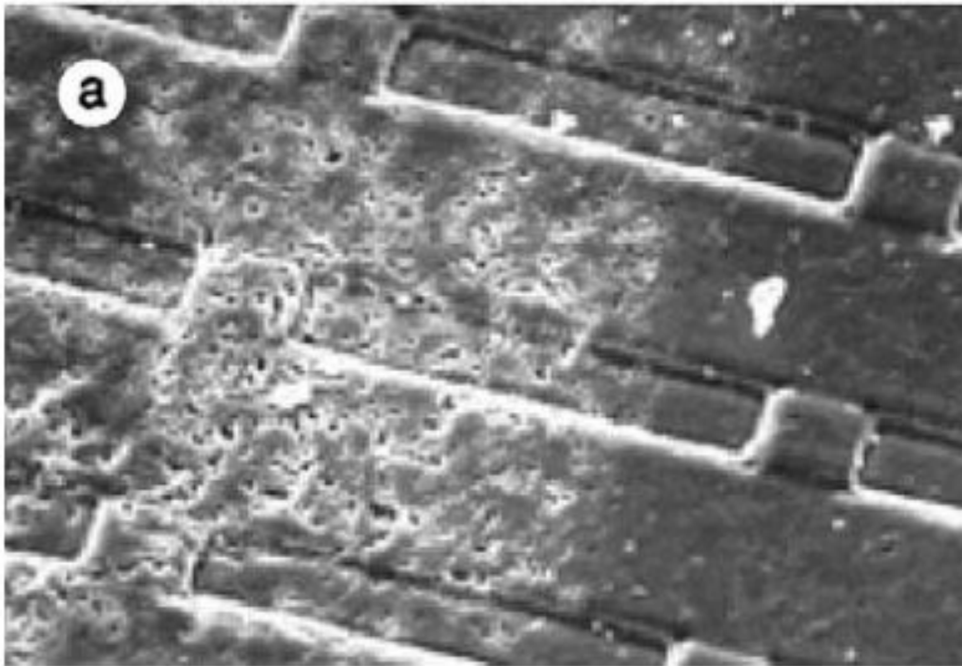


Fig. 15. (a) Rupture of emitter bond wires due to stress corrosion (SEM image, 30×). (b) Detail of a corroded emitter bond wire (SEM image, 80×).



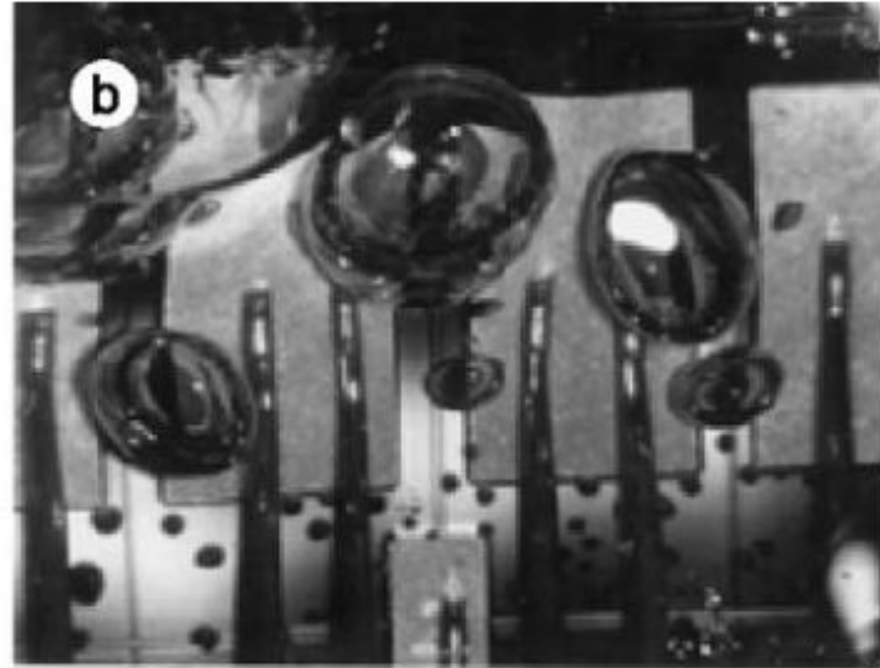


Fig. 16. (a) Corroded emitter bond pad close to an emitter bond wire (SEM image, 160×). (b) Formation of gaseous inclusions into the silicone gel during power cycling (optical image, 8×).

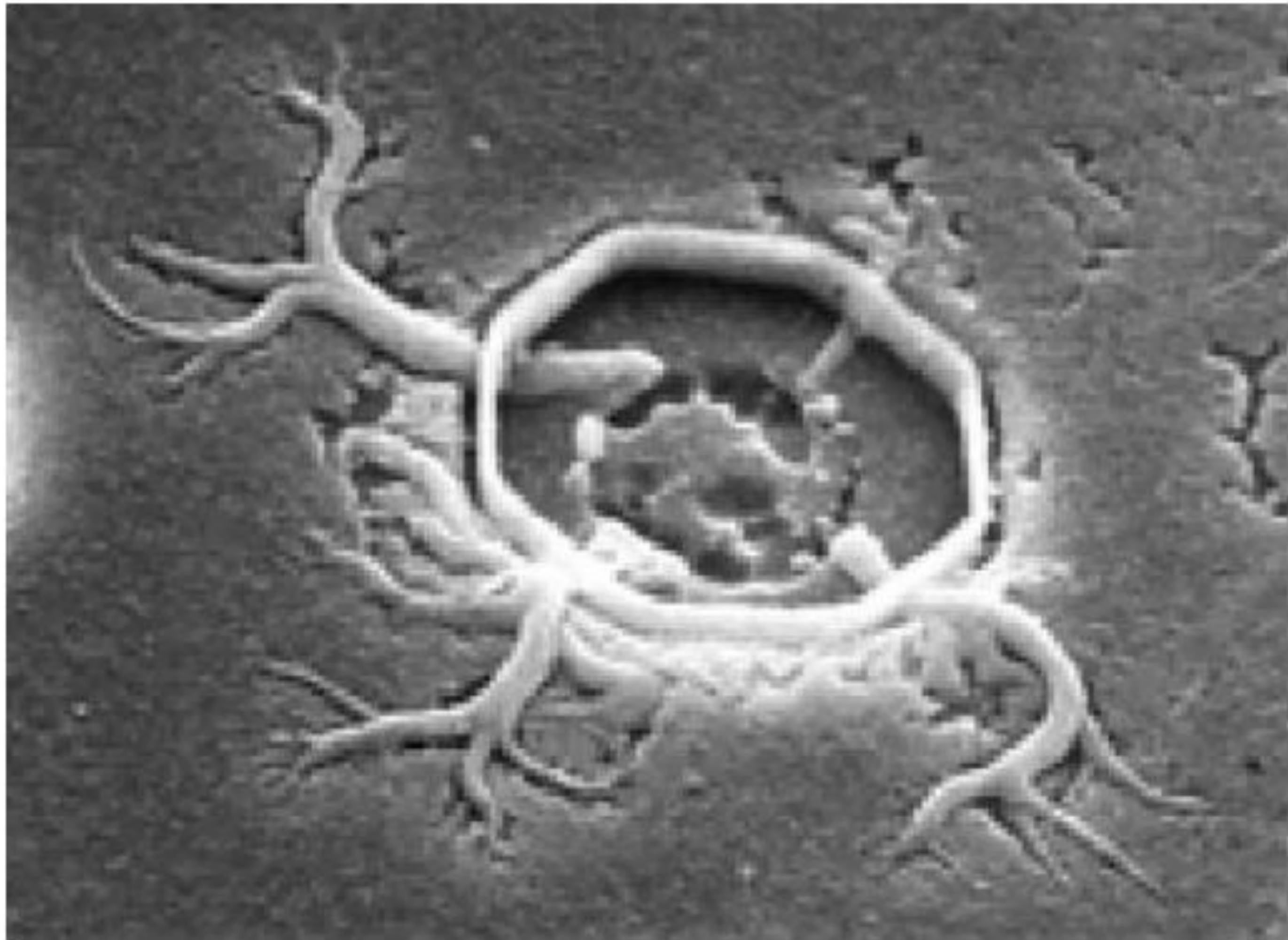
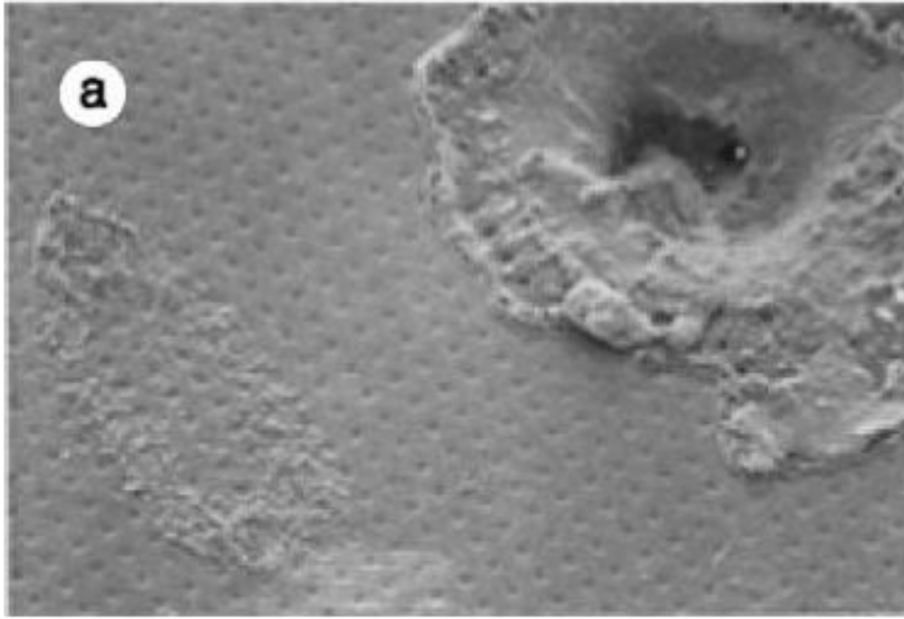


Fig. 18. Polysilicon filamentation in an IGBT as a consequence of a short circuit between gate and emitter, due to pre-damaged insulation during wire bonding (SEM image, 2000×).



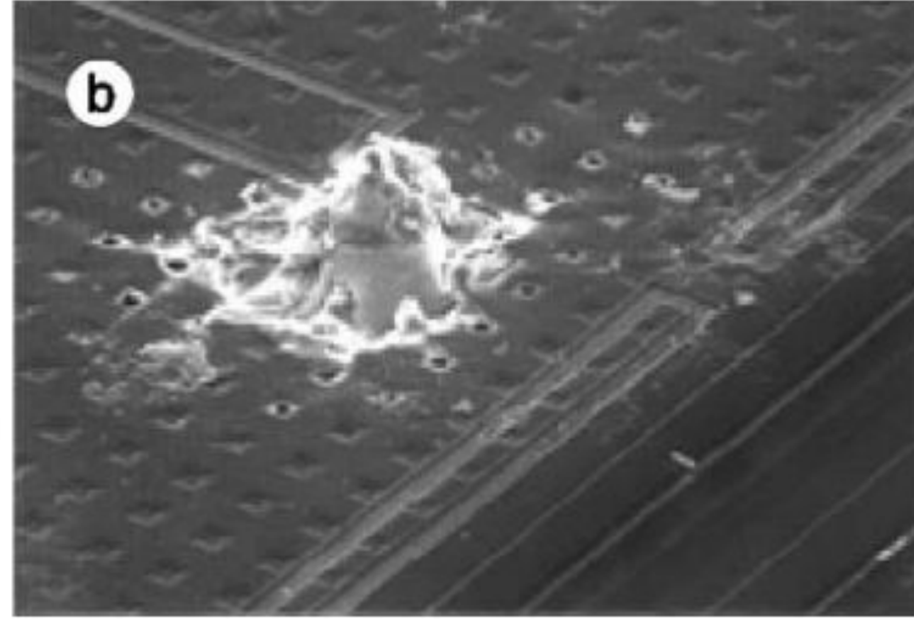


Fig. 20. (a) Melted pit in an IGBT due to a latch up event, which occurred in conjunction with bond wire lift off (SEM image, 50×). (b) Same effects than in the previous image but localized to some few cells (SEM image, 90×).