Lecture 5
System Buses.
(Continuation)

In what topology are combined bi-directional data transmission channels of PCIe?

The PCI Express system bus is a set of independent **serial** bi-directional data transmission channels combined in a **star topology.**

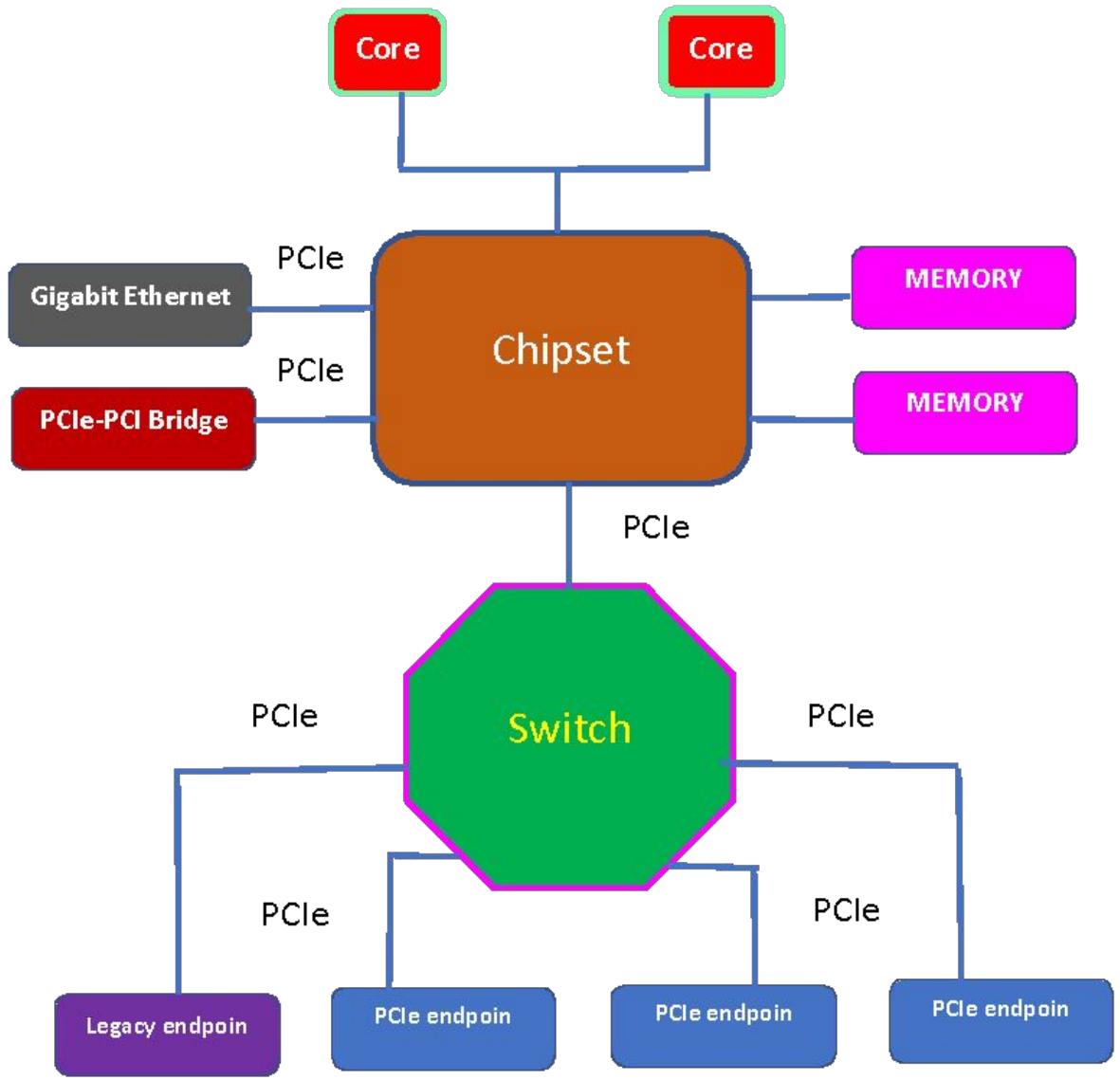
Can the PCIe connection be said to meet the system bus requirements?

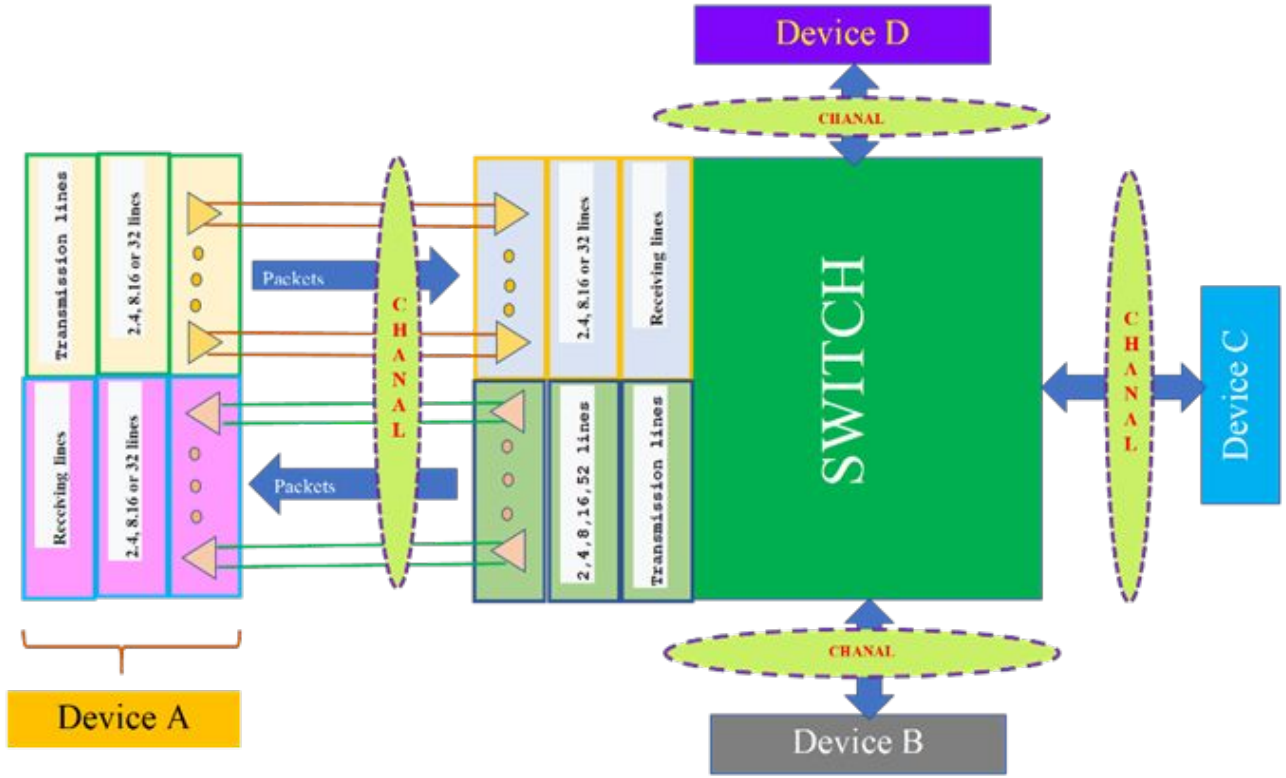
Each of the devices participating in the exchange is connected to the opposite end of the channel. Thus, a point-to-point connection is established between each device and the switch. Thanks to this scheme, any device through a switch can be connected to any other, which is required from the system bus.

How is information transmitted in PCIe?

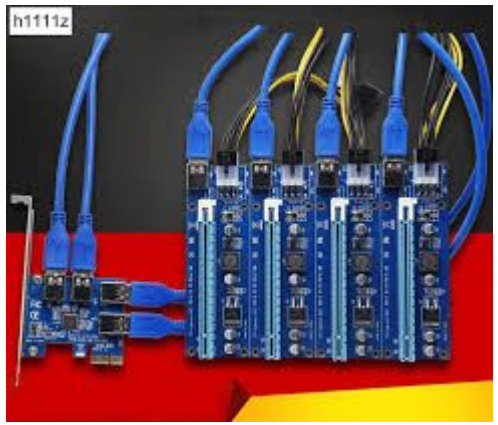
Information in PCI Express is transmitted in packets, which can contain data, addresses, service requests, etc., and all types of packets are transmitted over the same lines as data packets. Information exchange is carried out simultaneously (but not synchronously) on all available lines.

The PCI Express bus is controlled by a controller called the Host Bridge.





System bus organization based on PCI-E standard.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What kind of devices that implement PCIe may attach to PCIe links from the chipset?

PCIe links from the chipset may attach to the following kinds of devices that implement PCIe:

Switch: The switch manages multiple PCIe streams.

PCIe endpoint: An I/O device or controller that implements PCIe, such as a Gigabit Ethernet switch, a graphics or video controller, disk interface, or a communications controller.

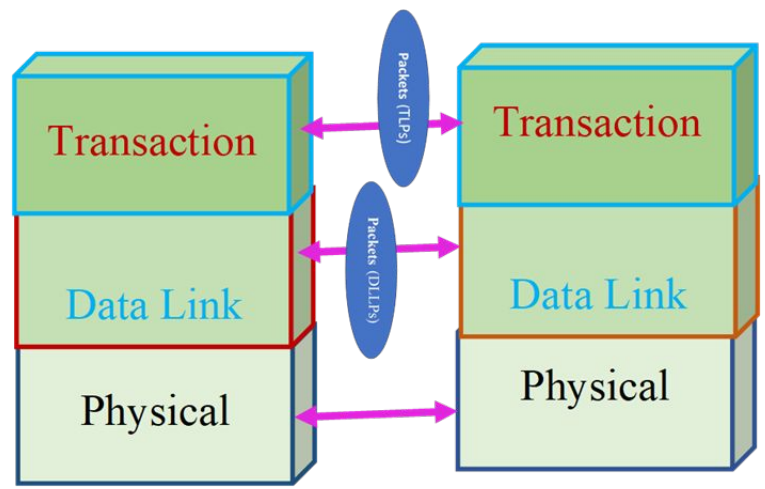
Legacy endpoint: Legacy endpoint category is intended for existing designs that have been migrated to PCI Express, and it allows legacy behaviors such as use of I/O space and locked transactions. PCI Express endpoints are not permitted to require the use of I/O space at runtime and must not use locked transactions. By distinguishing these categories, it is possible for a system designer to restrict or eliminate legacy behaviors that have negative impacts on system performance and robustness.

PCIe/PCI bridge: Allows older PCI devices to be connected to PCIe-based systems.

What types of Layers does the PCIe protocol architecture encompass?

The PCIe protocol architecture encompasses the following layers:

- Physical: Consists of the actual wires carrying the signals, as well as circuitry and logic to support ancillary features required in the transmission and receipt of the 1s and 0s.
- Data link: Is responsible for reliable transmission and flow control. Data packets generated and consumed by the DLL are called Data Link Layer Packets (DLLPs).
- Transaction: Generates and consumes data packets used to implement load/ store data transfer mechanisms and also manages the flow control of those packets between the two components on a link. Data packets generated and consumed by the TL are called Transaction Layer Packets (TLPs).



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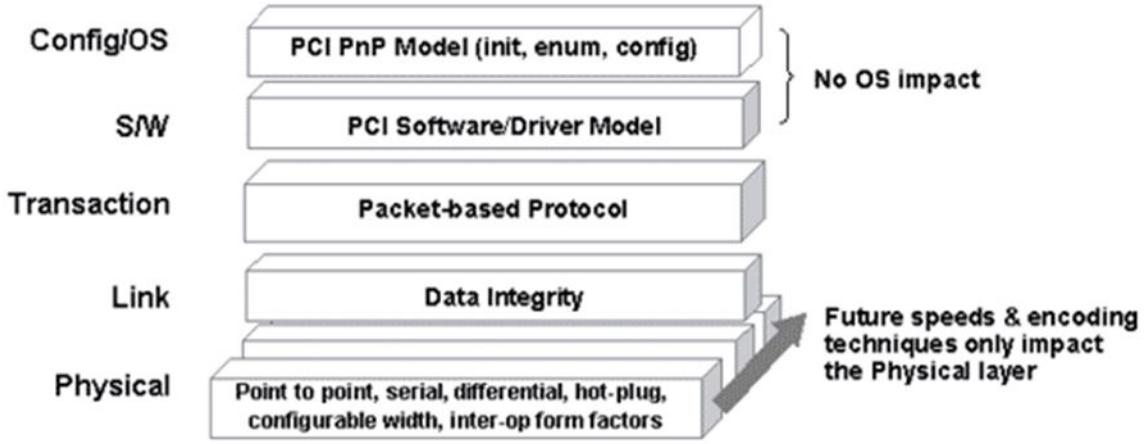
Above the TL are software layers that generate read and write requests that are transported by the transaction layer to the I/O devices using a packet-based transaction protocol.



The HyperTransport bus is organized at different levels (Figure 9):

- at the physical level, the bus is represented by data lines, control, clock, as well as controllers and standard electrical signals;
- at the data transmission level, the order of initialization and configuration of devices, establishment and termination of a communication session, cyclic control of data adequacy, allocation of packets for data transmission is determined;
- at the protocol level, commands for allocating virtual communication channels, rules for controlling data flow are defined;
- at the transaction level, protocol commands are concretized into control signals, for example, read or write;
- at the session level are determined network energy management rules and other general commands.